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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





High Temperature Triple Half-bridge Driver with SPI and PWM

PRELIMINARY DATASHEET

Features

- Supply voltage up to 40V
- R_{DSon} typically 0.8Ω at 25°C , maximum 1.8Ω at 200°C
- Up to 1.0A output current
- Three half-bridge outputs formed by three high-side and three low-side drivers
- Capable of switching loads such as DC motors, bulbs, resistors, capacitors, and inductors
- PWM capability up to 25kHz for each high-side output controlled by external PWM signal
- No shoot-through current
- Outputs short-circuit protected
- Selective overtemperature protection for each switch and overtemperature prewarning
- Undervoltage protection
- Various diagnostic functions such as shorted output, open load, overtemperature and power-supply fail detection
- Serial data interface, Daisy Chain capable, up to 2MHz clock frequency
- QFN18 package

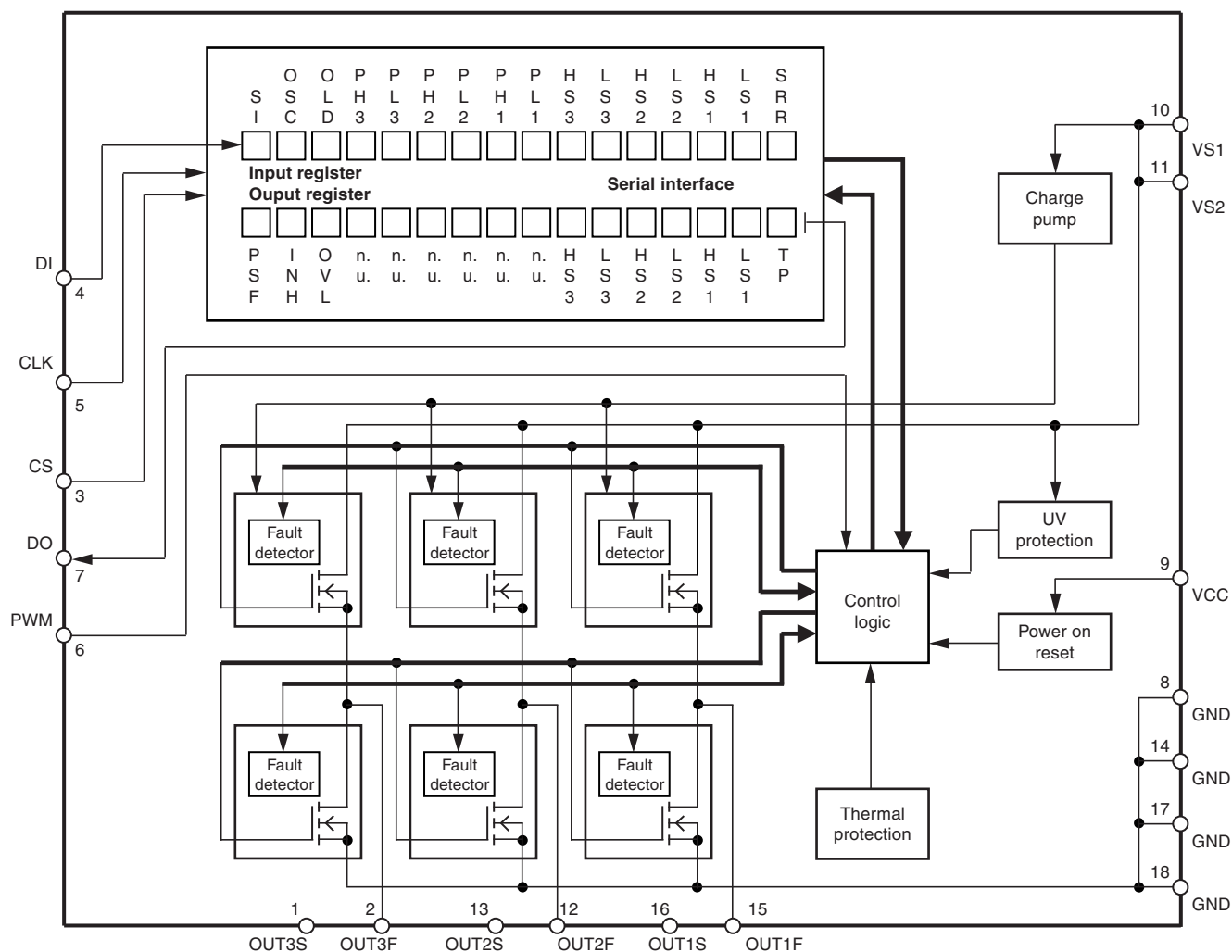
1. Description

The Atmel® ATA6832C is a fully protected driver IC specially designed for high temperature applications. In mechatronic solutions, for example turbo charger or exhaust gas recirculation systems, many flaps have to be controlled by DC motor driver ICs which are located very close to the hot engine or actuator where ambient temperatures up to 150°C are usual. Due to the advantages of SOI technology junction temperatures up to 200°C are allowed. This enables new cost effective board design possibilities to achieve complex mechatronic solutions.

The Atmel ATA6832C is a triple half-bridge driver to control up to three different loads by a microcontroller in automotive and industrial applications. Each of the three high-side and three low-side drivers is capable of driving currents up to 1.0A. Due to the enhanced PWM signal (up to 25kHz) it is possible to generate a smooth control of, for example, a DC motor without any noise. The drivers are internally connected to form three half-bridges and can be controlled separately from a standard serial data interface, enabling all kinds of loads, such as bulbs, resistors, capacitors and inductors, to be combined. The IC design especially supports the application of H-bridges to drive DC motors.

Protection is guaranteed with respect to short-circuit conditions, overtemperature and undervoltage. Various diagnostic functions and a very low quiescent current in standby mode enable a wide range of applications. Automotive qualification (protection against conducted interferences, EMC protection and 1.5-kV ESD protection) gives added value and enhanced quality for exacting requirements of automotive applications.

Figure 1-1. Block Diagram



2. Pin Configuration

Figure 2-1. Pinning QFN24

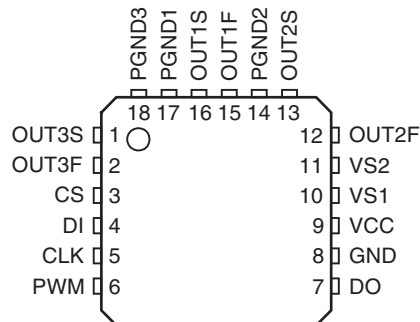


Table 2-1. Pin Description

| Pin | Symbol | Function |
|-----|--------|--|
| 1 | OUT3S | Used only for final testing, to be connected to OUT3F |
| 2 | OUT3F | Half-bridge output 3; formed by internally connecting power MOS high-side switch 3 and low-side switch 3 with internal reverse diodes; short circuit protection; overtemperature protection; diagnosis for short and open load |
| 3 | CS | Chip select input; 5V CMOS logic level input with internal pull-up; low = serial communication is enabled, high = disabled |
| 4 | DI | Serial data input; 5V CMOS logic level input with internal pull-down; receives serial data from the control device; DI expects a 16-bit control word with LSB transferred first |
| 5 | CLK | Serial clock input; 5V CMOS logic level input with internal pull-down; controls serial data input interface and internal shift register ($f_{max} = 2\text{MHz}$) |
| 6 | PWM | PWM input; 5V CMOS logic level input with internal pull-down |
| 7 | DO | Serial data output; 5V CMOS logic-level tri-state output for output (status) register data; sends 16-bit status information to the microcontroller (LSB transferred first); output will remain tri-stated unless device is selected by CS = low; this allows several ICs to operate on only one data-output line |
| 8 | GND | Ground |
| 9 | VCC | Logic supply voltage (5V) |
| 10 | VS1 | Power supply for output stages OUT1 and OUT2; internal supply |
| 11 | VS2 | Power supply for output stages OUT2 and OUT3; internal supply |
| 12 | OUT2F | Half-bridge output 2; formed by internally connected power MOS high-side switch 2 and low-side switch 2 with internal reverse diodes; short circuit protection; overtemperature protection; diagnosis for short and open load |
| 13 | OUT2S | Used only for final testing, to be connected to OUT2F |
| 14 | PGND2 | Power ground OUT2 |
| 15 | OUT1F | Half-bridge output 1; formed by internally connected power MOS high-side switch 1 and low-side switch 1 with internal reverse diodes; short circuit protection; overtemperature protection; diagnosis for short and open load |
| 16 | OUT1S | Used only for final testing, to be connected to OUT1F |
| 17 | PGND1 | Power ground OUT1 |
| 18 | PGND3 | Power ground OUT3 |

3. Functional Description

3.1 Serial Interface

Data transfer starts with the falling edge of the CS signal. Data must appear at DI synchronized to CLK and is accepted on the falling edge of the CLK signal. The LSB (bit 0, SRR) has to be transferred first. Execution of new input data is enabled on the rising edge of the CS signal. When CS is high, pin DO is in tri-state condition. This output is enabled on the falling edge of CS. Output data will change their state with the rising edge of CLK and stay stable until the next rising edge of CLK appears. LSB (bit 0, TP) is transferred first.

Figure 3-1. Data Transfer

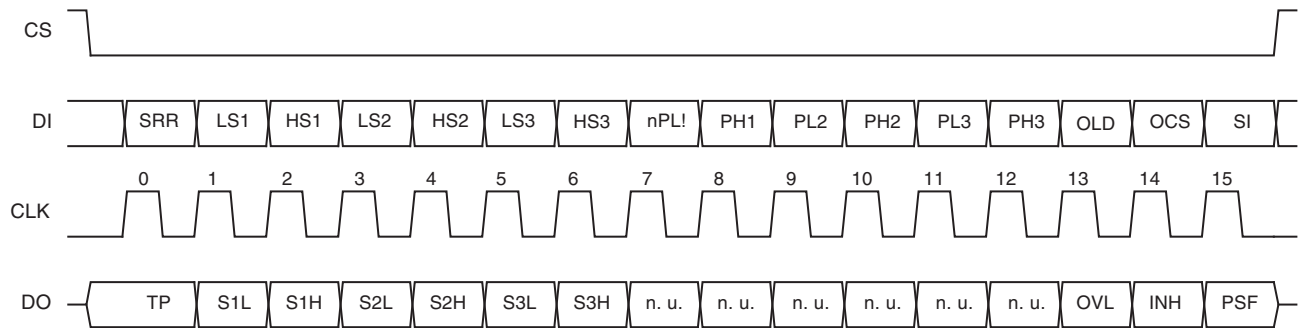


Table 3-1. Input Data Protocol

| Bit | Input Register | Function |
|-----|----------------|--|
| 0 | SRR | Status register reset (high = reset; the bits PSF and OVL in the output data register are set to low) |
| 1 | LS1 | Controls output LS1 (high = switch output LS1 on) |
| 2 | HS1 | Controls output HS1 (high = switch output HS1 on) |
| 3 | LS2 | See LS1 |
| 4 | HS2 | See HS1 |
| 5 | LS3 | See LS1 |
| 6 | HS3 | See HS1 |
| 7 | PL1 | Output LS1 additionally controlled by PWM Input |
| 8 | PH1 | Output HS1 additionally controlled by PWM Input |
| 9 | PL2 | See PL1 |
| 10 | PH2 | See PH1 |
| 11 | PL3 | See PL1 |
| 12 | PH3 | See PH1 |
| 13 | OLD | Open load detection (low = on) |
| 14 | OCS | Overcurrent shutdown (high = overcurrent shutdown is active) |
| 15 | SI | Software inhibit; low = standby, high = normal operation (data transfer is not affected by the standby function because the digital part is still powered) |

Table 3-2. Output Data Protocol

| Bit | Output (Status) Register | Function |
|-----|--------------------------|--|
| 0 | TP | Temperature prewarning: high = warning |
| 1 | Status LS1 | Normal operation: high = output is on, low = output is off Open-load detection: high = open load, low = no open load (correct load condition is detected if the corresponding output is switched off); not affected by SRR |
| 2 | Status HS1 | Normal operation: high = output is on, low = output is off Open-load detection: high = open load, low = no open load (correct load condition is detected if the corresponding output is switched off); not affected by SRR |
| 3 | Status LS2 | Description see LS1 |
| 4 | Status HS2 | Description see HS1 |
| 5 | Status LS3 | Description see LS1 |
| 6 | Status HS3 | Description see HS1 |
| 7 | n. u. | Not used |
| 8 | n. u. | Not used |
| 9 | n. u. | Not used |
| 10 | n. u. | Not used |
| 11 | n. u. | Not used |
| 12 | n. u. | Not used |
| 13 | OVL | Over-load detected: set high, when at least one output is switched off by a short-circuit condition or an overtemperature event. Bits 1 to 6 can be used to detect the affected switch |
| 14 | INH | Inhibit: this bit is controlled by software (bit SI in input register) High = standby, low = normal operation |
| 15 | PSF | Power-supply fail: undervoltage at pin VS detected |

After power-on reset, the input register has the following status:

| Bit 15 SI | Bit 14 OCS | Bit 13 OLD | Bit 12 PH3 | Bit 11 PL3 | Bit 10 PH2 | Bit 9 PL2 | Bit 8 PH1 | Bit 7 PL1 | Bit 6 HS3 | Bit 5 LS3 | Bit 4 HS2 | Bit 3 LS2 | Bit 2 HS1 | Bit 1 LS1 | Bit 0 SRR |
|--------------|---------------|---------------|---------------|---------------|---------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| H | H | H | L | L | L | L | L | L | L | L | L | L | L | L | L |

The following patterns are used to enable internal test modes of the IC. Do not use these patterns during normal operation.

| Bit 15 | Bit 14 | Bit 13 (OCS) | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 (HS3) | Bit 5 (LS3) | Bit 4 (HS2) | Bit 3 (LS2) | Bit 2 (HS1) | Bit 1 (LS1) | Bit 0 (SRR) |
|--------|--------|-----------------|--------|--------|--------|-------|-------|-------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| H | H | H | H | H | L | L | L | L | L | L | L | L | L | L | L |
| H | H | H | L | L | H | H | L | L | L | L | L | L | L | L | L |
| H | H | H | L | L | L | L | H | H | L | L | L | L | L | L | L |

3.2 Power-supply Fail

If undervoltage is detected at pin VS, the power-supply fail bit (PSF) in the output register is set and all outputs are disabled. To detect an undervoltage, its duration has to last longer than the undervoltage detection delay time t_{dUV} . The outputs are enabled immediately when the supply voltage returns to the normal operational value. The PSF bit stays high until it is reset by the SRR bit in the input register.

3.3 Open-load Detection

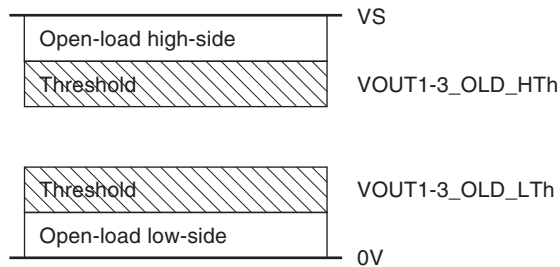
If the open-load detection bit (OLD) is set to low, a pull-up current for each high-side switch and a pull-down current for each low-side switch is turned on (open-load detection current I_{Out1-3}).

The open load condition of all the outputs is indicated in the SPI output register bit 1-6. High-side open load is detected in case of OUT1-3 voltage above maximum voltage $V_{OUT1-3_OLD_HTh}$ while Low-side open load is detected in case of OUT1-3 voltage below minimum voltage $V_{OUT1-3_OLD_LTh}$, see Figure 3-2.

If the OUTx is not connected, a Low-side open load is indicated, because the low-side current sink is higher than the high-side current source, see open load detection current ratio $I_{Out1-3L}/I_{Out1-3H}$.

Switching on an output stage with the OLD bit set to low disables the open-load function for this output.

Figure 3-2. OLD Threshold Level



3.4 Overtemperature Protection

If the junction temperature of one or more output stages exceeds the thermal prewarning threshold, $T_{jPW\ set}$, the temperature prewarning bit (TP) in the output register is set. When the temperature falls below the thermal prewarning threshold, $T_{jPW\ reset}$, the bit TP is reset. The TP bit can be read without transferring a complete 16-bit data word. The status of TP is available at pin DO with the falling edge of CS. After the microcontroller has read this information, CS is set high and the data transfer is interrupted without affecting the status of input and output registers.

If the junction temperature of an output stage exceeds the thermal shutdown threshold, $T_{jswitch\ off}$, the affected output is disabled and the corresponding bit in the output register is set to low. Additionally, the overload detection bit (OVL) in the output register is set. The output can be enabled again when the temperature falls below the thermal shutdown threshold, $T_{jswitch\ on}$, and the SRR bit in the input register is set to high. The hysteresis of thermal prewarning and shutdown threshold avoids oscillations.

3.5 Short-circuit Protection

The output currents are limited by a current regulator. Overcurrent detection is activated by writing a high to the overcurrent shutdown bit (OCS) bit in the input register. When the current in an output stage exceeds the overcurrent limitation and shutdown threshold, it is switched off, following a delay time (t_{dSd}). The over-load detection bit (OVL) is set and the corresponding status bit in the output register is set to low. For OCS = low, the overcurrent shutdown is inactive and the OVL bit is not set by an overcurrent. By writing a high to the SRR bit in the input register the OVL bit is reset and the disabled outputs are enabled.

3.6 Inhibit

The SI bit in the input register has to be set to zero to inhibit the Atmel® ATA6832C.

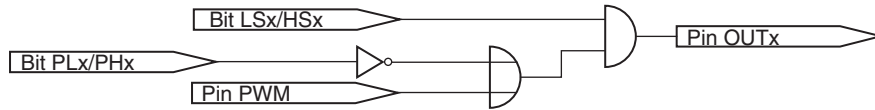
In this state, all output stages are then turned off but the serial interface remains active. The output stages can be reactivated by setting bit SI to “1”.

3.7 PWM Mode

The common input for all six outputs is pin PWM (Figure 3-3). The selection of the outputs, which are controlled by PWM, is done by input data register PLx or PHx. In addition to the PWM input register, the corresponding input registers HSx and LSs have to be set.

Switching the high side outputs is possible up to 25kHz, low side switches up to 8kHz.

Figure 3-3. Output Control by PWM



4. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| Parameters | Pin | Symbol | Value | Unit |
|--|------------|------------------------------------|--|------|
| Supply voltage | 10, 11 | V_{VS} | -0.3 to +40 | V |
| Supply voltage $t < 0.5s$; $I_{VS} > -2A$ | 10, 11 | V_{VS} | -1 | V |
| Logic supply voltage | 9 | V_{VCC} | -0.3 to +7 | V |
| Logic input voltage | 3, 4, 5, 6 | $V_{CS}, V_{DI}, V_{CLK}, V_{PWM}$ | -0.3 to $V_{VCC} + 0.3$ | V |
| Logic output voltage | 7 | V_{DO} | -0.3 to $V_{VCC} + 0.3$ | V |
| Input current | 3, 4, 5, 6 | $I_{CS}, I_{DI}, I_{CLK}, I_{PWM}$ | -10 to +10 | mA |
| Output current | 7 | I_{DO} | -10 to +10 | mA |
| Output current | 2, 12, 15 | $I_{Out1}, I_{Out2}, I_{Out3}$ | Internally limited, see output specification | |
| Output voltage | 2, 12, 15 | $I_{Out1}, I_{Out2}, I_{Out3}$ | -0.3 to +40 | V |
| Reverse conducting current ($t_{pulse} = 150\mu s$) | 2, 12, 15 | $I_{Out1}, I_{Out2}, I_{Out3}$ | 17 | A |
| Junction temperature range | | T_j | -40 to +200 | °C |
| Storage temperature range | | T_{STG} | -55 to +200 | °C |
| Ambient temperature range | | T_a | -40 to +150 | °C |

5. Thermal Resistance

| Parameters | Test Conditions | Symbol | Value | Unit |
|---|-------------------------|------------|-------|------|
| Thermal resistance from junction to case | | R_{thJC} | 5 | k/W |
| Thermal resistance from junction to ambient | Depends on the PC board | R_{thJA} | 40 | K/W |

6. Operating Range

| Parameters | Symbol | Value | Unit |
|----------------------------------|------------------------------------|----------------------|------|
| Supply voltage | V_{VS} | $V_{UV}^{(1)}$ to 40 | V |
| Logic supply voltage | V_{VCC} | 4.75 to 5.25 | V |
| Logic input voltage | $V_{CS}, V_{DI}, V_{CLK}, V_{PWM}$ | -0.3 to V_{VCC} | V |
| Serial interface clock frequency | f_{CLK} | 2 | MHz |
| PWM input frequency | f_{PWM} | max. 25 | kHz |
| Junction temperature range | T_j | -40 to +150 | °C |

Note: 1. Threshold for undervoltage description

7. Noise and Surge Immunity

| Parameters | Test Conditions | Value |
|---------------------------|-----------------|------------------------|
| Conducted interferences | ISO 7637-1 | Level 4 ⁽¹⁾ |
| Interference suppression | VDE 0879 Part 2 | Level 5 |
| ESD (Human Body Model) | ESD S 5.1 | 1.5kV |
| CDM (Charge Device Model) | ESD STM5.3.1 | 500V |

Note: 1. Test pulse 5: $V_{smax} = 40V$

8. Electrical Characteristics

$7.5V < V_{VS} < 40V$; $4.75V < V_{VCC} < 5.25V$; INH = High; $-40^{\circ}C \leq T_j \leq 200^{\circ}C$; $T_a \leq 150^{\circ}C$; unless otherwise specified, all values refer to GND pins.

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|---|-----------------------------------|--|--------|----------------------|------|------|------|-------------|-------|
| 1 Current Consumption | | | | | | | | | |
| 1.1 | Quiescent current VS | $V_{VS} < 20V$, SI = low | 10, 11 | I_{VS} | | 1 | 60 | μA | A |
| 1.2 | Quiescent current VCC | $4.75V < V_{VCC} < 5.25V$, SI = low | 9 | I_{VCC} | | 60 | 160 | μA | A |
| 1.3 | Supply current VS | $V_{VS} < 20V$ normal operating, all outputs off, input register bit 13 (OLD) = high | 10, 11 | I_{VS} | | 4 | 6 | mA | A |
| 1.4 | Supply current VCC | $4.75V < V_{VCC} < 5.25V$, normal operating | 9 | I_{VCC} | | 350 | 650 | μA | A |
| 1.5 | Discharge current VS | $V_{VS} = 32.5V$, INH = low | 10, 11 | I_{VS} | 0.5 | | 5.5 | mA | A |
| 1.6 | Discharge current VS | $V_{VS} = 40V$, INH = low | 10, 11 | I_{VS} | 2.0 | | 14 | mA | A |
| 2 Undervoltage Detection, Power-on Reset | | | | | | | | | |
| 2.1 | Power-on reset threshold | | 9 | V_{VCC} | 3.1 | 3.9 | 4.5 | V | A |
| 2.2 | Power-on reset delay time | After switching on V_{VCC} | | t_{dPor} | 30 | 95 | 190 | μs | A |
| 2.3 | Undervoltage-detection threshold | $V_{VCC} = 5V$ | 10, 11 | V_{UV} | 5.5 | | 7.1 | V | A |
| 2.4 | Undervoltage-detection hysteresis | $V_{VCC} = 5V$ | 10, 11 | ΔV_{UV} | | 0.6 | | V | A |
| 2.5 | Undervoltage-detection delay time | | | t_{dUV} | 10 | | 40 | μs | A |
| 3 Thermal Prewarning and Shutdown | | | | | | | | | |
| 3.1 | Thermal prewarning set | | | $T_{jPW\ set}$ | 170 | 195 | 220 | $^{\circ}C$ | B |
| 3.2 | Thermal prewarning reset | | | $T_{jPW\ reset}$ | 155 | 180 | 205 | $^{\circ}C$ | B |
| 3.3 | Thermal prewarning hysteresis | | | ΔT_{jPW} | | 15 | | K | B |
| 3.4 | Thermal shutdown off | | | $T_{j\ switch\ off}$ | 200 | 225 | 250 | $^{\circ}C$ | B |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

- Notes:
1. Delay time between rising edge of input signal at pin CS after data transmission and switch on/off output stages to 90% of final level. Device not in standby for $t > 1ms$.
 2. Delay time between rising/falling edge of input signal at pin PWM and switch on/off output stages to 90% of final level.
 3. Difference between switch-on and switch-off delay time of input signal at pin PWM to output stages in PWM mode.

8. Electrical Characteristics (Continued)

7.5V < V_{VS} < 40V; 4.75V < V_{VCC} < 5.25V; INH = High; -40°C ≤ T_j ≤ 200°C; T_a ≤ 150°C; unless otherwise specified, all values refer to GND pins.

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|----------|---|---|-----------|--|------------------------|------------------------|----------------------|------|-------|
| 3.5 | Thermal shutdown on | | | T _j switch on | 185 | 210 | 235 | °C | B |
| 3.6 | Thermal shutdown hysteresis | | | ΔT _j switch off | | 15 | | K | B |
| 3.7 | Ratio thermal shutdown off/thermal prewarning set | | | $\frac{T_{j\text{ switch off}}}{T_{j\text{ PW set}}}$ | 1.05 | 1.2 | | | B |
| 3.8 | Ratio thermal shutdown on/thermal prewarning reset | | | $\frac{T_{j\text{ switch on}}}{T_{j\text{ PW reset}}}$ | 1.05 | 1.2 | | | B |
| 4 | Output Specification (OUT1 to OUT3) | | | | | | | | |
| 4.1 | On resistance | I _{Out 1-3} = -0.9A | 2, 12, 15 | R _{DSon1-3H} | | | 1.8 | Ω | A |
| 4.2 | | I _{Out 1-3} = -0.9A | 2, 12, 15 | R _{DSon1-3L} | | | 1.8 | Ω | A |
| 4.3 | High-side output leakage current | V _{Out 1-3 H} = 0V, output stages off | 2, 12, 15 | I _{Out1-3H} | -60 | | | μA | A |
| 4.4 | Low-side output leakage current | V _{Out 1-3 L} = V _{VS} , output stages off | 2, 12, 15 | I _{Out1-3L} | | | 300 | μA | A |
| 4.5 | High-side switch reverse diode forward voltage | I _{Out} = 1.5A | 2, 12, 15 | V _{Out1-3} - V _{VS} | | | 2 | V | A |
| 4.6 | Low-side switch reverse diode forward voltage | I _{Out 1-3 L} = -1.5A | 2, 12, 15 | V _{Out1-3L} | 2 | | | V | A |
| 4.7 | High-side overcurrent limitation and shutdown threshold | 7.5V < V _{VS} < 20V | 2, 12, 15 | I _{Out1-3} | 1.0 | 1.3 | 1.8 | A | A |
| 4.8 | Low-side overcurrent limitation and shutdown threshold | 7.5V < V _{VS} < 20V | 2, 12, 15 | I _{Out1-3} | -1.8 | -1.3 | -1.0 | A | A |
| 4.9 | High-side overcurrent limitation and shutdown threshold | 20V < V _{VS} < 40V | 2, 12, 15 | I _{Out1-3} | 1.0 | 1.3 | 2.0 | A | A |
| 4.10 | Low-side overcurrent limitation and shutdown threshold | 20V < V _{VS} < 40V | 2, 12, 15 | I _{Out1-3} | -2.0 | -1.3 | -1.0 | A | A |
| 4.11 | Overcurrent shutdown delay time | | | t _{dSd} | 10 | | 40 | μs | A |
| 4.12 | High-side open load detection current | Input register bit 13 (OLD) = low, output off V _{VS} = 13V, V _{Out 1-3} = 0V | 2, 12, 15 | I _{Out1-3H} | 1 | 2.5 | 4 | mA | A |
| 4.12a | High-side open load detection threshold level | Input register bit 13 (OLD) = low, output off V _{VS} = 13V, I _{Out1-3} = 0mA | 2, 12, 15 | V _{Out1-3_OLD_HTh} | V _{VS} - 3.5V | V _{VS} - 2.5V | V _{VS} - 1V | V | A |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

- Notes:
1. Delay time between rising edge of input signal at pin CS after data transmission and switch on/off output stages to 90% of final level. Device not in standby for t > 1ms.
 2. Delay time between rising/falling edge of input signal at pin PWM and switch on/off output stages to 90% of final level.
 3. Difference between switch-on and switch-off delay time of input signal at pin PWM to output stages in PWM mode.

8. Electrical Characteristics (Continued)

7.5V < V_{VS} < 40V; 4.75V < V_{VCC} < 5.25V; INH = High; -40°C ≤ T_j ≤ 200°C; T_a ≤ 150°C; unless otherwise specified, all values refer to GND pins.

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|----------|---|--|------------|---|------------------------|------|------------------------|------|-------|
| 4.13 | Low-side open load detection current | Input register bit 13 (OLD) = low, output off V _{VS} = 13V, V _{Out 1-3} = 13V | 2, 12, 15 | I _{Out1-3L} | -6 | -9 | -11 | mA | A |
| 4.13a | Low-side open load detection threshold level | Input register bit 13 (OLD) = low, output off V _{VS} = 13V, I _{Out1-3} = 0mA | 2, 12, 15 | V _{Out1-3_OLd_LTh} | 0.5 | 1.5 | 2.5 | V | A |
| 4.14 | Open load detection current ratio | | | I _{Out1-3L} /I _{Out1-3H} | 2 | 3 | 4 | | |
| 4.15 | High-side output switch on delay ^{(1),(2)} | V _{VS} = 13V R _{Load} = 30Ω | | t _{don} | | | 20 | μs | A |
| 4.16 | Low-side output switch on delay ^{(1),(2)} | V _{VS} = 13V R _{Load} = 30Ω | | t _{don} | | | 20 | μs | A |
| 4.17 | High-side output switch off delay ^{(1),(2)} | V _{VS} = 13V R _{Load} = 30Ω | | t _{doff} | | | 20 | μs | A |
| 4.18 | Low-side output switch off delay ^{(1),(2)} | V _{VS} = 13V R _{Load} = 30Ω | | t _{doff} | | | 3 | μs | A |
| 4.19 | Dead time between corresponding high-side and low-side switches | V _{VS} = 13V R _{Load} = 30Ω | | t _{don} - t _{doff} | 1 | | | μs | A |
| 4.20 | Δt _{dPWM} low-side switch ⁽³⁾ | V _{VS} = 13V R _{Load} = 30Ω | | Δt _{dPWM} = t _{don} - t _{doff} | | | 20 | μs | A |
| 4.21 | Δt _{dPWM} high-side switch ⁽³⁾ | V _{VS} = 13V R _{Load} = 30Ω | | Δt _{dPWM} = t _{don} - t _{doff} | -5 | | 5 | μs | A |
| 5 | Logic Inputs DI, CLK, CS, PWM | | | | | | | | |
| 5.1 | Input voltage low-level threshold | | 3, 4, 5, 6 | V _{IL} | 0.3 × V _{VCC} | | | V | A |
| 5.2 | Input voltage high-level threshold | | 3, 4, 5, 6 | V _{IH} | | | 0.7 × V _{VCC} | V | A |
| 5.3 | Hysteresis of input voltage | | 3, 4, 5, 6 | ΔV _I | 50 | | 700 | mV | A |
| 5.4 | Pull-down current pins DI, CLK, PWM | V _{DI} , V _{CLK} , V _{PWM} = V _{VCC} | 4, 5, 6 | I _{PD} | 5 | | 70 | μA | A |
| 5.5 | Pull-up current pin CS | V _{CS} = 0V | 3 | I _{PU} | -70 | | -5 | μA | A |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

- Notes:
1. Delay time between rising edge of input signal at pin CS after data transmission and switch on/off output stages to 90% of final level. Device not in standby for t > 1ms.
 2. Delay time between rising/falling edge of input signal at pin PWM and switch on/off output stages to 90% of final level.
 3. Difference between switch-on and switch-off delay time of input signal at pin PWM to output stages in PWM mode.

8. Electrical Characteristics (Continued)

7.5V < V_{VS} < 40V; 4.75V < V_{VCC} < 5.25V; INH = High; -40°C ≤ T_j ≤ 200°C; T_a ≤ 150°C; unless otherwise specified, all values refer to GND pins.

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|---|---|---|-----|-------------------|-------------------------|------|------|------|-------|
| 6 Serial Interface – Logic Output DO | | | | | | | | | |
| 6.1 | Output-voltage low level | I _{DO} L = 2mA | 7 | V _{DO} L | | | 0.4 | V | A |
| 6.2 | Output-voltage high level | I _{DO} L = -2mA | 7 | V _{DO} H | V _{VCC} - 0.7V | | | V | A |
| 6.3 | Leakage current (tri-state) | V _{CS} = V _{VCC} 0V < V _{DO} < V _{VCC} | 7 | I _{DO} | -15 | | +15 | μA | A |
| 7 Inhibit Input – Timing | | | | | | | | | |
| 7.1 | Delay time from standby to normal operation | | | t _{dINH} | | | 100 | μs | A |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

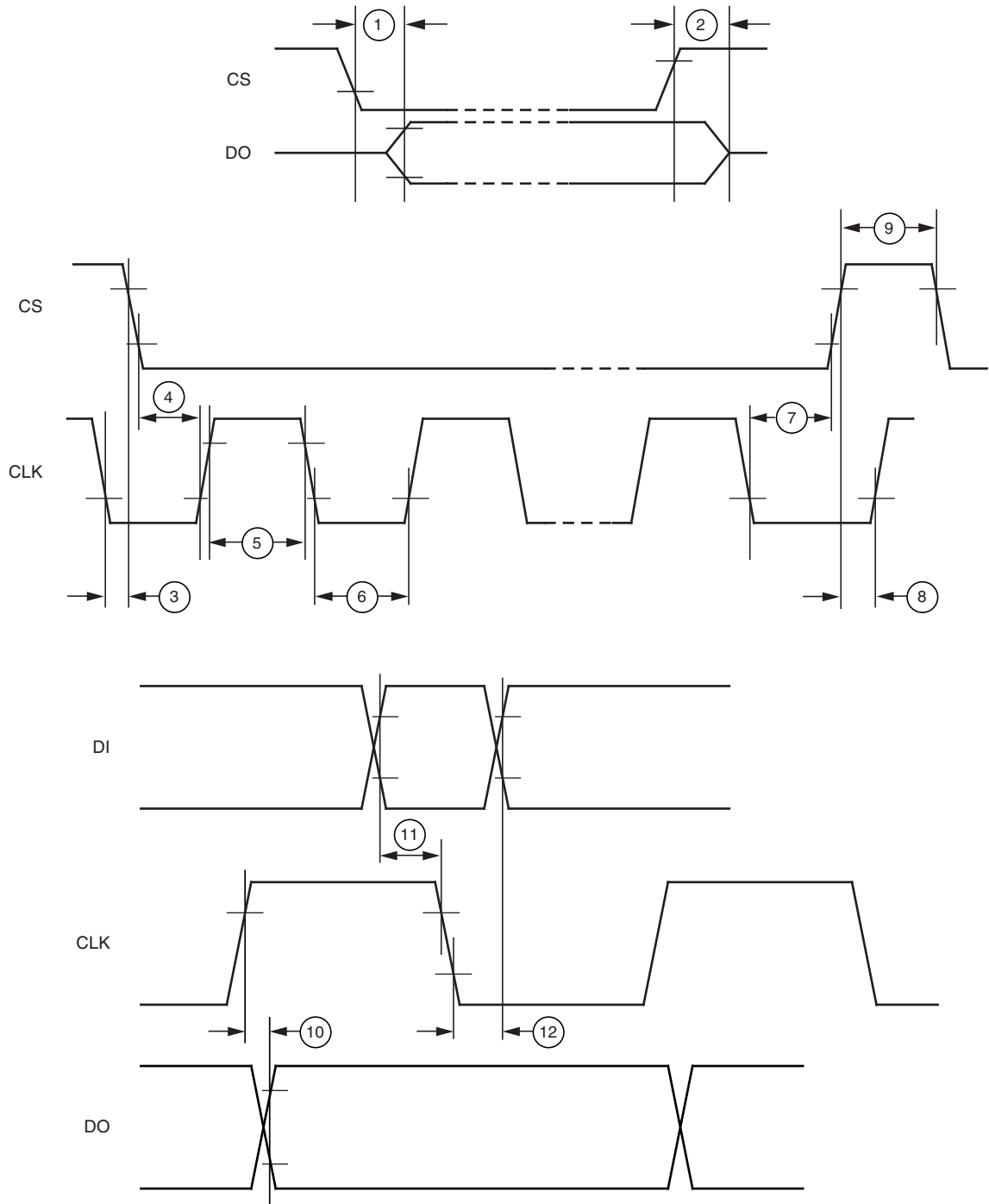
- Notes:
1. Delay time between rising edge of input signal at pin CS after data transmission and switch on/off output stages to 90% of final level. Device not in standby for t > 1ms.
 2. Delay time between rising/falling edge of input signal at pin PWM and switch on/off output stages to 90% of final level.
 3. Difference between switch-on and switch-off delay time of input signal at pin PWM to output stages in PWM mode.

9. Serial Interface Timing

| No. | Parameters | Test Conditions | Pin | Timing Chart No. ⁽¹⁾ | Symbol | Min. | Typ. | Max. | Unit | Type* |
|----------------------------------|---------------------------------|-------------------------|-----|---------------------------------|------------------------|------|------|------|------|-------|
| 8 Serial Interface Timing | | | | | | | | | | |
| 8.1 | DO enable after CS falling edge | C _{DO} = 100pF | 7 | 1 | t _{ENDO} | | | 200 | ns | D |
| 8.2 | DO disable after CS rising edge | C _{DO} = 100pF | 7 | 2 | t _{DISDO} | | | 200 | ns | D |
| 8.3 | DO fall time | C _{DO} = 100pF | 7 | - | t _{DO} f | | | 100 | ns | D |
| 8.4 | DO rise time | C _{DO} = 100pF | 7 | - | t _{DO} r | | | 100 | ns | D |
| 8.5 | DO valid time | C _{DO} = 100pF | 7 | 10 | t _{DO} val | | | 200 | ns | D |
| 8.6 | CS setup time | | 3 | 4 | t _{CS} SetHl | 225 | | | ns | D |
| 8.7 | CS setup time | | 3 | 8 | t _{CS} SetHh | 225 | | | ns | D |
| 8.8 | CS high time | | 3 | 9 | t _{CS} h | 500 | | | ns | D |
| 8.9 | CLK high time | | 5 | 5 | t _{CLK} h | 225 | | | ns | D |
| 8.10 | CLK low time | | 5 | 6 | t _{CLK} l | 225 | | | ns | D |
| 8.11 | CLK period time | | 5 | - | t _{CLK} p | 500 | | | ns | D |
| 8.12 | CLK setup time | | 5 | 7 | t _{CLK} SetHl | 225 | | | ns | D |
| 8.13 | CLK setup time | | 5 | 3 | t _{CLK} SetHh | 225 | | | ns | D |
| 8.14 | DI setup time | | 4 | 11 | t _{DI} set | 40 | | | ns | D |
| 8.15 | DI hold time | | 4 | 12 | t _{DI} Hold | 40 | | | ns | D |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

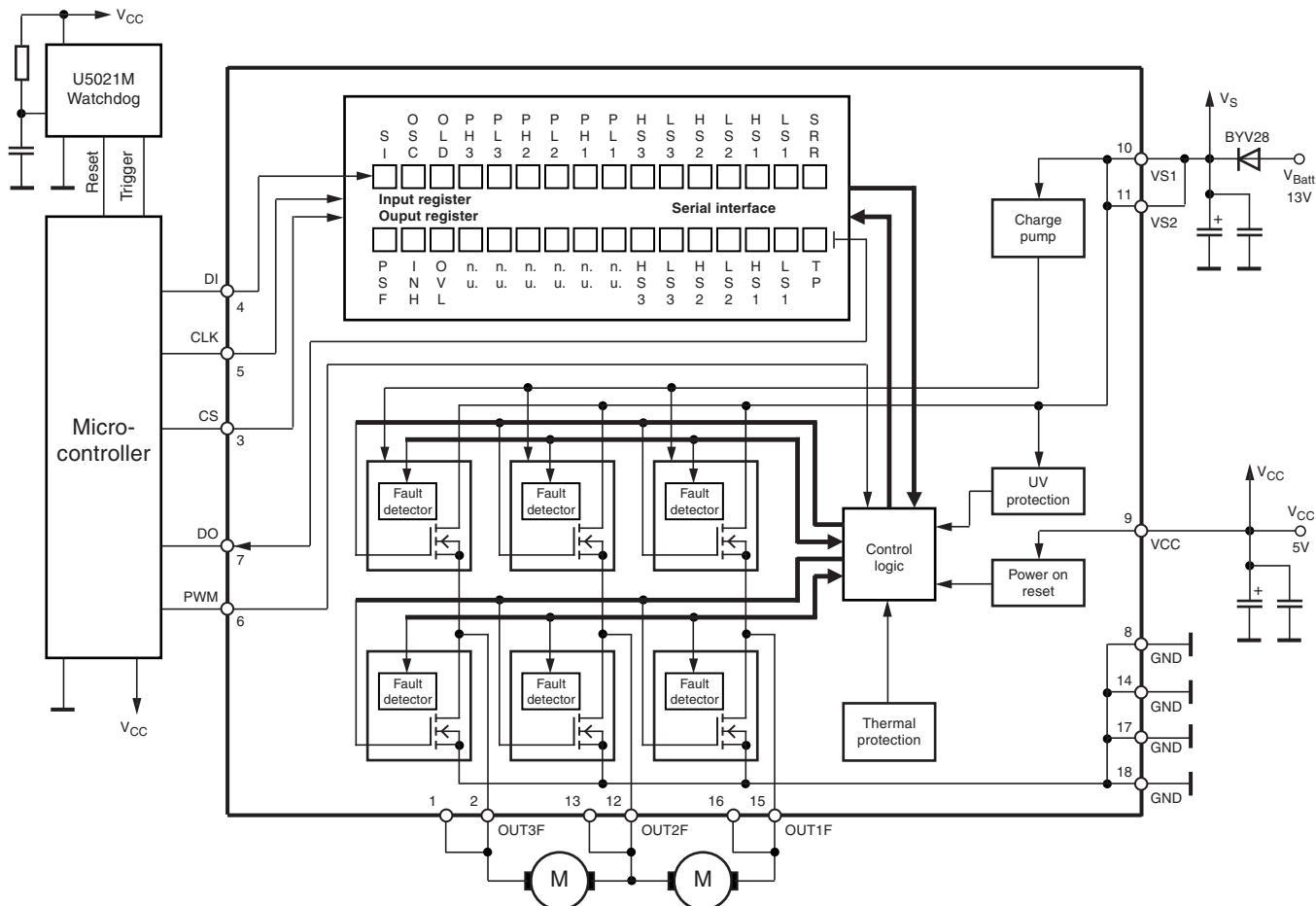
Figure 9-1. Serial Interface Timing with Chart Number



Inputs DI, CLK, CS: High level = $0.7 \times V_{CC}$, low level = $0.3 \times V_{CC}$
 Output DO: High level = $0.8 \times V_{CC}$, low level = $0.2 \times V_{CC}$

10. Application Circuit

Figure 10-1. Application Circuit



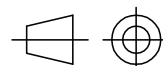
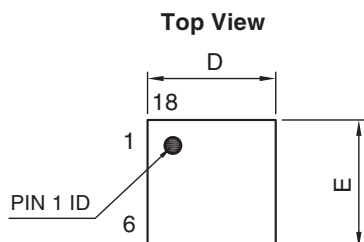
10.1 Application Notes

- Connect the blocking capacitors at V_{VCC} and V_{VS} as close as possible to the power supply and GND pins.
- Recommended value for capacitors at V_{VS} :
 - Electrolytic capacitor $C > 22\mu\text{F}$ in parallel with a ceramic capacitor $C = 100\text{nF}$. The value for the electrolytic capacitor depends on external loads, conducted interferences, and the reverse conducting current $I_{\text{Out}1,2,3}$.
- Recommended value for capacitors at V_{VCC} :
 - Electrolytic capacitor $C > 10\mu\text{F}$ in parallel with a ceramic capacitor $C = 100\text{nF}$.
- To reduce thermal resistance, place cooling areas on the PCB as close as possible to the GND pins and to the die pad.

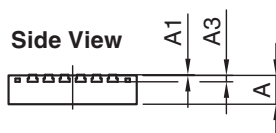
11. Ordering Information

| Extended Type Number | Package | Remarks |
|----------------------|------------------|---------------------------|
| ATA6832C-PIQW | QFN18, 4mm × 4mm | Taped and reeled, Pb-free |

12. Package Information

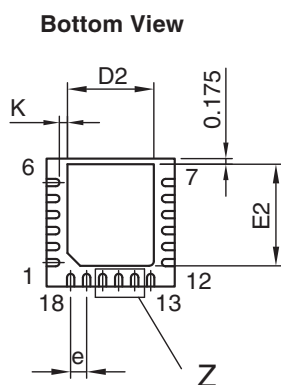


technical drawings
according to DIN
specifications

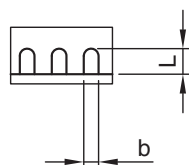


Dimensions in mm

Not indicated tolerances ± 0.05



Z 10:1



| COMMON DIMENSIONS | | | | |
|------------------------|-------|---------|-------|------|
| (Unit of Measure = mm) | | | | |
| Symbol | MIN | NOM | MAX | NOTE |
| A | 0.8 | 0.9 | 1 | |
| A1 | 0.0 | 0.02 | 0.05 | |
| A3 | 0.15 | 0.2 | 0.25 | |
| D | 3.95 | 4 | 4.05 | |
| D2 | 2.65 | 2.7 | 2.75 | |
| E | 3.95 | 4 | 4.05 | |
| E2 | 3.125 | 3.175 | 3.225 | |
| L | 0.3 | 0.4 | 0.5 | |
| K | 0.2 | 0.25 | 0.3 | |
| b | 0.16 | 0.23 | 0.3 | |
| e | | 0.5 BSC | | |

05/20/11



Package Drawing Contact:
packagedrawings@atmel.com

TITLE
Package: VQFN_4x4_18L
Exposed pad 2.7x3.175

DRAWING NO.
6.543-5133.01-4

REV.
3

13. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

| Revision No. | History |
|------------------|--|
| 9216C-AUTO-02/12 | <ul style="list-style-type: none">• Section 8 “Electrical Characteristics” number 4.7 and 4.8 on page 10 changed |
| 9216B-AUTO-06/11 | <ul style="list-style-type: none">• Package Information: drawing changed |



Enabling Unlimited Possibilities™

Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131
USA

Tel: (+1) (408) 441-0311

Fax: (+1) (408) 487-2600

www.atmel.com

Atmel Asia Limited

Unit 01-5 & 16, 19F
BEA Tower, Millennium City 5
418 Kwun Tong Roa
Kwun Tong, Kowloon

HONG KONG

Tel: (+852) 2245-6100

Fax: (+852) 2722-1369

Atmel Munich GmbH

Business Campus
Parkring 4
D-85748 Garching b. Munich
GERMANY

Tel: (+49) 89-31970-0

Fax: (+49) 89-3194621

Atmel Japan G.K.

16F Shin-Osaki Kangyo Building
1-6-4 Osaki
Shinagawa-ku, Tokyo 141-0032
JAPAN

Tel: (+81) (3) 6417-0300

Fax: (+81) (3) 6417-0370

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