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High Temperature Hex Half-bridge Driver with Serial Input Control

DATASHEET

Features

- Six half-bridge outputs formed by six high-side and six low-side drivers
- Capable of switching all kinds of loads (such as DC motors, bulbs, resistors, capacitors and inductors)
- R_{DSon} typically 1.0Ω at 25°C , maximum 2.2Ω at 200°C
- Up to 650-mA output current
- Very low quiescent current $I_S < 20\mu\text{A}$ in Standby Mode
- Outputs short-circuit protected
- Overtemperature prewarning and protection
- Undervoltage protection
- Various diagnosis functions such as shorted output, open load, overtemperature and power supply fail
- Serial data interface
- Operation voltage up to 40V
- Daisy chaining possible
- Serial interface 5V compatible, up to 2MHz clock frequency
- QFN24 package

1. Description

The Atmel® ATA6837 is designed for high-temperature applications. In mechatronic solutions, for example, turbo charger or exhaust gas recirculation systems, many flaps have to be controlled by DC motor driver ICs which are located very close to the hot engine or actuator and where ambient temperatures up to 150°C are usual. Due to the advantages of SOI technology, junction temperatures up to 200°C are allowed. This enables new cost-effective board design possibilities to achieve complex mechatronic solutions.

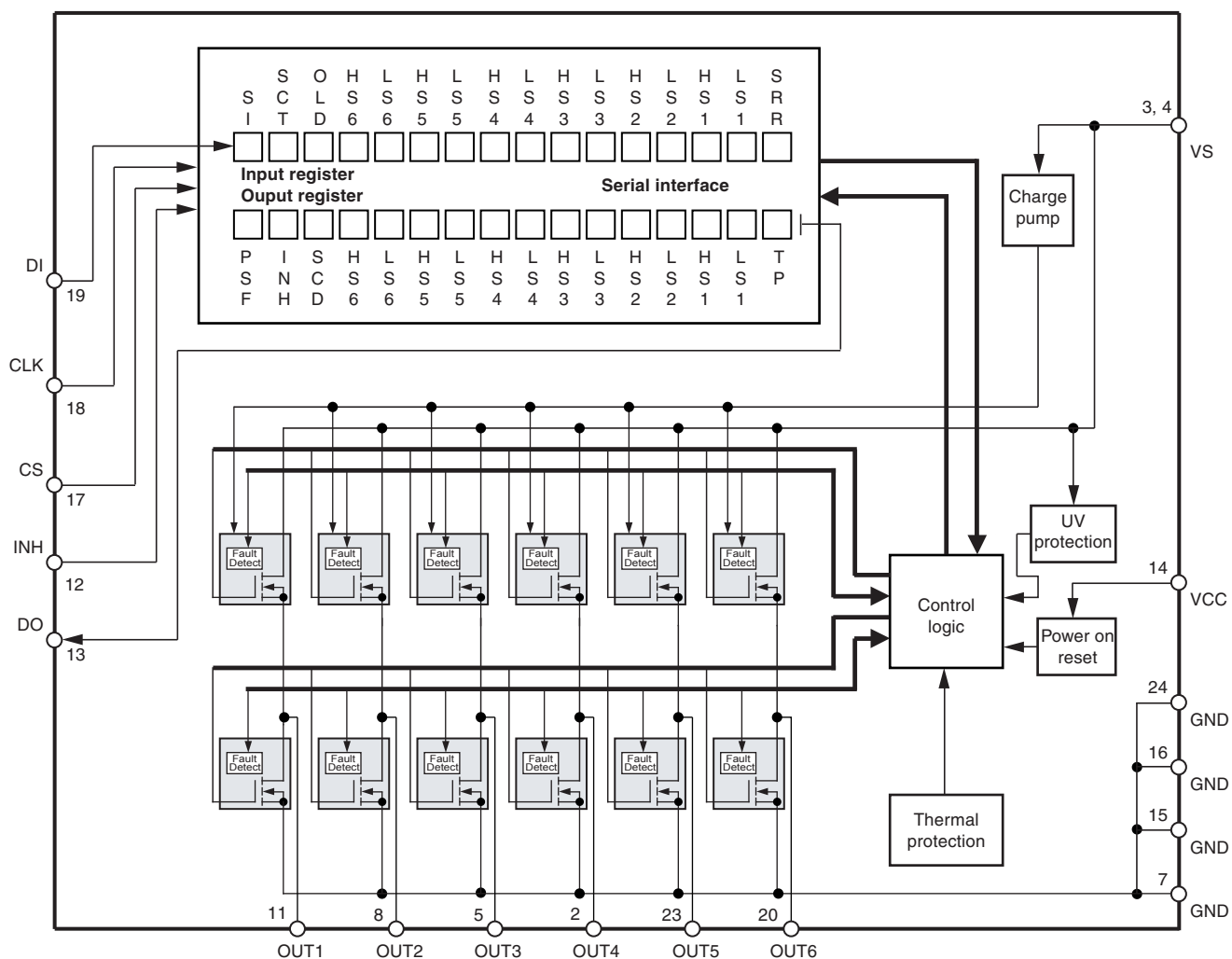
The Atmel ATA6837 is a fully protected hex half-bridge driver, used to control up to 6 different loads by a microcontroller in automotive and industrial applications.

Each of the six high-side and six low-side drivers is capable of driving currents up to 650mA. The drivers are internally connected to form 6 half-bridges and can be controlled separately from a standard serial data interface. Therefore, all kinds of loads, such as bulbs, resistors, capacitors and inductors, can be combined. The IC especially supports the application of H-bridges to drive DC motors.

Protection is guaranteed in terms of short-circuit conditions, overtemperature and undervoltage. Various diagnosis functions and a very low quiescent current in standby mode make a wide range of applications possible.

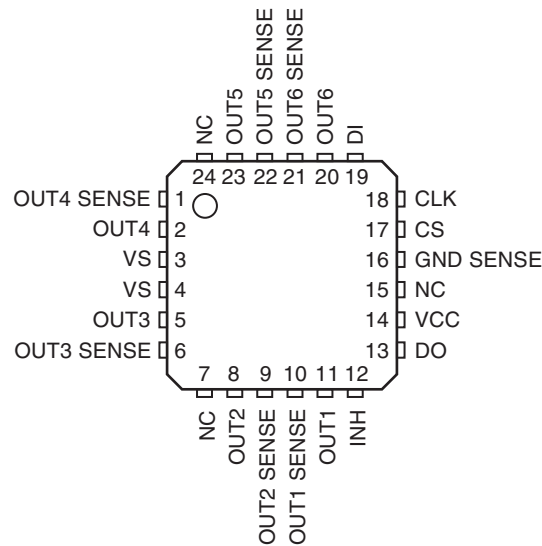
Automotive qualification referring to conducted interferences, EMC protection and ESD protection gives added value and enhanced quality for the exacting requirements of automotive applications.

Figure 1-1. Block Diagram QFN24



2. Pin Configuration

Figure 2-1. Pinning QFN 24, 5 × 5, 0.65mm Pitch



Note: YWW Date code (Y = Year above 2000, WW = week number)
 ATAxzy Product name
 ZZZZZ Wafer lot number
 AL Assembly sub-lot number

Table 2-1. Pin Description QFN24

| Pin | Symbol | Function |
|-----|------------|---|
| 1 | OUT4 SENSE | Only for testability in final test |
| 2 | OUT4 | Half-bridge output 4; formed by internally connected power MOS high-side switch 4 and low-side switch 4 with internal reverse diodes; short circuit protection; overtemperature protection; diagnosis for short and open load |
| 3 | VS | Power supply output stages HS4, HS5 and HS6 |
| 4 | VS | Power supply output stages HS1, HS2 and HS3 |
| 5 | OUT3 | Output 3; see pin 1 |
| 6 | OUT3 SENSE | Only for testability in final test |
| 7 | NC | Internal bond to GND |
| 8 | OUT2 | Output 2; see pin 1 |
| 9 | OUT2 SENSE | Only for testability in final test |
| 10 | OUT1 SENSE | Only for testability in final test |
| 11 | OUT1 | Output 1; see pin 1 |
| 12 | INH | Inhibit input; 5V logic input with internal pull down; low = standby, high = normal operation |
| 13 | DO | Serial data output; 5V CMOS logic level tri-state output for output (status) register data; sends 16-bit status information to the microcontroller (LSB is transferred first). Output will remain tri-stated unless device is selected by CS = low, therefore, several ICs can operate on one data output line only |
| 14 | VCC | Logic supply voltage (5V) |
| 15 | NC | Internal bond to GND |
| 16 | GND SENSE | Ground; reference potential; internal connection to the lead frame; cooling tab |

Table 2-1. Pin Description QFN24 (Continued)

| Pin | Symbol | Function |
|-----|------------|---|
| 17 | CS | Chip select input; 5V CMOS logic level input with internal pull up; low = serial communication is enabled, high = disabled |
| 18 | CLK | Serial clock input; 5V CMOS logic level input with internal pull down; controls serial data input interface and internal shift register ($f_{max} = 2\text{MHz}$) |
| 19 | DI | Serial data input; 5V CMOS logic level input with internal pull down; receives serial data from the control device; DI expects a 16-bit control word with LSB being transferred first |
| 20 | OUT6 | Output 6; see pin 1 |
| 21 | OUT6 SENSE | Only for testability in final test |
| 22 | OUT5 SENSE | Only for testability in final test |
| 23 | OUT5 | Output 5; see pin 1 |
| 24 | NC | Internal bond to GND |

3. Functional Description

3.1 Serial Interface

Data transfer starts with the falling edge of the CS signal. Data must appear at DI synchronized to CLK and is accepted on the falling edge of the CLK signal. LSB (bit 0, SRR) has to be transferred first. Execution of new input data is enabled on the rising edge of the CS signal. When CS is high, pin DO is in a tri-state condition. This output is enabled on the falling edge of CS. Output data will change their state with the rising edge of CLK and stay stable until the next rising edge of CLK appears. LSB (bit 0, TP) is transferred first.

Figure 3-1. Data Transfer Input Data Protocol

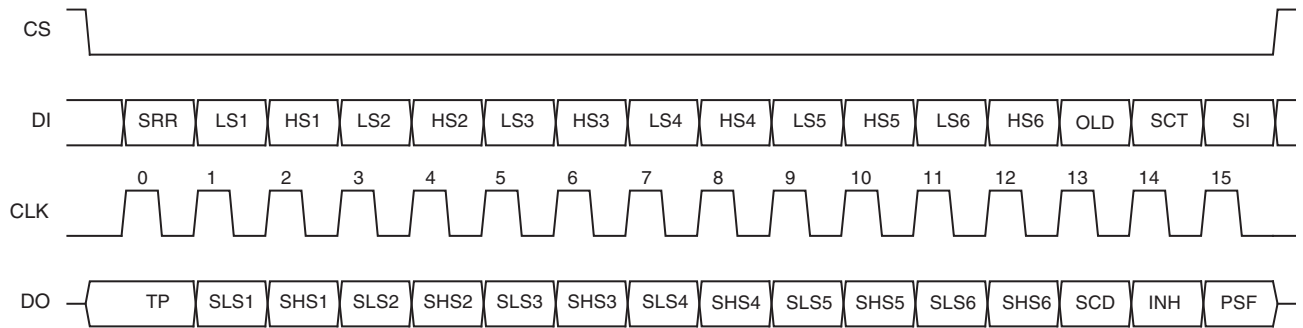


Table 3-1. Input Data Protocol

| Bit | Input Register | Function |
|-----|----------------|--|
| 0 | SRR | Status register reset (high = reset; the bits PSF, SCD and overtemperature shutdown in the output data register are set to low) |
| 1 | LS1 | Controls output LS1 (high = switch output LS1 on) |
| 2 | HS1 | Controls output HS1 (high = switch output HS1 on) |
| 3 | LS2 | See LS1 |
| 4 | HS2 | See HS1 |
| 5 | LS3 | See LS1 |
| 6 | HS3 | See HS1 |
| 7 | LS4 | See LS1 |
| 8 | HS4 | See HS1 |
| 9 | LS5 | See LS1 |
| 10 | HS5 | See HS1 |
| 11 | LS6 | See LS1 |
| 12 | HS6 | See HS1 |
| 13 | OLD | Open load detection (low = on) |
| 14 | SCT | Programmable time delay for short circuit (shutdown delay high/low = 12ms/1.5ms) |
| 15 | SI | Software inhibit; low = standby, high = normal operation (data transfer is not affected by standby function because the digital part is still powered) |

Table 3-2. Output Data Protocol

| Bit | Output (Status) Register | Function |
|-----|--------------------------|---|
| 0 | TP | Temperature prewarning: high = warning (overtemperature shutdown see remark below) |
| 1 | Status LS1 | Normal operation: high = output is on, low = output is off Open-load detection: high = open load, low = no open load (correct load condition is detected if the corresponding output is switched off) |
| 2 | Status HS1 | Normal operation: high = output is on, low = output is off Open-load detection: high = open load, low = no open load (correct load condition is detected if the corresponding output is switched off) |
| 3 | Status LS2 | Description see LS1 |
| 4 | Status HS2 | Description see HS1 |
| 5 | Status LS3 | Description see LS1 |
| 6 | Status HS3 | Description see HS1 |
| 7 | Status LS4 | Description see LS1 |
| 8 | Status HS4 | Description see HS1 |
| 9 | Status LS5 | Description see LS1 |
| 10 | Status HS5 | Description see HS1 |
| 11 | Status LS6 | Description see LS1 |
| 12 | Status HS6 | Description see HS1 |
| 13 | SCD | Short circuit detected: set high, when at least one output is switched off by a short circuit condition |
| 14 | INH | Inhibit: this bit is controlled by software (bit SI in input register) and hardware inhibit (pin INH). High = standby, low = normal operation |
| 15 | PSF | Power supply fail: undervoltage at pin VS detected |

Note: Bit 0 to 15 = high: overtemperature shutdown

Table 3-3. Status of the Input Register After Power on Reset

| Bit 15 (SI) | Bit 14 (SCT) | Bit 13 (OLD) | Bit 12 (HS6) | Bit 11 (LS6) | Bit 10 (HS5) | Bit 9 (LS5) | Bit 8 (HS4) | Bit 7 (LS4) | Bit 6 (HS3) | Bit 5 (LS3) | Bit 4 (HS2) | Bit 3 (LS2) | Bit 2 (HS1) | Bit 1 (LS1) | Bit 0 (SRR) |
|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| H | H | H | L | L | L | L | L | L | L | L | L | L | L | L | L |

3.2 Power-supply Fail

In case of undervoltage at pin VS, an internal timer is started. When during a permanent undervoltage the delay time (t_{dUV}) is reached, the power supply fail bit (PSF) in the output register is set and all outputs are disabled. When normal voltage is present again, the outputs are enabled immediately. The PSF bit remains high until it is reset by the SRR bit in the input register.

3.3 Open-load Detection

If the open-load detection bit (OLD) is set to low, a pull-up current for each high-side switch and a pull-down current for each low-side switch is turned on (open-load detection current I_{HS1-6} , I_{LS1-6}). If $V_{VS} - V_{HS1-6}$ or V_{LS1-6} is lower than the open-load detection threshold (open-load condition), the corresponding bit of the output in the output register is set to high. Switching on an output stage with OLD bit set to low disables the open load function for this output.

3.4 Overtemperature Protection

If the junction temperature exceeds the thermal prewarning threshold, T_{jPW} set, the temperature prewarning bit (TP) in the output register is set. When the temperature falls below the thermal prewarning threshold, T_{jPW} reset, the bit TP is reset. The TP bit can be read without transferring a complete 16-bit data word: with CS = high to low, the state of TP appears at pin DO. After the microcontroller has read this information, CS is set high and the data transfer is interrupted without affecting the state of the input and output registers.

If the junction temperature exceeds the thermal shutdown threshold, $T_{j\text{switch off}}$, the outputs are disabled and all bits in the output register are set high. The outputs can be enabled again when the temperature falls below the thermal shutdown threshold, $T_{j\text{switch on}}$, and when a high has been written to the SRR bit in the input register. Thermal prewarning and shutdown threshold have hysteresis.

3.5 Short-circuit Protection

The output currents are limited by a current regulator. Current limitation takes place when the overcurrent limitation and shutdown threshold (I_{HS1-6} , I_{LS1-6}) are reached. Simultaneously, an internal timer is started. The shorted output is disabled when during a permanent short the delay time (t_{dSd}) programmed by the short-circuit timer bit (SCT) is reached. Additionally, the short-circuit detection bit (SCD) is set. If the temperature prewarning bit TP in the output register is set during a short, the shorted output is disabled after t_{dSd} and SCD bit is set. By writing a high to the SRR bit in the input register, the SCD bit is reset and the disabled outputs are enabled.

3.6 Inhibit

There are two ways to inhibit the Atmel® ATA6837:

- Set bit SI in the input register to 0
- Switch pin INH to 0V

In both cases, all output stages are turned off but the serial interface stays active. The output stages can be activated again by bit SI = 1 (when INH = VCC) or by pin INH switched back to VCC (when SI = 1).

4. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

All values refer to GND pins.

| Parameters | Pin | Symbol | Value | Unit |
|--|---------------------|------------------------------------|--|------|
| Supply voltage | 3, 4 | V_{VS} | -0.3 to +40 | V |
| Supply voltage $t < 0.5s$; $I_S > -2A$ | 3, 4 | V_{VS} | -1 | V |
| Supply voltage difference $ V_{S_pin3} - V_{S_pin4} $ | 3, 4 | ΔV_{VS} | 150 | mV |
| Logic supply voltage | 14 | V_{VCC} | -0.3 to +7 | V |
| Logic input voltage | 17 - 19 | V_{DI}, V_{CLK}, V_{CS} | -0.3 to $V_{VCC} + 0.3$ | V |
| Logic output voltage | 13 | V_{DO} | -0.3 to $V_{VCC} + 0.3$ | V |
| Input current | 12, 17 - 19 | $I_{INH}, I_{DI}, I_{CLK}, I_{CS}$ | -10 to +10 | mA |
| Output current | 13 | I_{DO} | -10 to +10 | mA |
| Output current | 2, 5, 8, 11, 20, 23 | I_{OUT1} to I_{OUT6} | Internally limited, see “Output Specification” in Section 7. on page 9 | |
| Junction temperature range | | T_j | -40 to +200 | °C |
| Storage temperature range | | T_{STG} | -55 to +200 | °C |
| Ambient temperature range | | T_a | -40 to +150 | °C |

5. Thermal Resistance

Table 5-1. QFN24: Depends on the PCB-board

| Parameter | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit |
|------------------|-----------------|-----|------------|------|------|------|------|
| Junction pin | | 16 | R_{thJP} | | | < 5 | K/W |
| Junction ambient | | | R_{thJA} | | | 35 | K/W |

6. Operating Range

| Parameter | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit |
|----------------------------------|-----------------|-------------|------------------------------------|----------------|------|-----------|------|
| Supply voltage | | 3, 4 | V_{VS} | $V_{UV}^{(1)}$ | | 40 | V |
| Logic supply voltage | | 14 | V_{VCC} | 4.75 | | 5.25 | V |
| Logic input voltage | | 12, 17 - 19 | $V_{INH}, V_{DI}, V_{CLK}, V_{CS}$ | -0.3 | | V_{VCC} | V |
| Serial interface clock frequency | | | f_{CLK} | | | 2 | MHz |
| Junction temperature range | | | T_j | -40 | | +200 | °C |

7. Electrical Characteristics

7.5V < V_S < 40V; 4.75V < V_{CC} < 5.25V; INH = High; -40°C < T_j < 200°C, T_a ≤ 150°C; unless otherwise specified, all values refer to GND pins.

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|---|--|--|------|---------------------------|------|------|------|------|-------|
| 1 Current Consumption | | | | | | | | | |
| 1.1 | Total quiescent current (V _S and all outputs to VS) | V _S = 33V V _{CC} = 0V or V _{CC} = 5V, bit SI = low or V _{CC} = 5V, pin INH = low Output pins to VS and GND | 3, 4 | I _{VS} | | | 20 | μA | A |
| 1.2 | Quiescent current (VCC) | 4.75V < V _{VCC} < 5.25V, INH or bit SI = low | 14 | I _{VCC} | | | 40 | μA | A |
| 1.3 | Supply current (VS) | V _{VS} < 28V normal operation, all output stages off | 3, 4 | I _{VS} | | 0.8 | 1.2 | mA | A |
| 1.4 | Supply current (VS) | V _{VS} < 28V normal operation, all output low stages on, no load | 3, 4 | I _{VS} | | | 10 | mA | A |
| 1.5 | Supply current (VS) | V _{VS} < 28V normal operation, all output high stages on, no load | 3, 4 | I _{VS} | | | 16 | mA | A |
| 1.6 | Supply current (VCC) | 4.75V < V _{VCC} < 5.25V, normal operation | 14 | I _{VCC} | | | 200 | μA | A |
| 1.7 | Discharge current (VS) | V _{VS} = 40V, INH = low | 3, 4 | I _{VS} | | | 5 | mA | A |
| 2 Internal Oscillator Frequency | | | | | | | | | |
| 2.1 | Frequency (time base for delay timers) | | | f _{OSC} | 19 | | 45 | kHz | A |
| 3 Undervoltage Detection, Power-on Reset | | | | | | | | | |
| 3.1 | Power-on reset threshold | | 14 | V _{VCC} | 2.3 | 2.7 | 3.0 | V | A |
| 3.2 | Power-on reset delay time | After switching on V _{VCC} | | t _{dPor} | 20 | 95 | 180 | μs | A |
| 3.3 | Undervoltage detection threshold | | 14 | V _{UV} | 5.5 | | 7.0 | V | A |
| 3.4 | Undervoltage detection hysteresis | | 14 | ΔV _{UV} | | 0.4 | | V | A |
| 3.5 | Undervoltage detection delay | | | t _{dUV} | 7 | | 21 | ms | A |
| 4 Thermal Prewarning and Shutdown | | | | | | | | | |
| 4.1 | Thermal prewarning | | | T _{jPWset} | 170 | 195 | 220 | °C | B |
| 4.2 | Thermal prewarning | | | T _{jPWreset} | 155 | 180 | 205 | °C | B |
| 4.3 | Thermal prewarning hysteresis | | | T _{jPW} | | 15 | | K | C |
| 4.4 | Thermal shutdown | | | T _{j switch off} | 200 | 225 | 250 | °C | B |
| 4.5 | Thermal shutdown | | | T _{j switch on} | 185 | 210 | 235 | °C | B |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes: 1. Delay time between rising edge of input signal at pin CS after data transmission and switch on/off output stages to 90% of final level. Device not in standby for t > 1ms.

7. Electrical Characteristics (Continued)

7.5V < V_{VS} < 40V; 4.75V < V_{CC} < 5.25V; INH = High; -40°C < T_j < 200°C, T_a ≤ 150°C; unless otherwise specified, all values refer to GND pins.

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|------|--|---|---------------------------|--|-------|------|------|------|-------|
| 4.6 | Thermal shutdown hysteresis | | | T _j switch off | | 15 | | K | C |
| 4.7 | Ratio thermal shutdown/thermal prewarning | | | T _j switch off/ T _j PW set | 1.05 | 1.2 | | | C |
| 4.8 | Ratio thermal shutdown/thermal prewarning | | | T _j switch on/ T _j PW reset | 1.05 | 1.2 | | | C |
| 5 | Output Specification (LS1-LS6, HS1-HS6) 7.5V < V _{VS} < 40V | | | | | | | | |
| 5.1 | On resistance | I _{Out} = 600mA | 2, 5, 8, 11, 20, 23 | R _{DS OnL} | | | 2.2 | Ω | A |
| 5.2 | On resistance | I _{Out} = -600mA | 2, 5, 8, 11, 20, 23 | R _{DS OnH} | | | 2.2 | Ω | A |
| 5.3 | High-side output leakage current (total quiescent current see 1.1) | V _{Out1-6} = 0V all output stages off | 2, 5, 8, 11, 20, 23 | I _{Out1-6} | -60 | | | μA | A |
| 5.4 | Low-side output leakage current (total quiescent current see 1.1) | V _{Out1-6} = VS all output stages off | 2, 5, 8, 11, 20, 23 | I _{Out1-6} | | | 250 | μA | A |
| 5.5 | Inductive shutdown energy | | 2, 5, 8, 11, 20, 23 | W _{outx} | | | 15 | mJ | D |
| 5.6 | Overcurrent limitation and shutdown threshold | V _{VS} ≤ 13V | 2, 5, 8, 11, 20, 23 | I _{LS1-6} | 650 | 950 | 1400 | mA | A |
| 5.7 | Overcurrent limitation and shutdown threshold | V _{VS} ≤ 13V | 2, 5, 8, 11, 20, 23 | I _{HS1-6} | -1400 | -950 | -650 | mA | A |
| 5.8 | Overcurrent limitation and shutdown threshold | 20V < V _{VS} < 40V | 2, 5, 8, 11, 20, 23 | I _{LS1-6} | 650 | 950 | 1600 | mA | C |
| 5.9 | Overcurrent limitation and shutdown threshold | 20V < V _{VS} < 40V | 2, 5, 8, 11, 20, 23 | I _{HS1-6} | -1600 | -950 | -650 | mA | C |
| 5.10 | Overcurrent shutdown delay time | Input register bit 14 (SCT) = low V _{VS} = 13V | | t _{dSd} | 0.9 | 1.5 | 2.1 | ms | A |
| 5.11 | Overcurrent shutdown delay time | Input register bit 14 (SCT) = High V _{VS} = 13V | | t _{dSd} | 7 | 12 | 17 | ms | A |
| 5.12 | High-side open load detection current | Input register bit 13 (OLD) = low, output off | 2, 5, 8, 11, 20, 23 | I _{Out1-3H} | -1.6 | | -0.3 | mA | A |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes: 1. Delay time between rising edge of input signal at pin CS after data transmission and switch on/off output stages to 90% of final level. Device not in standby for t > 1ms.

7. Electrical Characteristics (Continued)

7.5V < V_S < 40V; 4.75V < V_{CC} < 5.25V; INH = High; -40°C < T_j < 200°C, T_a ≤ 150°C; unless otherwise specified, all values refer to GND pins.

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|----------|---|---|---------------------|--|------------------------|------|------------------------|------|-------|
| 5.13 | Low-side open load detection current | Input register bit 13 (OLD) = low, output off | 2, 5, 8, 11, 20, 23 | I _{Out1-3L} | 0.3 | | 1.6 | mA | A |
| 5.14 | Open load detection current ratio | | 2, 5, 8, 11, 20, 23 | I _{OLoutLX} / I _{OLoutHX} | 1.05 | 1.2 | 2 | | |
| 5.15 | High-side open load detection voltage | Input register bit 13 (OLD) = low, output off | 2, 5, 8, 11, 20, 23 | V _{Out1-6H} | 0.5 | | 2.5 | V | A |
| 5.16 | Low-side open load detection voltage | Input register bit 13 (OLD) = low, output off | 2, 5, 8, 11, 20, 23 | V _{Out1-6L} | 0.5 | | 2.2 | V | A |
| 5.17 | High-side output switch on delay ⁽¹⁾ | V _{VS} = 13V R _{Load} = 30Ω | | t _{don} | | | 20 | μs | A |
| 5.18 | Low-side output switch on delay ⁽¹⁾ | V _{VS} = 13V R _{Load} = 30Ω | | t _{don} | | | 20 | μs | A |
| 5.19 | High-side output switch off delay ⁽¹⁾ | V _{VS} = 13V R _{Load} = 30Ω | | t _{doff} | | | 20 | μs | A |
| 5.20 | Low-side output switch off delay ⁽¹⁾ | V _{VS} = 13V R _{Load} = 30Ω | | t _{doff} | | | 3 | μs | A |
| 5.21 | Dead time between corresponding high- and low-side switches | V _{VS} = 13V R _{Load} = 30Ω | | t _{don} - t _{doff} | 1 | | | μs | A |
| 6 | Inhibit Input | | | | | | | | |
| 6.1 | Input voltage low-level threshold | | 12 | V _{IL} | 0.3 × V _{VCC} | | | V | A |
| 6.2 | Input voltage high-level threshold | | 12 | V _{IH} | | | 0.7 × V _{VCC} | V | A |
| 6.3 | Hysteresis of input voltage | | 12 | ΔV _I | 100 | | 700 | mV | A |
| 6.4 | Pull-down current | V _{INH} = V _{VCC} | | I _{PD} | 10 | | 80 | μA | A |
| 7 | Serial Interface: Logic Inputs DI, CLK, CS | | | | | | | | |
| 7.1 | Input voltage low-level threshold | | 17 - 19 | V _{IL} | 0.3 × V _{VCC} | | | V | A |
| 7.2 | Input voltage high-level threshold | | 17 - 19 | V _{IH} | | | 0.7 × V _{VCC} | V | A |
| 7.3 | Hysteresis of input voltage | | 17 - 19 | ΔV _I | 50 | | 500 | mV | A |
| 7.4 | Pull-down current pin DI, CLK | V _{DI} , V _{CLK} = V _{VCC} | 18 - 19 | I _{PDSI} | 2 | | 50 | μA | A |
| 7.5 | Pull-up current pin CS | V _{CS} = 0V | 17 | I _{PUSI} | -50 | | -2 | μA | A |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes: 1. Delay time between rising edge of input signal at pin CS after data transmission and switch on/off output stages to 90% of final level. Device not in standby for t > 1ms.

7. Electrical Characteristics (Continued)

7.5V < V_S < 40V; 4.75V < V_{CC} < 5.25V; INH = High; -40°C < T_j < 200°C, T_a ≤ 150°C; unless otherwise specified, all values refer to GND pins.

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|-----|-----------------------------------|---|-----|------------------|-------------------------|------|------|------|-------|
| 8 | Serial Interface: Logic Output DO | | | | | | | | |
| 8.1 | Output voltage low level | I _{OL} = 3mA | 13 | V _{DOL} | | | 0.5 | V | A |
| 8.2 | Output voltage high level | I _{OL} = -1mA | 13 | V _{DOH} | V _{VCC} - 0.7V | | | V | A |
| 8.3 | Leakage current (tri-state) | V _{CS} = V _{VCC} , 0V < V _{DO} < V _{VCC} | 13 | I _{DO} | -10 | | 10 | μA | A |

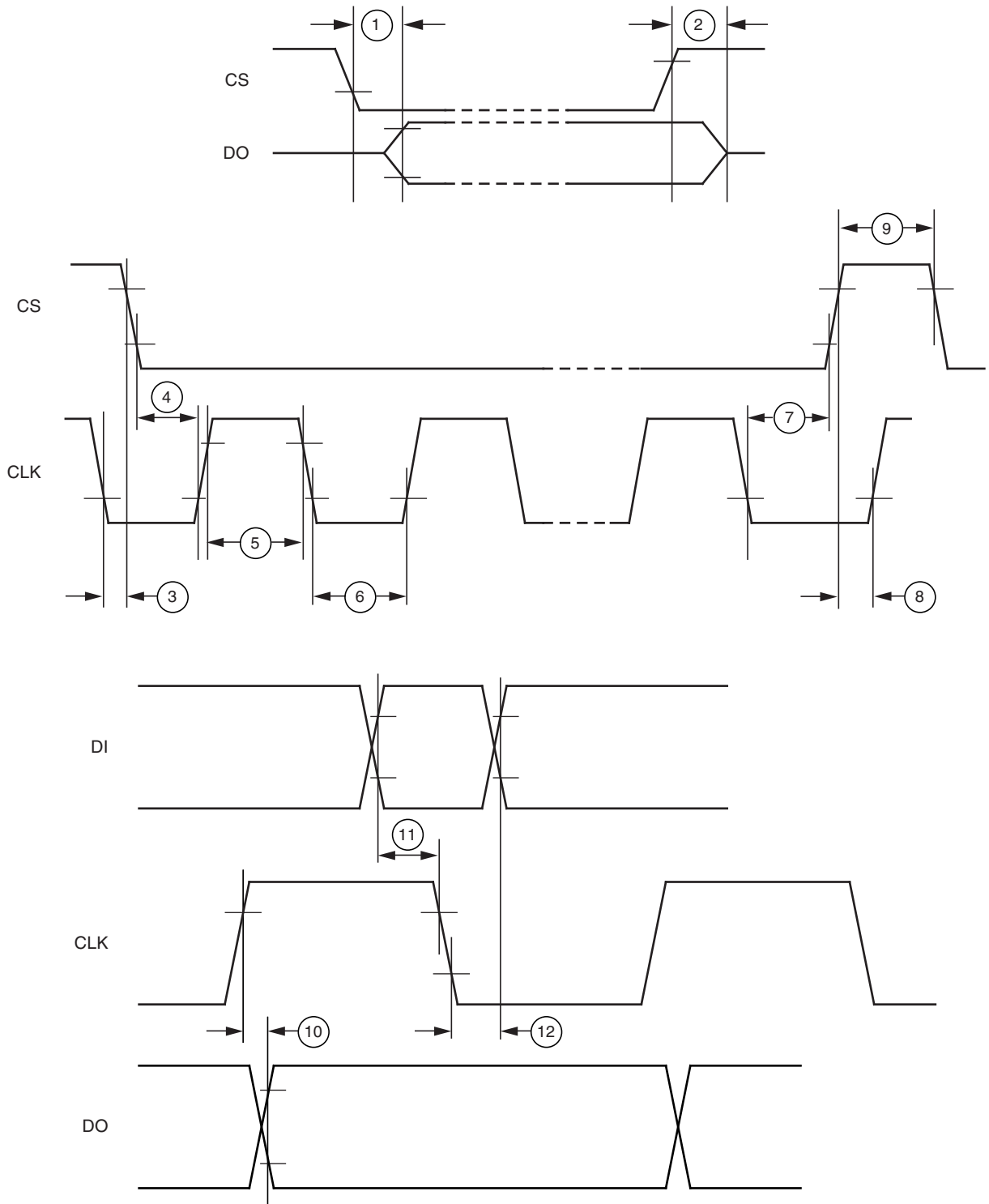
*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes: 1. Delay time between rising edge of input signal at pin CS after data transmission and switch on/off output stages to 90% of final level. Device not in standby for t > 1ms.

8. Serial Interface: Timing

| Parameters | Test Conditions | Pin | Timing Chart No. | Symbol | Min. | Typ. | Max. | Unit |
|---------------------------------|------------------------------------|-----|------------------|-----------------------|------|------|------|------|
| DO enable after CS falling edge | C _{DO} = 100pF | 13 | 1 | t _{ENDO} | | | 200 | ns |
| DO disable after CS rising edge | C _{DO} = 100pF | 13 | 2 | t _{DISDO} | | | 200 | ns |
| DO fall time | C _{DO} = 100pF | 13 | - | t _{DOF} | | | 100 | ns |
| DO rise time | C _{DO} = 100pF | 13 | - | t _{DOR} | | | 100 | ns |
| DO valid time | C _{DO} = 100pF | 13 | 10 | t _{DOVal} | | | 200 | ns |
| CS setup time | | 17 | 4 | t _{CSSethl} | 225 | | | ns |
| CS setup time | | 17 | 8 | t _{CSSethh} | 225 | | | ns |
| CS high time | Input register bit 14 (SCT) = high | 17 | 9 | t _{CSh} | 17 | | | ms |
| CS high time | Input register bit 14 (SCT) = low | 17 | 9 | t _{CSh} | 2.1 | | | ms |
| CLK high time | | 18 | 5 | t _{CLKh} | 225 | | | ns |
| CLK low time | | 18 | 6 | t _{CLKl} | 225 | | | ns |
| CLK period time | | 18 | - | t _{CLKp} | 500 | | | ns |
| CLK setup time | | 18 | 7 | t _{CLKsethl} | 225 | | | ns |
| CLK setup time | | 18 | 3 | t _{CLKsethh} | 225 | | | ns |
| DI setup time | | 19 | 11 | t _{Dlset} | 40 | | | ns |
| DI hold time | | 19 | 12 | t _{DlHold} | 40 | | | ns |

Figure 8-1. Serial Interface Timing Diagram with Chart Numbers



Inputs DI, CLK, CS: High level = $0.7 \times V_{CC}$, low level = $0.2 \times V_{CC}$
 Output DO: High level = $0.8 \times V_{CC}$, low level = $0.2 \times V_{CC}$

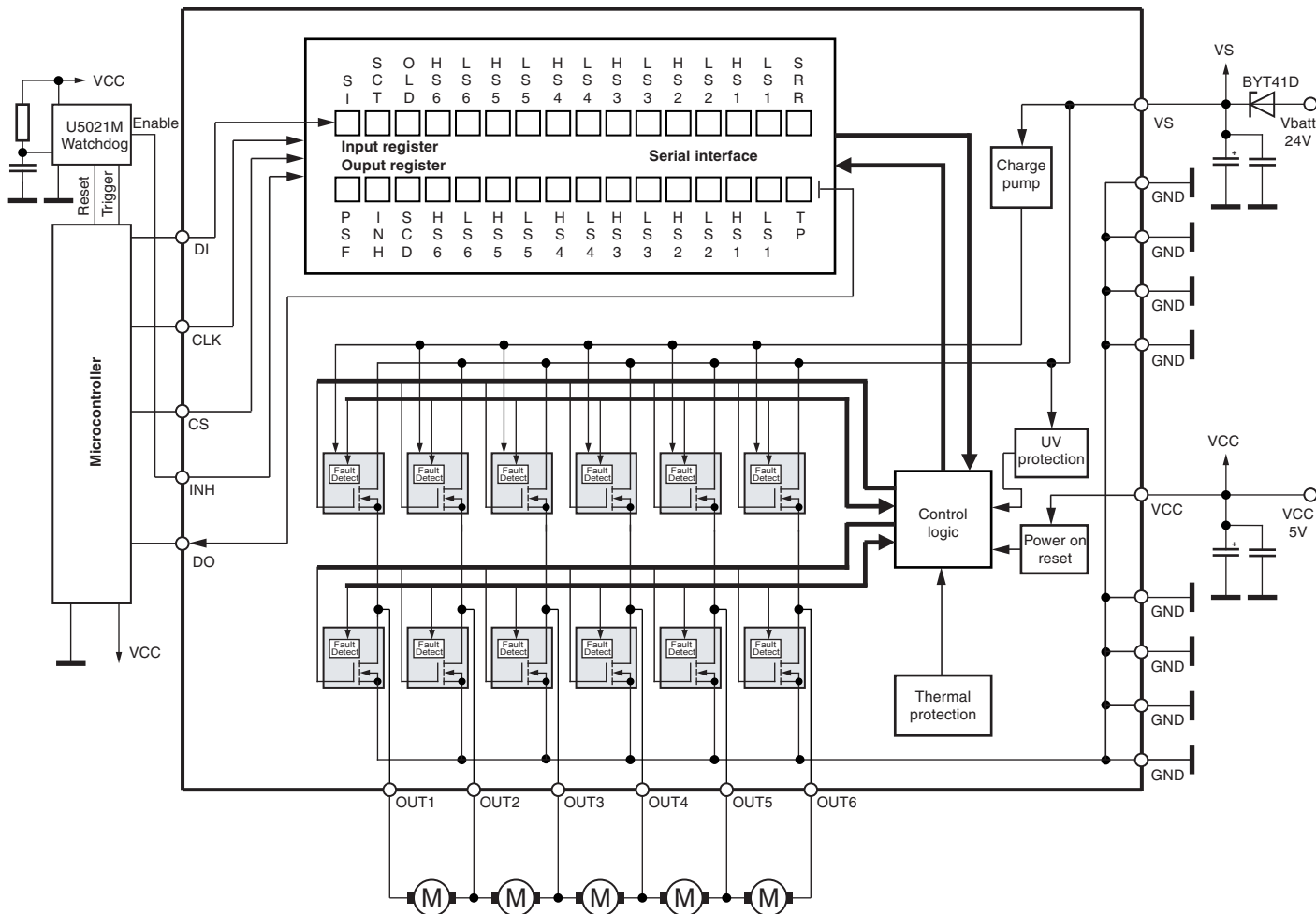
9. Noise and Surge Immunity

| Parameters | Test Conditions | Value |
|---------------------------|-----------------|------------------------|
| Conducted interferences | ISO 7637-1 | Level 4 ⁽¹⁾ |
| Interference suppression | VDE 0879 Part 2 | Level 5 |
| ESD (Human Body Model) | ESD S 5.1 | 4kV |
| CDM (Charge Device Model) | ESD STM5.3 | 500V |
| MM (Machine Model) | ESD STM5.2 | 200V |

Note: 1. Test pulse 5: $V_{vbmax} = 40V$

10. Application Circuit

Figure 10-1. Application Circuit



10.1 Application Notes

- Connect the blocking capacitors at V_{CC} and V_S as close as possible to the power supply and GND pins.
- Recommended value for capacitors at V_S :
Electrolytic capacitor $C > 22\mu\text{F}$ in parallel with a ceramic capacitor $C = 100\text{nF}$. Value for electrolytic capacitor depends on external loads, conducted interferences and reverse-conducting current I_{HSX} (see [Section 4. "Absolute Maximum Ratings" on page 8](#)).
- Recommended value for capacitors at V_{CC} :
Electrolytic capacitor $C > 10\mu\text{F}$ in parallel with a ceramic capacitor $C = 100\text{nF}$.
- To reduce thermal resistance, place cooling areas on the PCB as close as possible to GND pins and to the die paddle in QFN24.
- The sense pins $\text{OUT}_x \text{ SENSE}$ can either be left open or can be connected to the adjacent OUT_x pin. Never use the sense pins $\text{OUT}_x \text{ SENSE}$ as power outputs.

11. Ordering Information

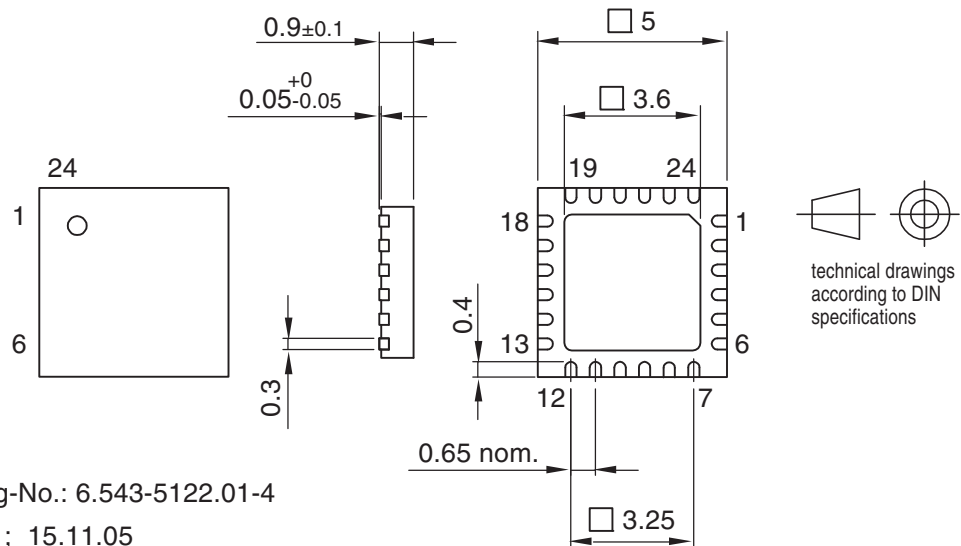
| Extended Type Number | Package | Remarks |
|----------------------|---------|---------------------------|
| ATA6837-PXQW | QFN24 | Taped and reeled, Pb-free |

12. Package Information

Package: QFN 24 - 5 x 5
 Exposed pad 3.6 x 3.6
 (acc. JEDEC OUTLINE No. MO-220)

Dimensions in mm

Not indicated tolerances ± 0.05



Drawing-No.: 6.543-5122.01-4

Issue: 1; 15.11.05

13. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

| Revision No. | History |
|------------------|---|
| 4953H-AUTO-03/12 | <ul style="list-style-type: none">• Section 3.5 “Short-circuit Protection” on page 7 changed |
| 4953G-AUTO-03/11 | <ul style="list-style-type: none">• Section 10.1 “Application Notes” on page 15 changed |
| 4953F-AUTO-02/10 | <ul style="list-style-type: none">• Section 7 “Electrical Characteristics” numbers 5.10 and 5.11 on page 10 changed |
| 4953E-AUTO-09/09 | <ul style="list-style-type: none">• Section 7 “Electrical Characteristics” number 1.7 on page 9 added |
| 4953D-AUTO-10/08 | <ul style="list-style-type: none">• Features on page 1 changed• Table 2-1 “Pin Description QFN24” on pages 3 to 4 changed• Section 4 “Abs.Max.Ratings” on page 8 changed• Section 5 “Thermal Resistance” on page 8 changed• Section 6 “Operating Range” on page 8 changed• Section 7 “Electrical Characteristics” numbers 1.1, 1.2, 1.6, 4.1 to 4.7, 5.3, 5.4 and 5.6 to 5.9 on pages 9 to 10 changed• Section 8 “Serial Interface: Timing” on page 12 changed• Section 9 “Noise and Surge Immunity” on page 16 changed• Section 11 “Ordering Information” on page 14 changed |
| 4953C-AUTO-09/07 | <ul style="list-style-type: none">• Section 7 “Electrical Characteristics” numbers 5.15 and 5.16 on page 10 changed• Section 9 “Noise and Surge Immunity” on page 14 changed |
| 4953B-AUTO-07/07 | <ul style="list-style-type: none">• Put datasheet in a new template• Section 7 “Electrical Characteristics” numbers 1.5, 3.1, 5.15 and 8.2 on pages 9 to 11 changed |



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