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ATA6843/ATA6844

BLDC Motor Driver and LIN System Basis Chip

DATASHEET

Features

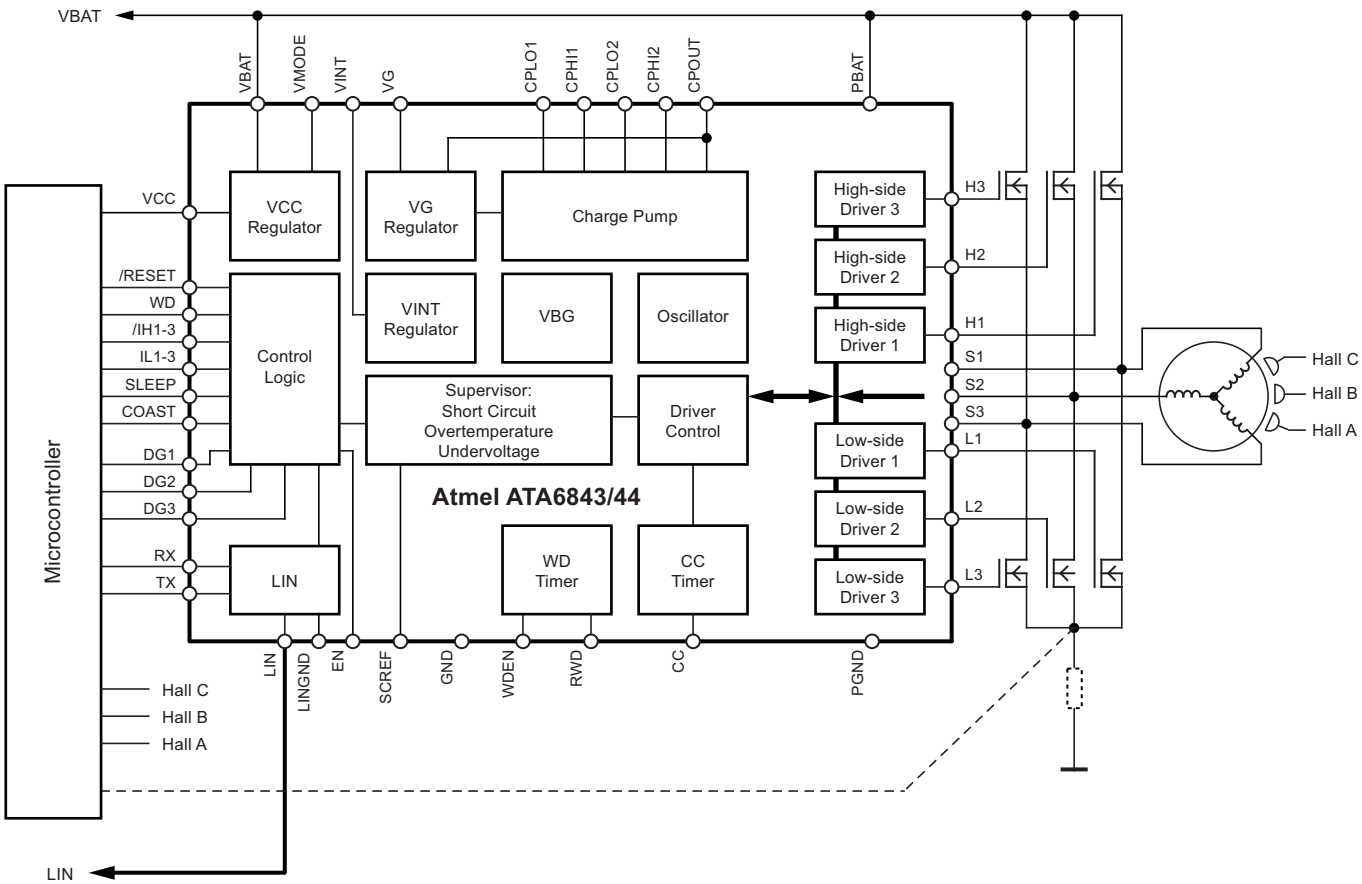
- Broad operation voltage range from 5.25V to 32V
- Atmel® ATA6843 temperature range T_J = 150°C
- Atmel ATA6844 extended temperature range T_J = 200°C
- Direct driving of six external NMOS transistors with a maximum switching frequency of 50kHz
- Integrated charge pump to provide gate voltages for high-side drivers and to supply the gate of the external battery reverse protection NMOS
- Built-in 5V/3.3V voltage regulator with current limitation
- Reset signal for the microcontroller
- Sleep Mode with supply current of typically < 45µA
- Wake-up via LIN bus or high voltage input
- Programmable window watchdog
- Battery overvoltage protection and battery undervoltage management
- Overtemperature warning and protection (shutdown)
- Jump start compatible
- LIN transceiver conformal to LIN 2.1 and SAEJ2602-2 with outstanding EMC and ESD performance
- QFN48 package 7mm × 7mm

1. Description

The Atmel® ATA6843 and Atmel ATA6844 are system basis chips for three-phase brushless DC motor controllers designed in Atmel's state-of-the-art 0.8µm SOI technology SMART-I.S.™1. In combination with a microcontroller and six discrete power MOSFETs, the system basis chip forms a BLDC motor control unit for automotive applications. In addition, the circuits provide a 3.3V/5V linear regulator and a window watchdog.

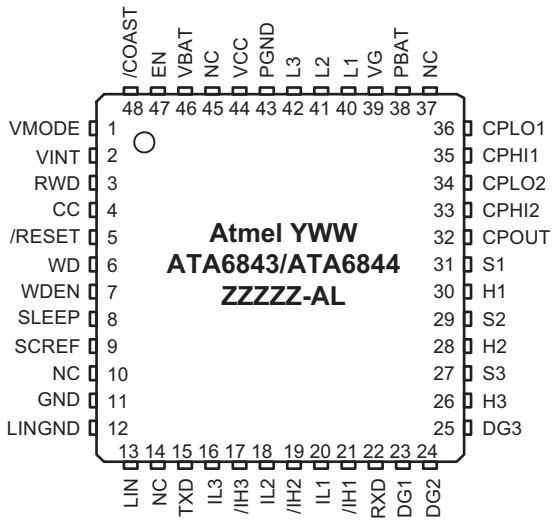
The circuit includes various control and protection functions like overvoltage and overtemperature protection, short circuit detection, and undervoltage management. Thanks to these function blocks, the driver fulfils a maximum of safety requirements and offers a high integration level to save cost and space in various applications. The target applications are most suitable for the automotive market due to the robust technology and the high qualification level. Atmel ATA6844, in particular, is designed for applications in a high-temperature environment.

Figure 1-1. Block Diagram



2. Pin Configuration

Figure 2-1. Pinning QFN48



Note: YWW Date code (Y = Year - above 2000, WW = week number)
ATA683x Product name
ZZZZZ Wafer lot number
AL Assembly sub-lot number

Table 2-1. Pin Description

Pin	Symbol	I/O	Function
1	VMODE	I	Selector for V_{CC} and interface logic voltage level
2	VINT	I/O	Blocking capacitor
3	RWD	I	Resistor defining the watchdog interval
4	CC	I/O	RC combination to adjust cross conduction time
5	/RESET	O	Reset signal for microcontroller
6	WD	I	Watchdog trigger signal
7	WDEN	I	Enable and disable the watchdog
8	SLEEP	I	Microcontroller output to switch system in Sleep Mode
9	SCREF	I	Short circuit comparator Reference input
10	NC		Connect to GND
11	GND	I	Ground
12	LINGND	I	Ground for LIN, Connect to GND
13	LIN	I/O	LIN-bus terminal
14	NC		Connect to GND
15	TXD	I	Transmit signal to LIN bus from microcontroller
16	IL3	I	Control Input for output L3
17	/IH3	I	Control Input for output H3
18	IL2	I	Control Input for output L2
19	/IH2	I	Control Input for output H2
20	IL1	I	Control Input for output L1
21	/IH1	I	Control Input for output H1

Table 2-1. Pin Description

Pin	Symbol	I/O	Function
22	RXD	O	Receive signal from LIN bus for microcontroller
23	DG1	O	Diagnostic output 1
24	DG2	O	Diagnostic output 2
25	DG3	O	Diagnostic output 3
26	H3	O	Gate voltage high-side 3
27	S3	I/O	Voltage at half bridge 3
28	H2	O	Gate voltage high-side 2
29	S2	I/O	Voltage at half bridge 2
30	H1	O	Gate voltage high-side 1
31	S1	I/O	Voltage at half bridge 1
32	CPOUT	I/O	Charge pump output capacitor
33	CPHI2	I	Charge pump capacitor 2
34	CPLO2	O	Charge pump capacitor 2
35	CPHI1	I	Charge pump capacitor 1
36	CPLO1	O	Charge pump capacitor 1
37	NC		Connect to GND
38	PBAT	I	Power supply (after reverse protection) for charge pump and gate drivers
39	VG	I/O	Blocking capacitor
40	L1	O	Gate voltage H-bridge, low-side 1
41	L2	O	Gate voltage H-bridge, low-side 2
42	L3	O	Gate voltage H-bridge, low-side 3
43	PGND	I	Power ground for H-bridge and charge pump
44	VCC	O	5V/100mA supply for microcontroller
45	NC		Connect to GND
46	VBAT	I	Supply voltage for IC core (after reverse protection)
47	EN	I	High voltage enable input
48	/COAST	I	Control input for coast function of bridge

3. Functional Description

3.1 Power Supply Unit with Supervisor Functions

3.1.1 Power Supply

The IC has to be supplied by a reverse-protected battery voltage. To prevent damage to the IC, proper external protection circuitry has to be added. It is recommended to use at least one capacitor combination of storage and RF capacitors be-hind the reverse protection circuitry, which is connected close to the VBAT and GND pins of the IC.

A fully integrated low-power and low-drop regulator (VINT regulator), stabilized by an external blocking capacitor, provides the necessary low-voltage supply needed for the wake-up process. A trimmed low-power band gap is used as reference for the VINT regulator as well as for the VCC regulator. All internal blocks are supplied by VINT regulator. VINT regulator must not be used for any external supply purposes.

Nothing inside the IC except the logic interface to the external microcontroller is supplied by the 5V/3.3V VCC regulator.

Both voltage regulators are checked by a “power-good comparator”, which keeps the whole chip in reset as long as the internal supply voltage (VINT regulator output) is too low and gnerates a reset for the external microcontroller if the out-put voltage of the VCC regulator is not sufficient.

3.1.2 Voltage Supervisor

This function is implemented to protect the IC and the external power MOS transistors from damage due to overvoltage on PBAT input. In the event of overvoltage (V_{THOV}) or undervoltage (V_{THUV}), the external NMOS motor driver transistors will be switched off. The failure state will be flagged on DG2 pin. It is recommended to block PBAT with an external RF capacitor to suppress high frequency disturbances.

3.1.3 Temperature Supervisor

An integrated temperature sensor prevents the IC from overheating. If the temperature is above the overtemperature prewarning threshold $T_{JPW\ set}$, the diagnostic pin DG3 will be switched to HIGH to signal this event to the external microcontroller. The microcontroller should take actions to reduce the power dissipation in the IC. If the temperature rises above the overtemperature shutdown threshold $T_{J\ switch\ off}$, the VCC regulator and all output drivers together with the LIN transceiver will be switched OFF immediately and the /RESET signal will go LOW. Both thresholds have a built-in hysteresis to avoid oscillations. The IC will return to normal operation (Active Mode) when it has cooled down below the shutdown threshold. When the junction temperature drops below the pre-warning threshold, bit DG3 will be switched LOW.

3.2 Active Mode and Sleep Mode

The IC has two modes: Active Mode and Sleep Mode. By default the IC starts in Active Mode (normal operation) after power-on. An *Enter Sleep Mode* procedure switches the IC from Active Mode to Sleep Mode (standby). *Enter Active Mode* procedures wake up the IC back from Sleep Mode. When in Sleep Mode the internal 5V supply (VINT regulator), the EN input pin, and a small part of the LIN receiver remain active to ensure a proper startup of the system. The VCC regulator is turned off.

The *Enter Sleep Mode* and *Enter Active Mode* procedures are implemented as follows:

Enter Sleep Mode:

Pin SLEEP is a low-voltage input supplied by the VCC regulator. It is ESD protected by diodes against VCC and GND. Thus the input voltage at pin SLEEP must not go below GND or exceed the output voltage of the VCC regulator. A transition from HIGH to LOW followed by a permanent LOW signal for a minimum time period $t_{gotosleep}$ (typical 10µs) at pin SLEEP switches the IC to Sleep Mode as the SLEEP is edge triggered. V_{CC} is switched off in Sleep Mode. It is recommended to keep SLEEP LOW during normal operation.

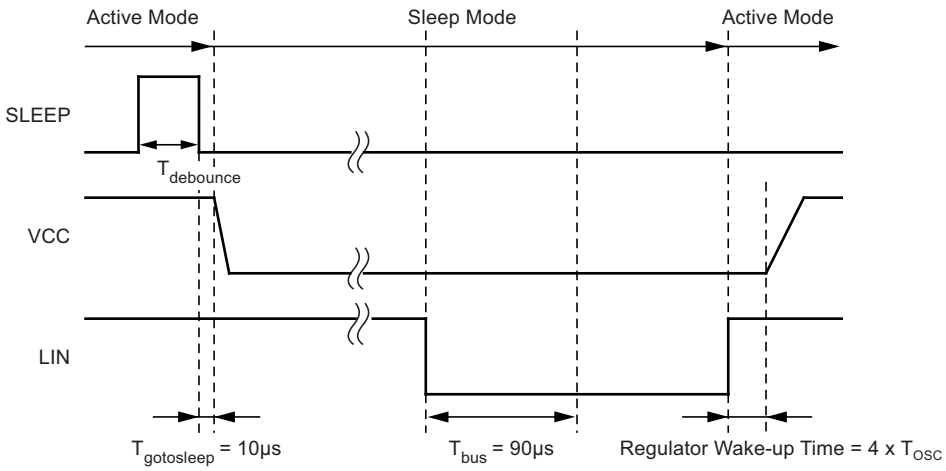
Enter Active Mode Using Pin EN:

Pin EN is a high-voltage input for external wake-up signals. Its input structure consists of a comparator with a built-in hysteresis. It is ESD-protected by diodes against GND and V_{BAT}, and for this reason the applied input voltage must not go below GND or exceed V_{BAT}. Pulling EN up to V_{BAT} switches the IC to Active Mode. EN is debounced and edge triggered.

Enter Active Mode Using the LIN Interface:

Using the LIN interface provides a second possibility to wake-up the IC (see Figure 3-1). A voltage lower than the LIN pre-wake detection V_{LINL} at pin LIN activates the internal LIN receiver and starts the wake-up detection timer. A falling edge at pin LIN followed by a dominant bus level V_{BUSdom} maintained for a minimum time period (T_{bus}) and ending with a rising edge leads to a remote wake-up request. The device switches from Sleep Mode to Active Mode. The VCC regulator is activated and the internal LIN slave termination resistor is switched on.

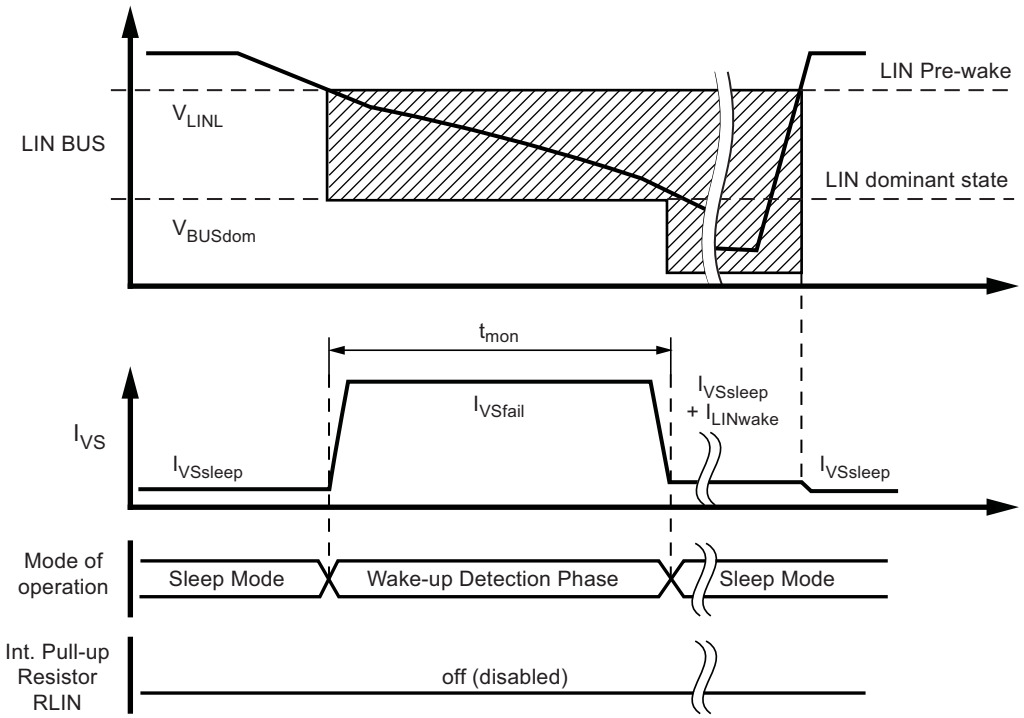
Figure 3-1. Wake-up Using the LIN Interface



In Sleep Mode the device has a very low current consumption even during short circuits or floating conditions on the bus. A floating bus can arise if the Master pull-up resistor is missing, e.g., it is switched off when the LIN-Master is in Sleep Mode or even if the power supply of the Master node is switched off.

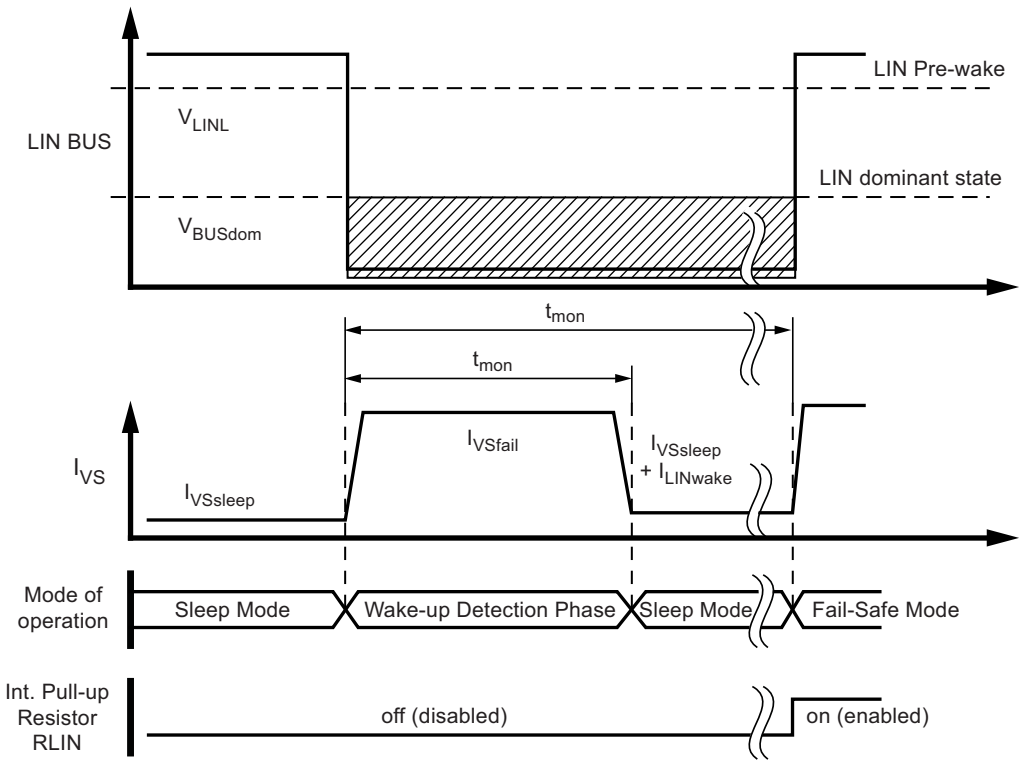
In order to minimize the current consumption IVBAT during voltage levels at the LIN-pin below the LIN pre-wake threshold, the receiver is activated only for a specific time t_{mon}. If t_{mon} elapses while the voltage at the bus is lower than Pre-wake detection low (V_{LINL}) and higher than the LIN dominant level, the receiver is switched off again and the circuit changes back to sleep mode. The current consumption is then the result of I_{VBAT} plus $I_{LINwake}$. If a dominant state is reached on the bus no wake-up will occur. Even if the voltage rises above the Pre-wake detection high (V_{LINH}), the IC will stay in sleep mode (see Figure 3-2). This means the LIN-bus must be above the Pre-wake detection threshold V_{LINH} for a few microseconds before a new LIN wake-up is possible.

Figure 3-2. Floating LIN-bus During Sleep Mode



If the Atmel® ATA6843/ATA6844 is in Sleep Mode and the voltage level at the LIN is in dominant state ($V_{LIN} < V_{BUSdom}$) for a time period exceeding t_{mon} (during a short circuit at LIN, for example), the IC switches back to Sleep mode. The VBAT current consumption then consists of I_{VBAT} plus $I_{LINWAKE}$. After a positive edge at pin LIN the IC switches directly to Active Mode (see Figure 3-3).

Figure 3-3. Short Circuit to GND on the LIN-bus During Sleep Mode



3.3 5V/3.3V VCC Regulator

The 5V/3.3V regulator is fully integrated. It requires an external electrolytic capacitor in the range of 2.2µF up to 10µF and with an ESR in the range from 2 to 15 for stability (see Figure 3-4). The output voltage can be configured as either 5V or 3.3V by connecting pin VMODE to either pin VINT or GND. Since the regulator is not designed to be switched between both output voltages during operation, it is advisable to hard-wire VMODE pin. The logic levels of the microcontroller interface are adapted to the VCC regulator output voltage. The maximum output current (I_{OS1}) of the regulator is 100mA. For T_J > 150°C the IOS1 of Atmel® ATA6844 is reduced to 80mA. The VCC regulator has a built-in short circuit protection. A comparator checks the output voltage of the VCC regulator and keeps the external microcontroller in reset as long as the voltage is below the lower operation minimum (shown in Figure 3-5).

Figure 3-4. ESR versus Load Current for External Capacitors with Different Values

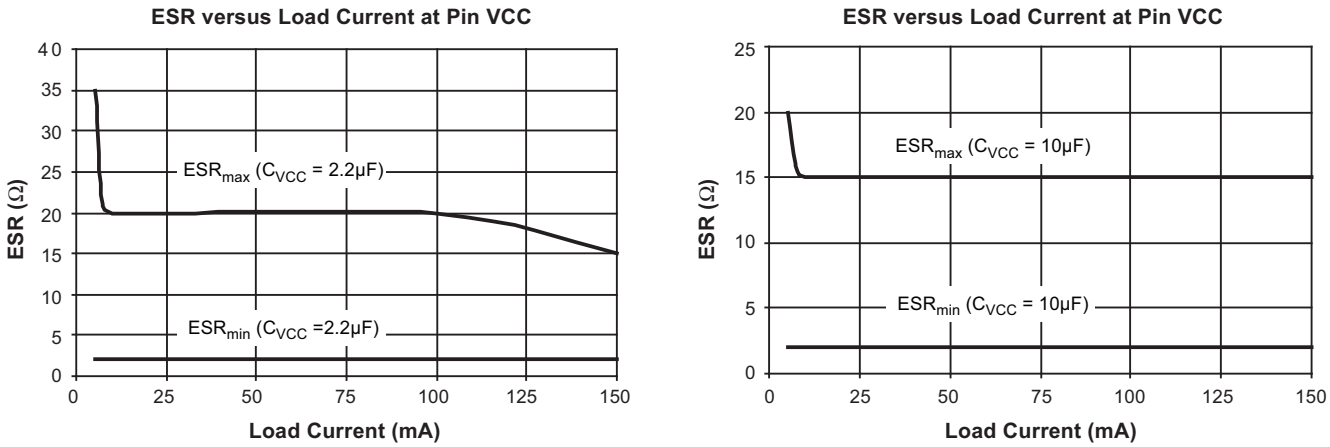
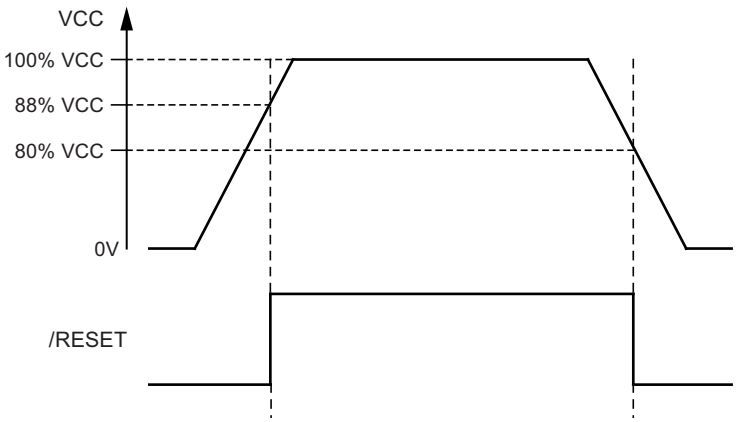


Figure 3-5. /RESET as Function of the VCC Output Voltage

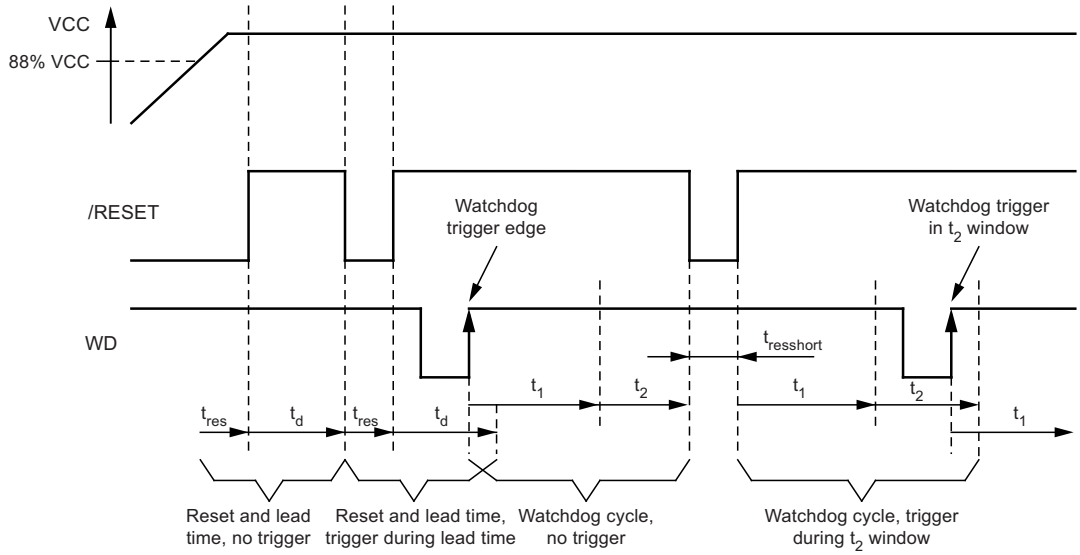


3.4 Reset and Watchdog Management

The watchdog timing is based on the trimmed internal watchdog oscillator. Its period time T_{OSC} is determined by the external resistor R_{WD}. A HIGH signal on WDEN pin enables the watchdog function; a LOW signal disables it. Since the WDEN pin is equipped with an internal pull-up resistor the watchdog is enabled by default. In order to keep the current consumption as low as possible the watchdog is switched off during Sleep Mode.

The timing diagram in Figure 3-6 shows the watchdog and external reset timing.

Figure 3-6. Timing Diagram of the Watchdog in Conjunction with the /RESET Signal



After power-up of the VCC regulator (VCC output exceeds 88% of its nominal value) /RESET output stays LOW for the timeout period t_{res} (typical 10ms). Subsequently /RESET output switches to HIGH. During the following time t_d (typical 500ms) a rising edge at the input WD is expected otherwise another external reset will be triggered.

When the watchdog has been correctly triggered for the first time, normal watchdog operation begins. A normal watchdog cycle consists of two time sections t_1 and t_2 followed by a short pulse for the time tresshort at /RESET if no valid trigger has been applied at pin WD during t_2. Rising edges on WD pin during t_1 also cause a short pulse on /RESET. Start for such a cycle is always the time of the last rising edge either on WD pin or on /RESET pin.

If the watchdog is disabled (WDEN = LOW), only the initial reset for the time t_{res} after power-up will be generated.

Additional resets will be generated if the VCC output voltage drops below 80% of its nominal value.

The following example demonstrates how to calculate the timing scheme for valid watchdog trigger pulses, which the external microcontroller has to provide in order to prevent undesired resets.

Example:

Using an external resistor R_{WD} = 33kΩ ±1% results in typical parameters as follows:

T_{OSC} = 12.4µs

$t_1 = 980 \times T_{OSC}$ = 12.1ms ±10%

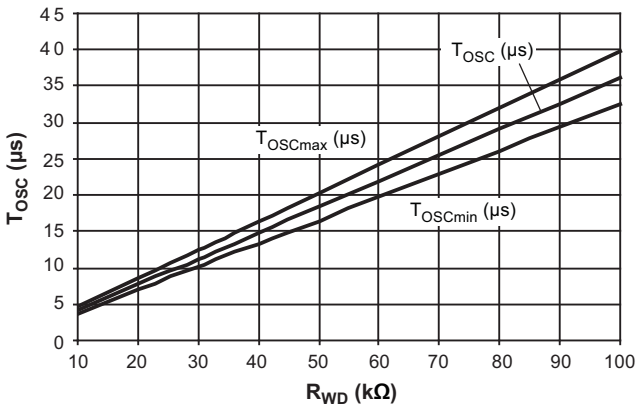
$t_2 = 780 \times T_{OSC}$ = 9.6ms ±10%

$t_1 + t_2$ = 21.7ms ±10%

Hence, the minimum time the external microcontroller has to wait before pin WD can be triggered is in worst case $t_{min} = 1.1 \times t_1$ = 13.3ms. The maximum time for the watchdog trigger on WD pin is $t_{max} = 0.9 \times (t_1 + t_2)$ = 19.5ms. Thus watchdog trigger input must remain within $t_{max} - t_{min}$ = 6.2ms.

Other values can be set up by picking a different resistor value for R_{WD}. The dependency of T_{OSC} on the value of R_{WD} is shown in Figure 3-7.

Figure 3-7. T_{OSC} versus R_{WD}



The tolerance of T_{OSC} is ±10% for resistors R_{WD} with maximum ±1% in tolerance.

3.5 Charge Pump

A charge pump has been implemented in order to provide sufficient voltage to operate the external high-side power-NMOS transistors and the VG regulator, which drives the low-side Power-NMOS transistors. The charge pump output voltage at CPOUT pin is controlled to settle typically about 15V above the voltage at pin PBAT. A built-in supervisor circuit checks if the output voltage is sufficient to operate the VG regulator and external Power-NMOS transistors. The output voltage is accepted as good when it rises above VCP_{CPGOOD}. A charge pump failure is flagged at DG2 if this minimum can not be reached or if the output voltage drops below the lower threshold of VCP_{CPGOOD} due to overloading.

The two shuffle capacitors should have the same value. The value of the reservoir capacitor should be at least twice the value of one shuffle capacitor. Two external shuffle capacitors and an external reservoir capacitor have to be provided. The typical value for the two shuffle capacitors is 100nF, and for the reservoir capacitor is 1.5µF. All capacitors should be ceramic. The greater the capacitors are, the greater the output current capability.

3.6 VG Regulator

The VG regulator provides a stable voltage to supply the low-side gate drivers and to deliver sufficient voltage for the external low-side Power-NMOS transistors. Typically the output voltage is 12V. In order to guarantee reliable operation even with a low battery voltage, the VG regulator is supplied by the charge pump output. For stability, an external ceramic capacitor of typically 470nF has to be provided. There is no internal supervision of the VG output voltage.

3.7 Output Drivers and Control Inputs IL1-IL3, /IH1-/IH3 and /COAST

This IC offers six push-pull output drivers for the external low-side and high-side power-NMOS transistors. To guarantee reliable operation, the low-side drivers are supplied by the VG regulator while the high-side drivers are supplied directly by the charge pump. All drivers are designed to operate at switching frequencies in the range of DC up to 50kHz. The maximum gate charge that can be delivered to each external Power-NMOS transistor at 50kHz is 100nC.

The output drivers L1 to L3 and H1 to H3 are directly controlled by the digital input pins IL1 to IL3 and /IH1 to /IH3 (see Table 3-1 on page 11). IL1 to IL3 are high active digital inputs equipped with an internal pull-down resistor, while /IH1 to /IH3 are low active digital inputs equipped with an internal pull-up resistor.

The pin /COAST is a low active input with internal pull-up resistor, which forces low all output drivers L1-L3 and H1-H3, and turns off all external FETs. As a safety function, /COAST allows to emergency switch off all output drivers to coast a BLDC motor.

To operate the output drivers properly the following requirements have to be fulfilled:

1. Device is in Active Mode.
2. In case of watchdog is enabled, at least one valid watchdog trigger has been accepted.
3. The voltage at pin PBAT lies within its operation range. Neither undervoltage nor overvoltage is present.
4. The charge pump output voltage has been accepted as good, thus it exceeded VCP_{CPGOOD}.
5. No overtemperature shutdown has occurred.
6. /COAST is high

If a short circuit is detected by one of the sense inputs S1 to S3, the output drivers will be switched off after a blanking time t_{SC} of typically 6 µs and the output DG1 will be flagged (see also Section 3.8 “Short Circuit Detection and Short Circuit Comparator Reference Input” on page 11). The output drivers will be enabled again and DG1 will be cleared with a rising edge at one of the control inputs IL1 to IL3, or falling edge at one of the control inputs /IH1 to /IH3.

Additional logic prevents short circuits due to switching on one power-NMOS transistor while the opposite one in the same branch is switched on already.

Table 3-1. Status of the Output Drivers Depending on the Control Inputs

Mode	Control Inputs IL(1..3)	Control Inputs /IH(1..3)	/COAST	Driver Stage for External Power MOS L(1..3), H(1..3)	Comments
Sleep	X	X	X	OFF	Sleep Mode
Active	X	X	0	OFF	Coast function active
Active	0	1	1	OFF	
Active	1	1	1	L(1..3) ON, H(1..3) OFF	
Active	0	0	1	L(1..3) OFF, H(1..3) ON	
Active	1	0	1	OFF	Shoot-through protection

3.8 Short Circuit Detection and Short Circuit Comparator Reference Input

Short circuits in the motor bridge circuitry are sensed by S1 to S3 inputs. Internal comparators monitor the voltage differences between the drain and the source terminals of the external power-NMOS transistors and compare it to voltage V_{SCREF} applied at pin SCREF. If one transistor switches on and its drain-source voltage exceeds V_{SCREF} threshold after a blanking time t_{SC} (see Figure 3-8 on page 12), a short circuit in this branch will be detected. In this case, the short-circuit detected output will be switched off immediately and pin DG1 will be set to HIGH. With a rising edge at any of the pins IL1 to IL3 or a falling edge at any of the pins /IH1 to /IH3, the diagnostic output DG1will be reset and the drivers switched on again.

Note, valid voltage range for short-circuit reference is $0.5V \le V_{SCREF} \le 3.3V$. Voltages outside this range will lead to incorrect short circuit thresholds. If pin SCREF is floating V_{SCREF} will be set to approximately 2.5V by an integrated resistive voltage divider.

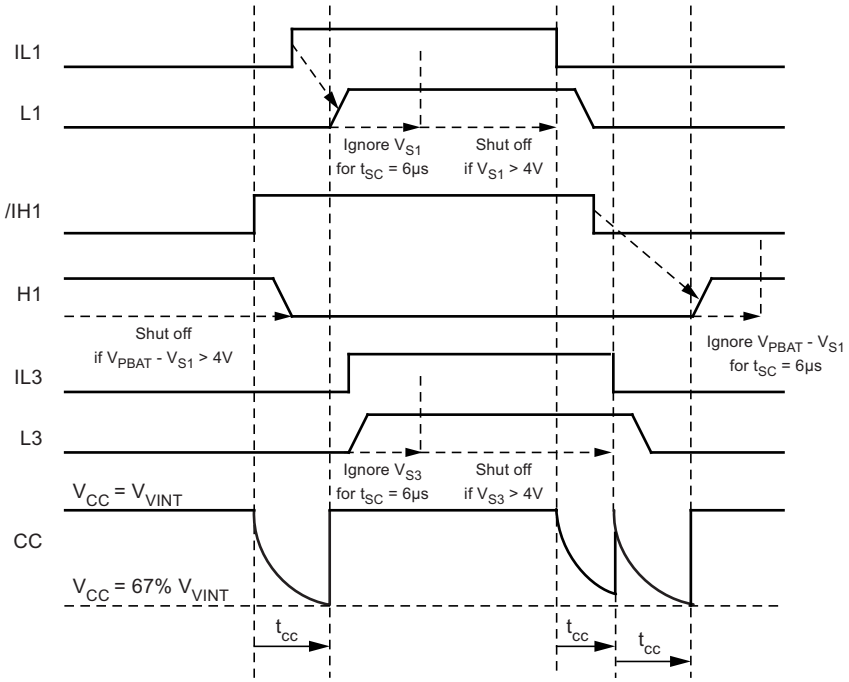
3.9 Cross Conduction Timer

In order to prevent damage of the motor bridge due to peak currents a non-overlapping phase for switching the power-NMOS transistors is mandatory. Therefore, a cross conduction timer has been implemented to prevent switching on any output driver for a time t_{CC} after any other driver has been switched off. This also accounts for toggling any other driver after a short circuit was detected. An external RC parallel combination defines the value for t_{CC} and can be estimated as follows:

$t_{CC} = K_{CC} \times R_{CC}\ (k\Omega) \times C_{CC}\ (nF)$, K_{CC} is specified in Section 8. “Electrical Characteristics” on page 16.

The RC combination is connected between CC and GND pins. When one of the drivers has been switched off the RC combination is charged to 5V (VINT) and discharged with its time constant. Any low to high transition at IL1 to IL3 or any high to low transition at /IH1 to IH3 will be masked out at the driver outputs until the voltage at CC pin drops below 67% of its initial value (VINT). The timer will be re-triggered at any time by any falling edge at the control inputs. This is shown in the following figure.

Figure 3-8. Interaction of Short Circuit Detection and Cross Conduction Timer



At least 5kΩ minimum and 5nF at maximum should be used as values for the RC combination. 10kΩ is recommended. If the non-overlapping phase is controlled by the external microcontroller, it is possible to do without the external capacitor. The minimum time t_{CC} is defined by the parasitic capacitance at CC pin.

3.10 Diagnostic Outputs DG1 - DG3

As mentioned in the sections above, the diagnostic outputs DG1 to DG3 are used to signal failures. This is summarized in the following table.

Note: This is only valid for VCC > $V_{tHRESHLow}$. Otherwise all diagnostic outputs will be tristated.

Table 3-2. Status of the Diagnostic Outputs (Normal Operation)

Device Status					Diagnostic Outputs			
CPOK	OT1	OV	UV	SC	DG1	DG2	DG3	Comments
0	X	X	X	X	–	1	–	Charge pump failure
X	1	X	X	X	–	–	1	Overtemperature prewarning
X	X	1	X	X	–	1	–	Overvoltage
X	X	X	1	X	–	1	–	Undervoltage
X	X	X	X	1	1	–	–	Short circuit

Note: X represents: no effect)
OT1: overtemperature warning
OV: overvoltage of PBAT
UV: undervoltage of PBAT
SC: short circuit
CPOK: charge pump OK

In order to differentiate between LIN and EN wake-up, DG1 output will be set to LOW or HIGH respectively. LOW indicates wake-up by LIN, HIGH indicates wake-up by EN. DG1 output will be cleared by the first valid watchdog trigger after wake-up or by the first rising edge at IL1 to IL3 if the watchdog is disabled or by the first falling edge at /IH1 to /IH3if the watchdog is disabled.

Table 3-3. Indicating Wake-up Source

Diagnostic Outputs			Wake-up Source
DG1	DG2	DG3	
1	–	–	EN
0	–	–	LIN

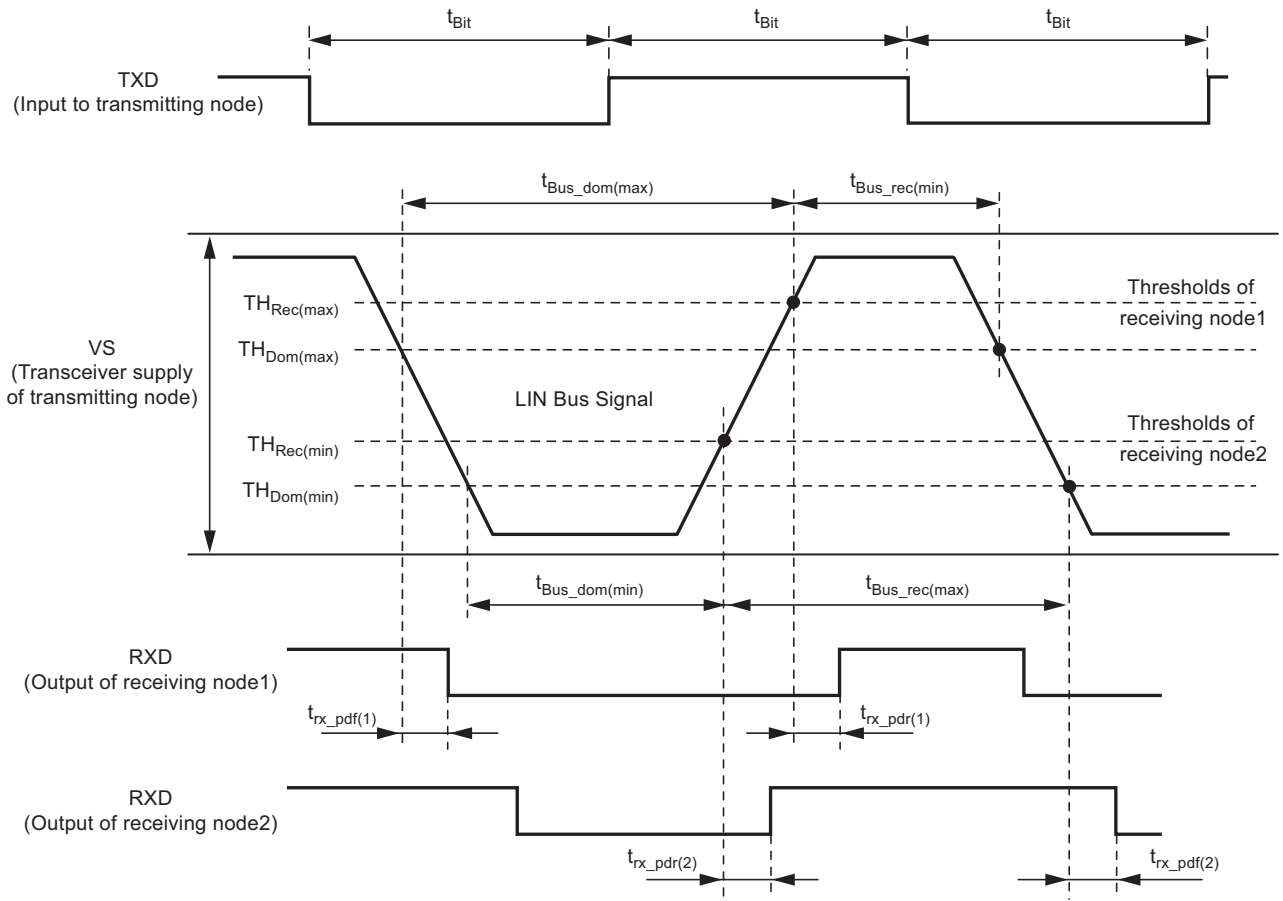
3.11 LIN Transceiver

Atmel® ATA6843 and Atmel ATA6844 include a fully integrated LIN transceiver complying with LIN specification 2.1 and SAEJ2602 2. The transceiver consists of a low-side driver with slew rate control, wave shaping, current limiting, and a high voltage comparator followed by a debouncing unit in the receiver.

During transmission, the data applied at pin TXD will be transferred to the bus driver to generate a bus signal on LIN pin. TXD input has an internal pull-up resistor.

To minimize the electromagnetic emission of the bus line, the bus driver has a built-in slew rate control and wave-shaping unit. The transmission will be aborted by a thermal shutdown or by a transition to Sleep Mode.

Figure 3-9. Definition of Bus Timing Parameters



The recessive BUS level is generated from the integrated 30kΩ pull-up resistor in series with an active diode. This diode protects against reverse currents on the bus line in case of a voltage difference between the bus line and VSUP ($V_{BUS} > V_{SUP}$). No additional termination resistor is necessary to use the IC as a LIN slave. If this IC is used as a LIN master, the LIN pin is terminated by an external 1 kΩ resistor in series with a diode to VBAT.

As PWM communication directly over the LIN transceiver in both directions is possible, there is no TXD timeout feature implemented in the LIN transceiver.

4. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

All voltages are referenced to pin GND. (xxx) Values for the Atmel® ATA6844.

Parameters	Pin	Symbol	Min.	Max.	Unit
Input voltage	PGND	V_{PGND}	–0.3	+0.3	V
Negative input current	VBAT	IVBAT	–15		mA
Negative input current	PBAT	IPBAT	–20		mA
Supply voltage	VBAT	V_{VBAT}		+40	V
Supply voltage	PBAT	V_{PBAT}		+40	V
Logic output voltage	/RESET, DG1, DG2, DG3, RXD	$V_{/RESET}$, V_{DG1}, V_{DG2}, V_{DG3}, V_{RXD}	–0.3	V_{VCC} + 0.3	V
Logic input voltage	IL1-3, /IH1-3, WD, WDD, SLEEP, TXD	V_{IL1-3}, $V_{/IH1-3}$, V_{WD}, V_{SLEEP}, V_{TXD}	–0.3	V_{VCC} + 0.3	V
Output voltage	VINT, VCC	V_{INT}, V_{VVCC}	–0.3	+5.5	V
Analog input voltage	RWD, CC, SCREF	V_{RWD} , V_{CC}, V_{SCREF}	–0.3	V_{VCC} + 0.3	V
Digital input voltage	EN	V_{EN}	–0.3	V_{VBAT} + 0.3	V
Digital input voltage	VMODE	V_{VMODE}	–0.3	V_{VINT} + 0.3	V
Output voltage	VG	V_{VG}		+16	V
Input voltage	LIN	V_{VLIN}	–27	V_{VBAT} + 2	V
Output voltage	S1, S2, S3	V_{S1}, V_{S2}, V_{S3}	(–6)	+40	V
Output voltage	L1, L2, L3	V_{L1}, V_{L2}, V_{L3}	V_{PGND} – 0.3	V_{VG} + 0.3	V
Output voltage	H1, H2, L3	V_{H1}, V_{H2}, V_{H3}	$V_{S1, 2, 3}$ – 1	$V_{S1, 2, 3}$ + 16	V
Charge pump	CPLO1, 2	V_{CPLO1}, V_{CPLO2}		V_{PBAT} + 0.3	V
Charge pump	CPHI1, 2	V_{CPHI1}, V_{CPHI2}		V_{CPOUT} + 0.3	V
Output voltage	CPOUT	V_{CPOUT}		+52	V
Storage temperature		$T_{Storage}$	–55	+150	°C
Reverse current	CPLOx, CPHIx, VG, CPOUT, Sx	I_{CPLOx_R}, I_{CPHIx_R}, I_{VG_R}, I_{CPOUT_R}, I_{Sx_R}	–2		mA
	Lx, Hx	I_{Lx_R}, I_{Hx_R}	–1		mA

Note: Estimated values take T_J > 150°C into account.

5. Thermal Resistance

Parameters	Symbol	Value	Unit
Thermal resistance junction to heat slug	R_{thjc}	< 5	K/W
Thermal resistance junction to ambient when heat slug is soldered to PCB	R_{thja}	25	K/W

6. Operating Range

The operating conditions define the limits for functional operation and parametric characteristics of the device. Functionality outside these limits is not implied unless otherwise stated explicitly. (xxx) Values for the Atmel® ATA6844

Parameters	Symbol	Min	Max	Unit
Operating supply voltage(1)	V_{VBAT}	5.5	V_{THOV}	V
Operating supply voltage(2)	V_{VBAT}	4.3	5.5	V
Operating supply voltage(3)	V_{VBAT}	V_{THOV}	40	V
Ambient temperature range	T_A	–40	+150	°C
Junction temperature range	T_J	–40	+150 (200)	°C

Notes: 1. Full functionality
2. Output drivers are switched off, extended range for parameters for voltage regulators
3. Output drivers and charge pump are switched off

7. Noise and Surge Immunity, ESD and Latch-up

Parameters	Standard and Test Conditions	Value
Conducted interferences	ISO 7637-1	Level 4(1)
Conducted disturbances	CISP25	Level 5
ESD according to IBEE LIN EMC - Pins LIN, PBAT, VBAT - Pin EN (33kΩ serial resistor)	Test specification 1.0 following IEC 61000-4-2	 ±6kV ±5kV
ESD HBM with 1.5kΩ/100pF	ESD- STM5.1-2001 JESD22-A114E 2007 CEI/IEC 60749-26: 2006 AEC-Q100-002-Ref_D	±2kV
ESD HBM with 1.5kΩ/100pF Pins EN, LIN, PBAT, VBAT against GND	ESD- STM5.1-2001 JESD22-A114E 2007 CEI/IEC 60749-26: 2006 AEC-Q100-002-Ref_D	±8kV
ESD CDM (field induced method)	ESD STM5.3.1 - 1999	±500V

Note: 1. Test pulse 5: $V_{bat\ max}$ = 40V

Static latch-up tested according to AEC-Q100-004 and JESD78.

- 3 to 6 samples, 0 failures
- Electrical post-stress testing at room temperature

In test, the voltage at the pins VBAT, LIN, CP, VBATSW, Hx, and Sx must not exceed 45V when not able to drive the specified current.

8. Electrical Characteristics

All parameters given are valid for 5.5V ≤ V_{VBAT} ≤ V_{THOVLO} and for –40°C ≤ T_J ≤ 150°C (200°C) unless stated otherwise. All values refer to PIN GND. (xxx) Values for the Atmel® ATA6844.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	Power Supply and Supervisor Functions								
1.1	Current consumption V_{VBAT}	V_{VBAT} = 13.5V(1)	46	I_{VBAT}			7	mA	A
1.3	Current consumption V_{VBAT} in Standby Mode	V_{VBAT} = 13.5V	46	I_{VBAT}			65	µA	A
1.4	Current consumption V_{PBAT} in Standby Mode	V_{PBAT} = 13.5V	38	I_{VPBAT}	9.0		20.0	µA	A
1.5	Internal power supply	V_{VBAT} > 7V	2	V_{VINT}	4.7	5.0	5.3	V	A
1.6	Overvoltage lock-out threshold		38	V_{THOVLO}	32.0		34.0	V	A
1.7	Overvoltage hysteresis		38	V_{TOVhys}	1.5		2.5	V	A
1.8	Undervoltage lock-out threshold		38	V_{THUVRC}	4.75		5.25	V	A
1.9	Undervoltage threshold hysteresis		38	V_{TUVhys}	0.2		0.4	V	A
1.11	Thermal prewarning set			$T_{JPW\ set}$	120 (170)	145 (195)	170 (220)	°C	B
1.12	Thermal prewarning reset			$T_{JPW\ reset}$	105 (155)	130 (180)	155 (205)	°C	B
1.13	Thermal prewarning hysteresis			ΔT_{JPW}		15		°C	B
1.14	Thermal shutdown off			$T_{J\ switch\ off}$	150 (200)	175 (225)	200 (250)	°C	B
1.15	Thermal shutdown on			$T_{J\ switch\ on}$	135 (185)	160 (210)	185 (235)	°C	B
1.16	Thermal shutdown hysteresis			$\Delta T_{J\ switch\ off}$		15		°C	B
1.17	Ratio thermal shutdown off/thermal prewarning set			$T_{J\ switch\ off}$/ $T_{JPW\ set}$	1.05	1.15			B
1.18	Ratio thermal shutdown on/thermal prewarning reset			$T_{J\ switch\ on}$/ $T_{JPW\ reset}$	1.05	1.15			B
2	5V/3.3V Regulator								
2.1	Regulated output voltage	V_{MODE} = V_{INT}, 7V < V_{BAT} < 40V V_{MODE} = GND, 5.5V < V_{BAT} < 40V I_{Load} = 0 to 100mA	44	V_{VCC}	4.85 3.20		5.15 3.40	V	A
2.2	Regulated output voltage	V_{MODE} = V_{INT}, 7V < V_{BAT} < 40V V_{MODE} = GND, 5.5V < V_{BAT} < 40V I_{Load} = 0 to 80mA 150°C < T_J < 200°C	44	V_{VCC}	4.85 3.20		5.15 3.40	V	A
2.3	Regulated output voltage	V_{MODE} = V_{INT}, 5.5V < V_{BAT} < 7V V_{MODE} = GND, 5V < V_{BAT} < 5.5V I_{Load} = 0 to 60mA	44	V_{VCC}	4.50 2.97		5.15 3.40	V	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

8. Electrical Characteristics (Continued)

All parameters given are valid for 5.5V ≤ V_{VBAT} ≤ V_{THOVLO} and for –40°C ≤ T_J ≤ 150°C (200°C) unless stated otherwise. All values refer to PIN GND. (xxx) Values for the Atmel® ATA6844.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
2.4	Regulated output voltage	V_{MODE} = V_{INT}, 5.5V < V_{BAT} < 7V V_{MODE} = GND, 5V < V_{BAT} < 5.5V I_{Load} = 0 to 50mA 150°C < T_J < 200°C	44	V_{VCC}	4.50 2.97		5.15 3.40	V	A
2.5	Line regulation	V_{MODE} = V_{INT}, 7V < V_{BAT} < 40V V_{MODE} = GND, 5.5V < V_{BAT} < 40V I_{Load} = 50mA, –40°C < T_J < 150°C	44				50 50	mV	A
2.6	Load regulation	V_{MODE} = V_{INT}, V_{BAT} > 7V V_{MODE} = GND, V_{BAT} > 5.5V I_{Load} = 0 to 100mA I_{Load} = 0 to 80mA, 150°C < T_J < 200°C	44				50 50	mV	A
2.7	Output current limit	V_{MODE} = V_{INT}, V_{BAT} > 7V V_{MODE} = GND, V_{BAT} > 5.5V I_{Load} at RESET	44	I_{OS1}	100 100		360 360	mA	A
2.8	Output current limit	V_{MODE} = V_{INT}, V_{BAT} > 7V V_{MODE} = GND, V_{BAT} > 5.5V I_{Load} at RESET, 150°C < T_J < 200°C	44	I_{OS1}	70 70		360 360	mA	C
2.12	HIGH threshold VMODE		1	$V_{VMODE\ H}$			4.0	V	A
2.13	LOW threshold VMODE		1	$V_{VMODE\ L}$	0.7			V	A
3	Reset and Watchdog								
3.1	V_{CC} threshold voltage level for /RESET	VMODE = VINT (VMODE = GND)	5	$V_{tHRESHLow}$	3.8 2.5		4.2 2.8	V	A B
3.2	Hysteresis	VMODE = VINT (VMODE = GND)	5	HYS_{RESth}	0.2 0.13		0.6 0.4	V	A B
3.3	Length of pulse at /RESET		5	t_{res}	8		12	ms	A
3.4	Length of short pulse at /RESET		5	$t_{resshort}$	1.6		2.4	ms	A
3.5	Wait for the first WD trigger		5	t_d	400		600	ms	A
3.6	Time for VCC < V_{tHRESL} before activating /RESET		5	$t_{delayRESL}$			2	µs	C
3.8	Watchdog oscillator period	R_{RWD} = 33kΩ ±1%	(5)	T_{OSC}	11.09		13.55	µs	A
3.12	Close window		(5)	t1		980 × T_{OSC}			A
3.13	Open window		(5)	t2		780 × T_{OSC}			A
3.14	Output low-level at pin /RESET	I_{OLRES} = 1mA	5	V_{OLRES}			0.4	V	A
3.15	Internal pull-up resistor at pin /RESET		5	R_{PURES}	5	10	15	kΩ	D

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

8. Electrical Characteristics (Continued)

All parameters given are valid for 5.5V ≤ V_{VBAT} ≤ V_{THOVLO} and for –40°C ≤ T_J ≤ 150°C (200°C) unless stated otherwise. All values refer to PIN GND. (xxx) Values for the Atmel® ATA6844.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
4	LIN Transceiver								
4.1	Low-level output current	Normal mode; V_{LIN} = 0V, V_{RXD} = 0.4V	22	IL_{RXD}	2			mA	D
4.2	High-level output current	Normal mode; V_{LIN} = V_{BAT} V_{RXD} = V_{CC} – 0.4V	22	IH_{RXD}			–2	mA	D
4.3	Driver recessive output voltage	V_{TXD} = V_{CC}; I_{LIN} = 0mA	13	V_{BUSrec}	0.9 × VBAT			V	A
4.4	Driver dominant voltage $V_{BUSdom\_DRV\_LoSUP}$	V_{VBAT} = 7.3V R_{load} = 500Ω	13	$V_{\_LoSUP}$			1.2	V	A
4.5	Driver dominant voltage $V_{BUSdom\_DRV\_HiSUP}$	V_{VBAT} = 18V R_{load} = 500Ω	13	$V_{\_HiSUP}$			2	V	A
4.6	Driver dominant voltage $V_{BUSdom\_DRV\_LoSUP}$	V_{VBAT} = 7.3V R_{load} = 1000Ω	13	$V_{\_LoSUP\_1k}$	0.6			V	A
4.7	Driver dominant voltage $V_{BUSdom\_DRV\_HiSUP}$	V_{VBAT} = 18V R_{load} = 1000Ω	13	$V_{\_HiSUP\_1k\_}$	0.8			V	A
4.8	Pull up resistor to VS	Serial diode required	13	R_{LIN}	20		47	kΩ	A
4.9	Current limitation	V_{BUS} = V_{BAT_max}	13	I_{BUS_LIM}	50		200	mA	A
4.10	Input leakage current at the receiver including pull-up resistor as specified	Input leakage current driver off V_{BUS} = 0V V_{BAT} = 12V	13	$I_{BUS\_PAS\_dom}$	–1			mA	A
4.11	Leakage current LIN recessive	Driver off 8V < V_{BAT} < 18V 8V < V_{BUS} < 18V V_{BUS} = V_{BAT}	13	$I_{BUS\_PAS\_rec}$			20	µA	A
4.12	Leakage current at ground loss Control unit disconnected from ground Loss of local ground must not affect communication in the residual network	GND_{Device} = VS V_{BAT} = 12V 0V < V_{BUS} < 18V	13	$I_{BUS\_NO\_gnd}$	–1		+1	mA	A
4.13	Node has to sustain the current that can flow under this condition. Bus must remain operational under this condition	V_{BAT} disconnected V_{SUP_Device} = GND 0V < V_{BUS} < 18V	13	I_{BUS}			100	µA	A
4.14	Center of receiver threshold	V_{BUS_CNT} = (V_{th_dom} + V_{th_rec})/2	13	V_{BUS_CNT}	0.475 × V_{VBAT}	0.5 × V_{VBAT}	0.525 × V_{VBAT}	V	A
4.15	Receiver dominant state	V_{EN} = 5V	13	V_{BUSdom}			0.4 × V_{VBAT}	V	A
4.16	Receiver recessive state	V_{EN} = 5V	13	V_{BUSrec}	0.6 × V_{VBAT}			V	A
4.17	Receiver input hysteresis	V_{HYS} = V_{th_rec} – V_{th_dom}	13	V_{BUShys}			0.175 × V_{VBAT}	V	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

8. Electrical Characteristics (Continued)

All parameters given are valid for 5.5V ≤ V_{VBAT} ≤ V_{THOVLO} and for –40°C ≤ T_J ≤ 150°C (200°C) unless stated otherwise. All values refer to PIN GND. (xxx) Values for the Atmel® ATA6844.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
4.18	Duty cycle 1	7V < V_{VBAT} < 18V $TH_{rec(max)}$ = 0.744 × V_{VBAT} $TH_{Dom(max)}$ = 0.581 × V_{VBAT} t_{Bit} = 50µs D1 = $t_{Bus\_rec(min)}$/(2 × t_{Bit}) Load1: 1nF + 1kΩ Load2: 10nF + 500Ω	13	D1	0.396				A
4.19	Duty cycle 2	7V < V_{VBAT} < 18V $TH_{rec(min)}$ = 0.422 × V_{VBAT} $TH_{Dom(min)}$ = 0.284 × V_{VBAT} t_{Bit} = 50µs D2 = $t_{Bus\_rec(max)}$/(2×t_{Bit}) Load1: 1nF + 1kΩ Load2: 10nF + 500Ω	13	D2			0.581		A
4.20	Duty cycle 3	7V < V_{VBAT} < 18V $TH_{rec(max)}$ = 0.778 × V_{VBAT} $TH_{Dom(max)}$ = 0.616 × V_{VBAT} t_{Bit} = 96µs D3 = $t_{Bus\_rec(min)}$/(2 × t_{Bit}) Load1: 1nF + 1kΩ Load2: 10nF + 500Ω	13	D3	0.417				A
4.21	Duty cycle 4	7V < V_{VBAT} < 18V $TH_{rec(max)}$ = 0.389 × V_{VBAT} $TH_{Dom(max)}$ = 0.251 × V_{VBAT} t_{Bit} = 96µs D4 = $t_{Bus\_rec(min)}$/(2 × t_{Bit}) Load1: 1nF + 1kΩ Load2: 10nF + 500Ω	13	D4			0.590		A
4.22	Receiver propagation delay	7V < V_{VBAT} < 18V t_{rec_pd} = max(t_{rx_pdr}, t_{rx_pdf})	22	t_{rx_pd}			6	µs	A
4.23	Symmetry of receiver propagation delay rising edge minus falling edge	7V < V_{VBAT} < 18V t_{rx_sym} = t_{rx_pdr} – t_{rx_pdf}	22	t_{rx_sym}	–2		+2	µs	A
4.24	Dominant time for wake-up via LIN Bus	V_{LIN} = 0V	13	T_{BUS}	30	90	150	µs	A
4.25	Monitoring time for wake-up over LIN Bus		13	T_{mon}	6	10	15	ms	B
4.26	Pre-wake detection LIN Low-Level Input Voltage	Switches the LIN receiver on	13	V_{LINL}	–27		V_{VBAT} – 3.3	V	A
4.27	Pre-wake detection LIN High-Level Input Voltage		13	V_{LINH}	V_{VBAT} – 2		V_{VBAT} + 0.3	V	A
4.28	LIN Pre-Wake pull-up current	V_{VBAT} < 27V V_{LIN} = 0V	13	$I_{LINWake}$	–30	–10		µA	A
4.29	Capacitance on LIN Pin to GND		13	C_{LIN}			10	pF	D

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

8. Electrical Characteristics (Continued)

All parameters given are valid for 5.5V ≤ V_{VBAT} ≤ V_{THOVLO} and for –40°C ≤ T_J ≤ 150°C (200°C) unless stated otherwise. All values refer to PIN GND. (xxx) Values for the Atmel® ATA6844.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
5	Control Inputs WD, WDEN, SLEEP, TXD, IL1-3, /IH1-3, /COAST								
5.1	Input low-level threshold		6-8, 15-21, 48	V_{IL}			0.3 × V_{VCC}	V	A
5.2	Input high-level threshold		6-8, 15-21, 48	V_{IH}	0.7 × V_{VCC}			V	A
5.3	Hysteresis		6-8, 15-21, 48	HYS	0.3				C
5.4	Pull-down resistor	WD, SLEEP, IL1-3	6, 8, 16, 18, 20	R_{PD}	25	50	100	kΩ	A
5.5	Pull-up resistor	WDEN, TXD, /IH1-3, /COAST	7, 15, 17, 19, 21, 48	R_{PU}	25	50	100	kΩ	A
5.7	Debounce time SLEEP		8	$t_{gotosleep}$	9	10	11	µs	A
6	Charge Pump								
6.1	Charge pump voltage	V_{VBAT} > 7V $I_{LoadCPOUT}$ = 0A I_{LoadVG} = 0A $C_{CP1,2}$ = 47nF C_{CPOUT} = 220nF	32	V_{CPOUT}	V_{VBAT} + 11V		V_{VBAT} + 18	V	A
6.2	Charge pump voltage	V_{VBAT} > 7V $I_{LoadCPOUT}$ = 7.5mA, I_{LoadVG} = 0A $C_{CP1,2}$ = 47nF C_{CPOUT} = 220nF	32	V_{CPOUT}	V_{VBAT} +10V			V	A
6.3	Period charge pump oscillator			T_{CP}		2.5		µs	B
6.4	Charge pump output voltage for active drivers		32	VCP_{CPGOOD}	5.25		8.0	V	A
7	VG Regulator								
7.1	VG Regulator Output Voltage	V_{BAT} = 13.5V V_{CPOUT} = 20V I_{LoadVG} = 7.5mA	39	V_{VG}	11	12.5	14	V	A
7.2	VG Regulator Line Regulation	V_{BAT} = 13.5V V_{CPOUT1} = 20V, V_{CPOUT2} = 35V I_{LoadVG} = 7.5mA	39	ΔV_{VG_Line}			100	mV	A
7.3	VG Regulator Load Regulation	V_{BAT} = 13.5V V_{CPOUT} = 25V $I_{LoadVG1}$ = 1mA, $I_{LoadVG2}$ = 60mA	39	ΔV_{VG_Load}			100	mV	A
8	H-bridge Driver								
8.1	Low-side driver HIGH output voltage		40-42	V_{LxH}			V_{VG}	V	D
8.2	ON-resistance of sink stage of pins Lx	ILX = 100mA	40-42	R_{DSON_LxL}			20	Ω	A
8.3	ON-resistance of source stage of pins Lx	ILX = 100mA	40-42	R_{DSON_LxH}			20	Ω	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

8. Electrical Characteristics (Continued)

All parameters given are valid for 5.5V ≤ V_{VBAT} ≤ V_{THOVLO} and for –40°C ≤ T_J ≤ 150°C (200°C) unless stated otherwise. All values refer to PIN GND. (xxx) Values for the Atmel® ATA6844.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
8.6	Sink resistance between Lx and GND		40-42 to 43	R_{Lxsink}	45	75	115	kΩ	A
8.7	ON-resistance of sink stage of pins Hx	V_{Sx} = 0V	26, 28, 30	R_{DSON_HxL}			20	Ω	A
8.8	ON-resistance of source stage of pins Hx	V_{Sx} = V_{VBAT} I_{Hx} = 100mA	26, 28, 30	R_{DSON_HxH}			20	Ω	A
8.13	Output voltage low level pins Hx	V_{Sx} = 0V I_{Hx} = 1mA	26, 28, 30	V_{HxL}			0.3	V	A
8.14	Output voltage high level pins Hx	I_{Hx} = –100µA	26, 28, 30	$V_{HxHstat}$	V_{VCPOUT} – 1V		V_{VCPOUT}	V	A
8.15	Sink resistance between Hx and Sx		26-31	R_{Hxsink}	45	75	115	kΩ	A
8.16	Sink resistance between Sx and GND		27, 29, 31, 38	R_{Sxsink}		1		MΩ	D
	Dynamic Parameters								
8.17	Propagation delay time, low-side driver from high to low		40-42	t_{LxHL}			0.9	µs	A
8.18	Propagation delay time, low-side driver from low to high		40-42	t_{LxLH}			0.9	µs	A
8.19	Fall time low-side driver	V_{VBAT} = 13.5V C_{Gx} = 5nF	40-42	t_{Lxf}			0.3	µs	A
8.20	Rise time low-side driver	V_{VBAT} = 13.5V C_{Gx} = 5nF	40-42	t_{Lxr}			0.3	µs	A
8.21	Propagation delay time, high-side driver from high to low		26, 28, 30	t_{HxHL}			0.9	µs	A
8.22	Propagation delay time, high-side driver from low to high		26, 28, 30	t_{HxLH}			0.9	µs	A
8.23	Fall time high-side driver	V_{VBAT} = 13.5V, C_{Gx} = 5nF	26, 28, 30	t_{Hxf}			0.3	µs	A
8.24	Rise time high-side driver	V_{VBAT} = 13.5V, C_{Gx} = 5nF	26, 28, 30	t_{Hxr}			0.3	µs	A
8.25	Valid Short circuit detection voltage range		9	V_{SCREF}	0.5		3.3	V	A
8.26	Accuracy Short circuit detection voltage	0.5V ≤≤ V_{SCREF} ≤≤ 3.3V	9, 27, 29, 31	V_{SCREF}	–10		+10	%	A
8.27	Default Short Circuit detection voltage		9	V_{SCREF_DEF}		2.5		V	C
8.28	Internal resistor to GND		9	Ri_{GND}	80	100	120	kΩ	A
8.29	Internal resistor to VBAT		9	Ri_{VBAT}	80	100	120	kΩ	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

8. Electrical Characteristics (Continued)

All parameters given are valid for 5.5V ≤ V_{VBAT} ≤ V_{THOVLO} and for –40°C ≤ T_J ≤ 150°C (200°C) unless stated otherwise. All values refer to PIN GND. (xxx) Values for the Atmel® ATA6844.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
8.30	Short circuit blanking time			t_{SC}	5.4	6	6.6	µs	A
	Cross Conduction Timer								
8.31	Cross conduction time constant			K_{CC}	0.345	0.405	0.465		B
9	Input EN								
9.1	Input low level threshold		47	V_{IL}	2.3		3.6	V	A
9.2	Input high level threshold		47	V_{IH}	2.8		4.0	V	A
9.3	Hysteresis		47	HYS		0.47		V	C
9.4	Pull-down resistor		47	R_{PD}	50	100	200	kΩ	A
9.5	Debounce time		47	t_{db}	10	20	25	µs	A
10	Diagnostic Outputs DG1, DG2, DG3								
10.1	Low level output current	V_{DG} = 0.4V	23-25	IL	2			mA	A
10.2	High level output current	V_{DG} = VCC – 0.4V	23-25	IH			–2	mA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

9. Application

This section describes the principal application for which the Atmel® ATA6843/ATA6844 was designed.

Figure 9-1. Typical Application

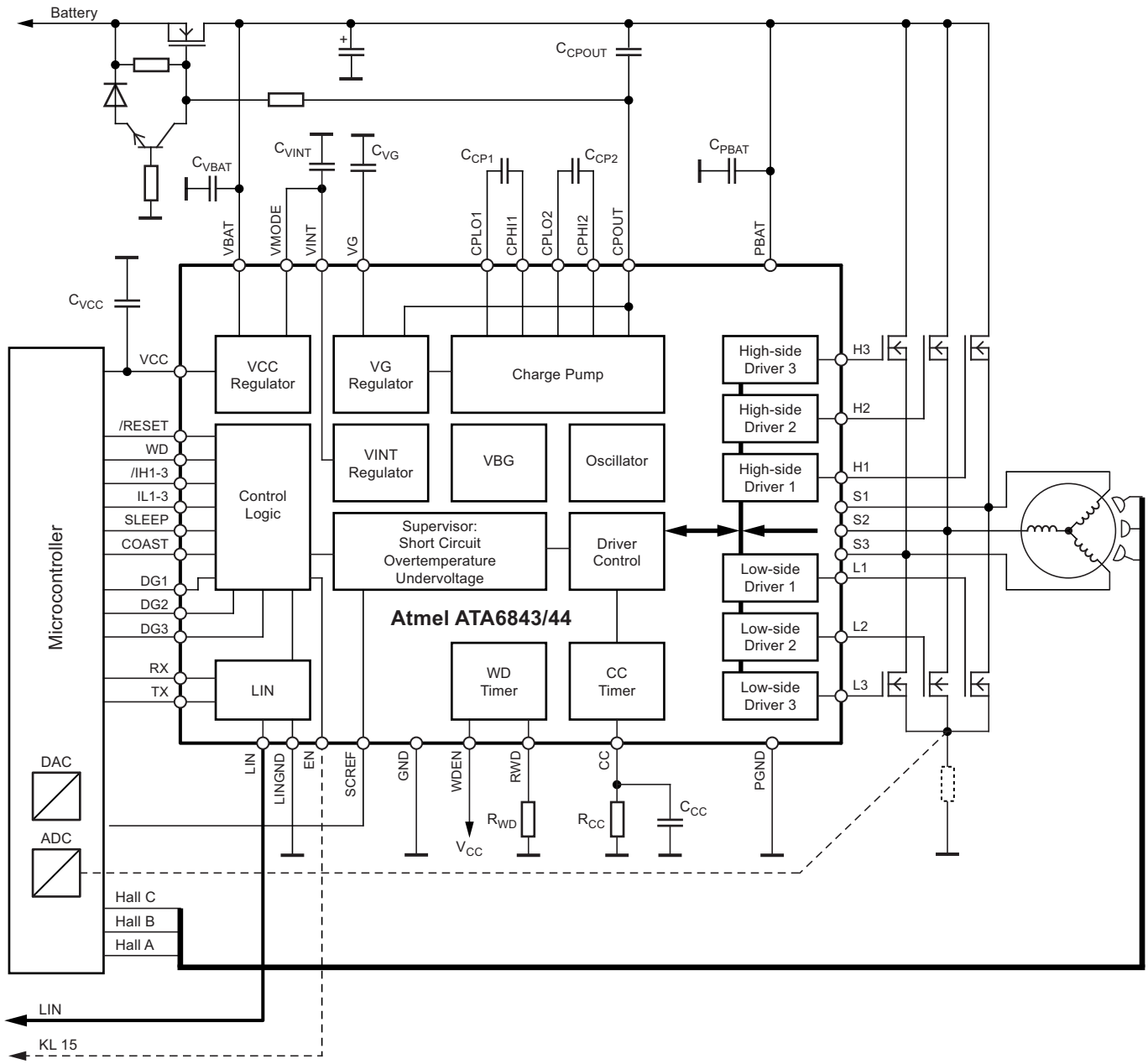


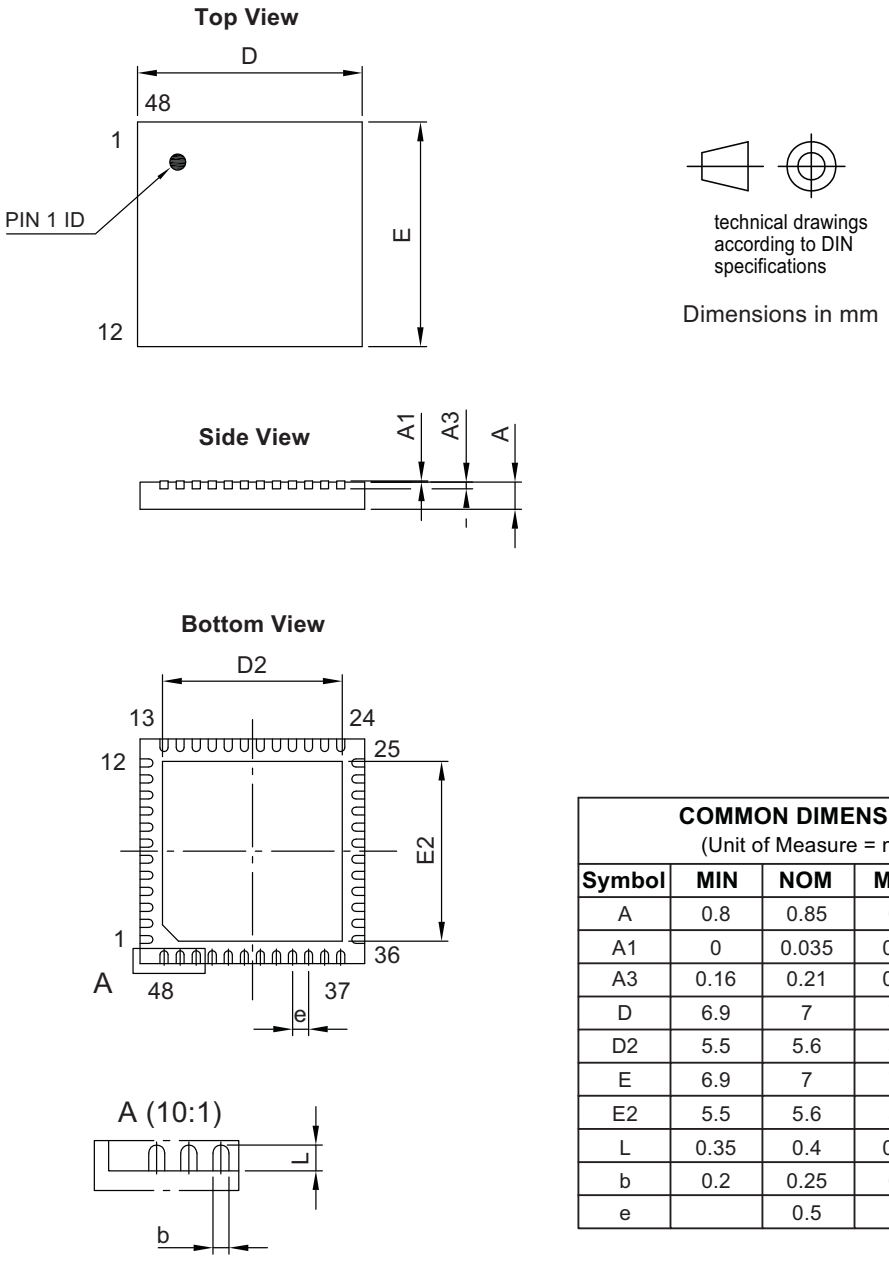
Table 9-1. Typical External Components

Component	Function	Min.	Typical	Max.
CVINT	Blocking capacitor at VINT	100nF	220nF/10V	470nF
C_{VCC}	Blocking capacitor at VCC	1.5µF		10µF
ESL (C_{VCC})	Serial inductance to C_{VCC} including PCB	1nH		20nH
ESR (C_{VCC})	Serial resistance to C_{VCC} including PCB	2Ω		15Ω
CVG	Blocking capacitor at VG	220nF	470nF, 25V	1µF
CCP1	Charge pump shuffle capacitor	47nF	100nF/25V	220nF
CCP2	Charge pump shuffle capacitor	47nF	100nF/25V	220nF
CCPOUT	Charge pump reservoir capacitor	470nF	15 × CCPx/25V	3.3µF
RRWD	Resistor defining internal bias currents for watchdog oscillator	10kΩ	33 kΩ	91kΩ
RCC	Cross conduction time definition resistor	5kΩ	10kΩ	
CCC	Cross conduction time definition capacitor		330pF	5nF
C_{VBAT}	Blocking capacitor VBAT		100nF	
C_{PBAT}	Blocking capacitor PBAT		100nF	

10. Ordering Information

Extended Type Number	Package	Remarks
ATA6843-PLQW-1	QFN48	Pb-free, 4k
ATA6844-PLQW-1	QFN48	Pb-free, 4k

11. Package Information



COMMON DIMENSIONS (Unit of Measure = mm)				
Symbol	MIN	NOM	MAX	NOTE
A	0.8	0.85	0.9	
A1	0	0.035	0.05	
A3	0.16	0.21	0.26	
D	6.9	7	7.1	
D2	5.5	5.6	5.7	
E	6.9	7	7.1	
E2	5.5	5.6	5.7	
L	0.35	0.4	0.45	
b	0.2	0.25	0.3	
e		0.5		

05/20/14

Package Drawing Contact: packagedrawings@atmel.com	TITLE	GPC	DRAWING NO.	REV.
	Package: QFN_7x7_48L Exposed pad 5.6x5.6		6.543-5188.03-4	1