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Atmel

ATA6870N

Li-Ion, NiMH Battery Measuring, Charge Balancing and Power-supply Circuit

DATASHEET

Features

- 12-bit battery-cell voltage measurement
- Simultaneous battery cells measurement in parallel
- Cell temperature measurement
- Charge Balancing Capability
  - Parallel balancing of cells possible
- Integrated power supply for MCU
- Undervoltage detection
- Less than 10µA standby current
- Low cell imbalance current (< 10µA)
- Hot plug-in capable
- Interrupt timer for cycling MCU wake-ups
- Cost-efficient solution due to cost-optimized 30V CMOS technology
- Reliable communication between stacked ICs due to level shifters with current sources and checksum monitoring of data
- Daisy-chainable
  - Each IC monitors up to 6 battery cells
  - 16 ICs (96 cells) per string
  - No limit on number of strings
- Package QFN48 7mm ×7mm

Applications

- Battery measurement, supply and monitoring IC for Li-ion and NiMH battery systems in Electric (EV) and Hybrid Electrical (HEV) Vehicles
- Electrical and hybrid electrical vehicles
- Li-Ion batteries as 12V lead-acid battery replacement
- Ebike, scooters
- Uninterruptible power supply (UPS)
- Smart grid

Benefits

- Cost reduction due to integrated measurement circuit and high voltage power-supply

1. Description

The Atmel® ATA6870N is a measurement and monitoring circuit designed for Li-ion and NiMH multicell battery stacks in hybrid electrical vehicles.

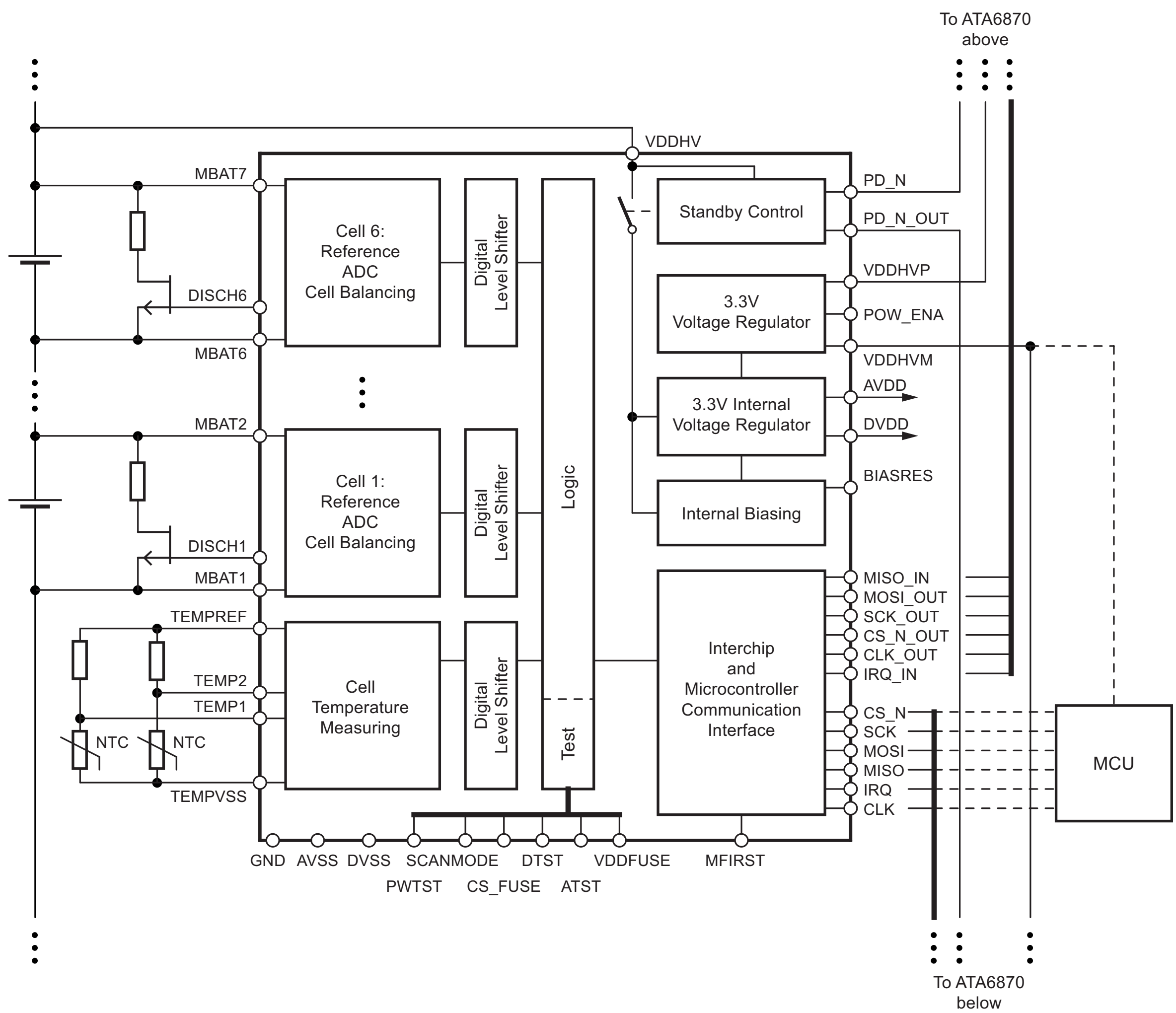
The Atmel ATA6870N monitors the battery-cell voltage and the battery-cell temperature with a 12-bit ADC.

The circuit also provides charge-balancing capability for each battery-cell.

In addition, a linear regulator is integrated to supply a microcontroller or other external components. Reliable communication between stacked ICs is achieved by level-shifters with current sources. The Atmel ATA6870N can be connected to three, four, five or six battery-cells. Up to 16 circuits (96 cells) can be cascaded in one string. The number of strings is not limited.

2. Block Diagram

Figure 2-1. Block Diagram



3. Pin Configuration

Figure 3-1. Pinning QFN48, 7 mm ×7 mm

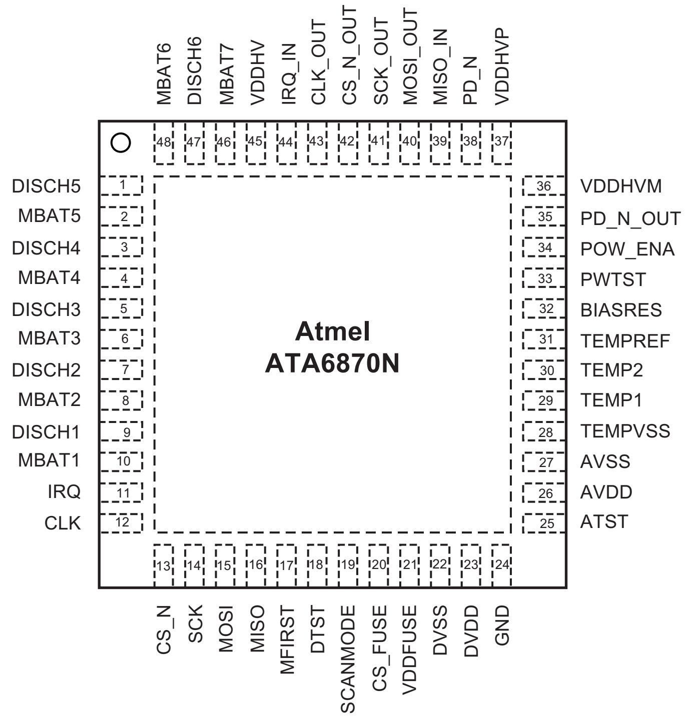


Table 3-1. Pin Description

Pad Number	Pad Name	Function	Remark
Exposed Pad		Heatslug	
1	DISCH5	Output to drive external cell-balancing transistor	
2	MBAT5	Battery cell sensing line	
3	DISCH4	Output to drive external cell-balancing transistor	
4	MBAT4	Battery cell sensing line	
5	DISCH3	Output to drive external cell-balancing transistor	
6	MBAT3	Battery cell sensing line	
7	DISCH2	Output to drive external cell-balancing transistor	
8	MBAT2	Battery cell sensing line	
9	DISCH1	Output to drive external cell-balancing transistor	
10	MBAT1	Battery cell sensing line	
11	IRQ	Interrupt output for MCU/ATA6870N below	
12	CLK	System clock	
13	CS_N	Chip select input from MCU/ATA6870N below	
14	SCK	SPI clock input from MCU/ATA6870N below	
15	MOSI	Master Out Slave In input from MCU	SPI data input

Table 3-1. Pin Description (Continued)

Pad Number	Pad Name	Function	Remark
16	MISO	Master In Slave Out output for MCU	SPI data output
17	MFIRST	Select Master/Slave	
18	DTST	Test-mode pin	Keep pin open (output)
19	SCANMODE	Test-mode pin	Connected to VSSA
20	CS_FUSE	Test-mode pin	Connected to VSSA
21	VDDFUSE	Test-mode pin	Connected to VSSA
22	DVSS	Digital negative supply	
23	DVDD	Digital positive supply input (3.3V)	Connected to AVDD
24	GND	Ground	
25	ATST	Test-mode pin	Keep pin open (output)
26	AVDD	3.3V Regulator output	
27	AVSS	Analog negative supply	
28	TEMPVSS	Ground for temperature measuring	
29	TEMP1	Temperature measuring input 1	
30	TEMP2	Temperature measuring input 2	
31	TEMPREF	Reference voltage for temperature measuring	
32	BIASRES	Internal supply current adjustment	
33	PWTST	Test - mode pin	Keep pin open (output)
34	POW_ENA	Power regulator enable/disable	
35	PD_N_OUT	Power down output	
36	VDDHVM	Power regulator output to supply e.g. an external microcontroller	
37	VDDHVP	Power regulator supply voltage	
38	PD_N	Power down input	
39	MISO_IN	Master In Slave Out input from ATA6870N above	
40	MOSI_OUT	Master Out Slave In output for ATA6870N above	
41	SCK_OUT	SPI clock output for input of ATA6870N above	
42	CS_N_OUT	Chip select output for input of ATA6870N above	
43	CLK_OUT	System clock output for input of ATA6870N above	
44	IRQ_IN	Interrupt input from ATA6870N above	
45	VDDHV	Supply voltage	
46	MBAT7	Battery cell sensing line	
47	DISCH6	Output to drive external cell-balancing transistor	
48	MBAT6	Battery cell sensing line	

4. ATA6870N System Overview

The Atmel® ATA6870N can be stacked up to 16 times in one string. The communication with MCU is carried out on the lowest level through an SPI bus. The data on the SPI bus is transmitted to the 15 other Atmel ATA6870Ns using the communication interface implemented inside Atmel ATA6870N.

Figure 4-1. Battery Management Architecture with One Battery String

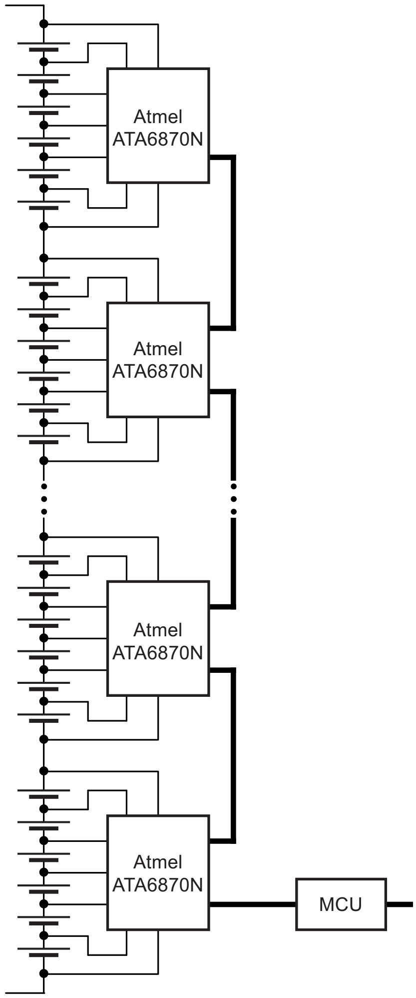
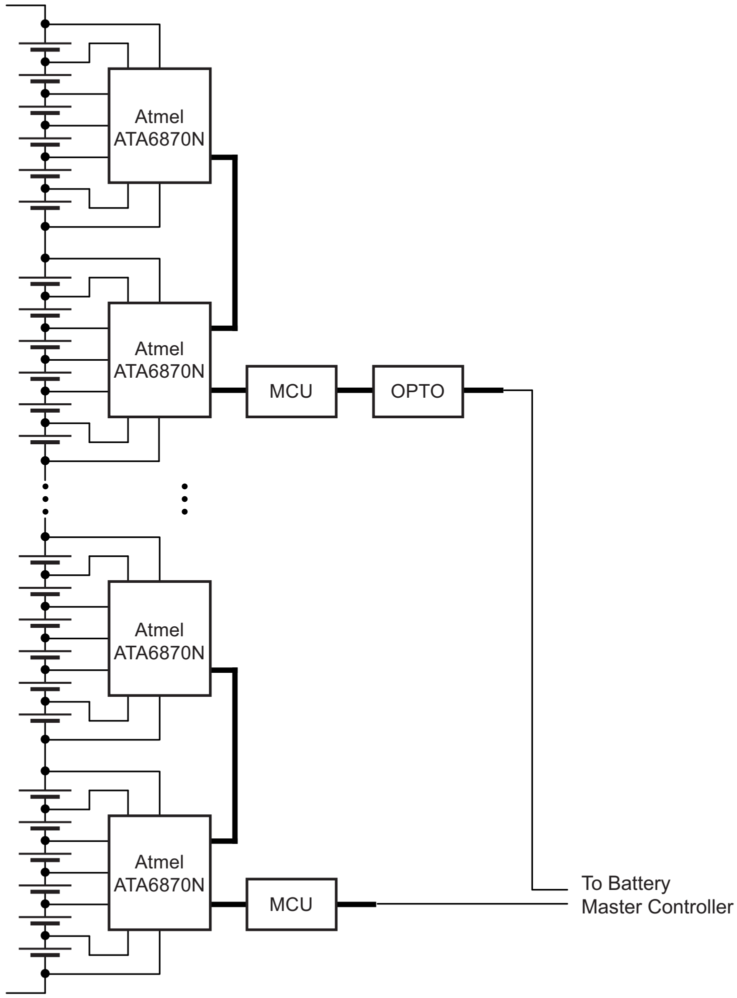


Figure 4-2. Battery Management Architecture with Several Battery Strings



5. Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Unless otherwise specified all voltages to pin VSSA.

Parameters	Pin	Symbol	Min.	Max.	Unit
Ambient temperature		T_A	–40	+85	°C
Junction temperature		T_J	–40	+125	°C
Storage temperature		T_S	–55	+150	°C
Battery cell voltage	MBAT(i+1), MBAT(i)	$V_{MBAT(i+1)}$ - $V_{MBAT(i)}$	–0.3	+5.5	V
V_{VDDHV} - V_{VMBAT7}max		V_{VDDHV} - V_{VMBAT7}	–5.5	+0.3	V
V_{MBAT1}	MBAT1	V_{MBAT1}	–0.3	+0.3	V
Supply voltage power regulator	VDDHVP	V_{VDDHVP}	–0.3	+33.6	V
Operating supply voltage	VDDHV	V_{VDDHV}	–0.3	+30	V
Supply voltage DVDD (regulator is off)	DVDD	V_{DVDD}	–0.3	+5.5	V
Supply voltage AVDD (regulator is off)	AVDD	V_{AVDD}	–0.3	+5.5	V
Test-input	VDDFUSE	$V_{VDDFUSE}$	–0.3	+5.5	V
Reference voltage for temperature measuring (regulator is Off)	TEMPREF	$V_{TEMPREF}$	–0.3	VDD+0.3	V
Supply voltage VDDHVM (regulator is Off)	VDDHVM	V_{VDDHVM}	–0.3	+5.5	V
Digital ground	DVSS	V_{AVSS} - V_{GND}	–0.3	+0.3	V
Analog ground	AVSS	V_{AVSS} - V_{GND}	–0.3	+0.3	V
Digital/analog ground	AVSS, DVSS	V_{AVSS} - V_{DVSS}	–0.3	+0.3	V
Ground voltage for temperature measuring	TEMPVSS	$V_{TEMPVSS}$	–0.3	+0.3	V
Input voltage for logic I/O pins	CLK, CS_N, SCK, MOSI, DTST, ATST, SCANMODE, MFIRST, POW_ENA, CS_FUSE, PWTST	V_{CLK}, V_{CS_N}, V_{SCK}, V_{MOSI}, V_{DTST}, V_{ATST}, $V_{SCANMODE}$, V_{MFIRST}, V_{POW_ENA}, V_{CS_FUSE}, V_{PWTST}	–0.3	VDD + 0.3	V
	IRQ, MISO	V_{IRQ}, V_{MISO}	–0.3	+5.5	V
Input voltage for analog I/O pins	TEMP1, TEMP2, BIASRES	V_{TEMP1}, V_{TEMP2}, $V_{BIASRES}$	–0.3	VDD + 0.3	V
Input voltage for digital high voltage input pins	MISO_IN, IRQ_IN	V_{MISO_IN}, V_{IRQ_IN}	VDDHV – 0.3	VDDHV + 0.3	V
Voltage at digital high voltage output pins	MOSI_OUT, SCK_OUT, CS_N_OUT, CLK_OUT	V_{MOSI_OUT}, V_{SCK_OUT}, $V_{CS\_N\_OUT}$, V_{CLK_OUT}	VDDHV – 0.3	VDDHV + 0.3	V
Input: PD_N	PD_N	V_{PD_N}	VDDHV – 5.5	VDDHV + 0.3	V
Output: PD_N_OUT	PD_N_OUT	$V_{PD\_N\_OUT}$	–5.5	+0.3	V
Voltage at cell balancing outputs	DISCH(i)	VDISCH(i)	$V_{MBAT(i)}$ – 0.3	$V_{MBAT(i+1)}$ + 0.3	V

5. Absolute Maximum Ratings (Continued)

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Unless otherwise specified all voltages to pin VSSA.

Parameters	Pin	Symbol	Min.	Max.	Unit
HBM ESD ANSI/ESD-STM5.1 JESD22-A114 AEC-Q100 (002)		ESD	±2		kV
CDM ESD STM 5.3.1			500		V
	1, 12, 13, 24, 25, 36, 37, 48		750		V
Latch-up acc. to AECQ100-004, JESD78A		LATCH-UP	±100		mA

6. Thermal Resistance

Parameters	Symbol	Value	Unit
Package. QFN48 7×7			
Max. thermal resistance junction-ambient[1]	R_{thja}max	20	K/W
Max. thermal resistance junction-case	R_{thjC}max	TBD	K/W

Note: 1. Package mounted on 4 large PCB (per JESD51-7) under natural convention as defined in JESD51-2.

7. Circuit Description and Electrical Characteristics

Unless otherwise specified all parameters in this section are valid for a supply voltage range of 6.9V < V_{DDHV} < 30V and a battery cell voltage of $V_{MBAT(i+1)} – V_{MBAT(i)}$ = 0V to 5V, –40°C < T_A < 85°C. All values refer to pin VSSA, unless otherwise specified.

7.1 Operating Modes

The Atmel® ATA6870N has two operation modes.

1. Power-down mode (PDmode)
2. Normal mode (NORM mode)

7.1.1 Power-down Mode

In power-down mode all blocks of the IC are switched off.

The circuit can be switched from Power-down to ON mode or back via the PD_N input. If the pin is connected to VDDHV via an external optocoupler, for example, the circuit is in ON mode. If several Atmel ATA6870N are stacked, the power-down signal must be only provided for the IC on the top level of the stack. The next lower IC receives this information from the PD_N_OUT output of its upper IC. The PD_N_OUT pin must be connected to either the PD_N pin of the next lower Atmel ATA6870N or to VSSA.

Figure 7-1. Power-down

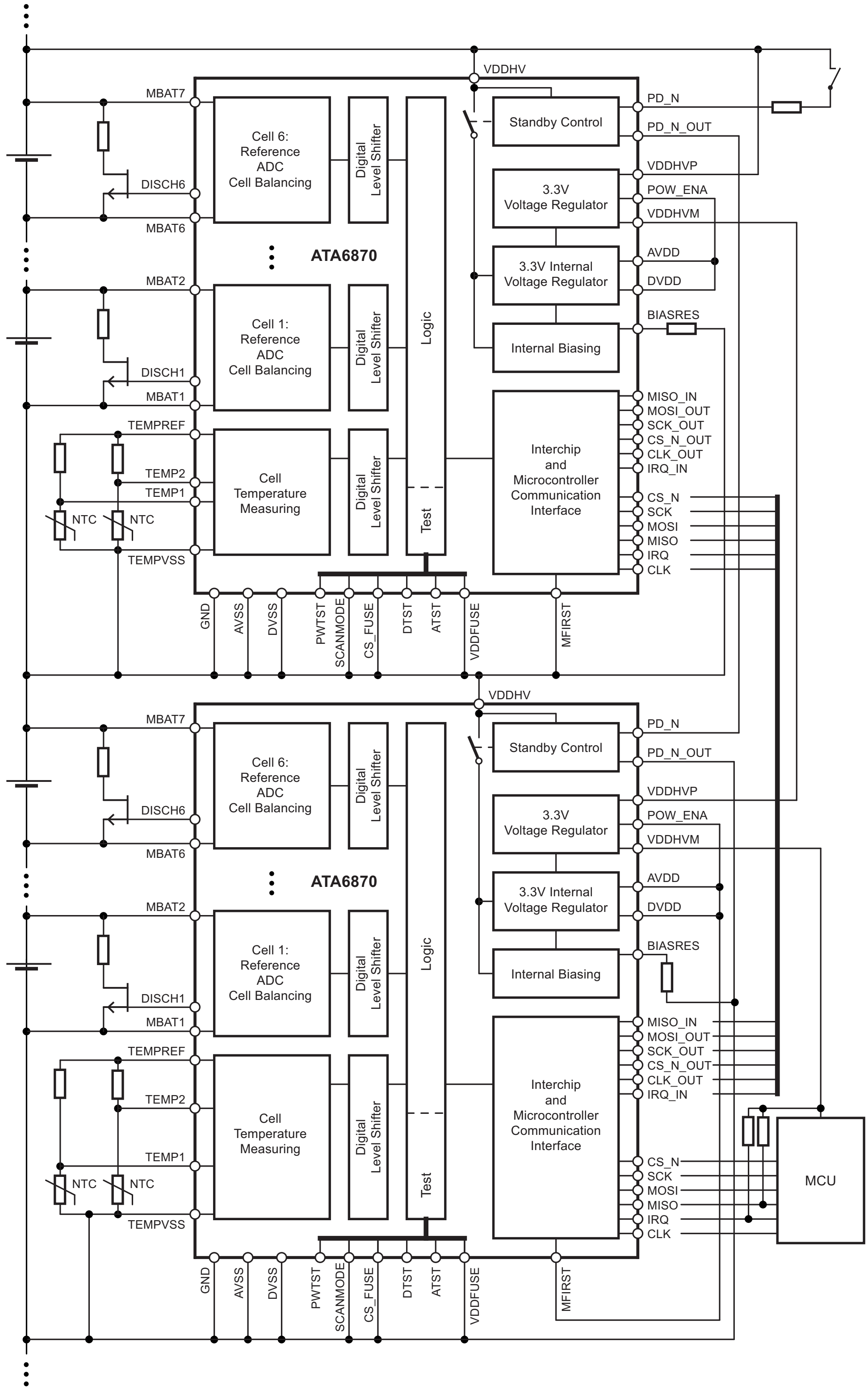


Table 7-1. Electrical Characteristics

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1.1	Maximum allowed input current in power-down mode (e.g., leakage current of an optocoupler)		PD_N	I_{PD_N}			50	µA	A
1.2	Input current in ON mode		PD_N	I_{PD_N}	2.5		5	mA	A
1.3	Maximum voltage (pin PD_N left open)	I_{PD_N} = 0 to 50µA	PD_N	$V_{VDDHV} - V_{PD\_N}$			5	V	A
1.4	Propagation delay time from power-down mode to NORM mode	min slope $I_{PD\_N} = \frac{1\ mA}{msec}$	DVDD	t_{VDDON}			3	ms	A
1.5	Propagation delay time from NORM mode to power-down mode		DVDD	t_{VDDOFF}			10	ms	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

7.1.2 Normal Operating Mode (NORM Mode)

The Atmel® ATA6870N turns on when the PD_N signal is switched from low to high. The power supplies AVDD and DVDD as well as VDDHVM (if the input signal POW_ENA = high) are turned on. The configuration registers are set to their default values. In NORM mode the Atmel ATA6870N can acquire analog data (voltage or temperature channels) upon request from the host microcontroller. When the host microcontroller orders an acquisition through the SPI bus, the IC starts digitizing all voltage and one temperature channel in parallel. The on-chip digital signal processor filters, in real time, the channel samples. When conversion and filtering are done, the data-ready interrupt to the host processor indicates the data availability. The MCU can now read the ADC result registers. The MCU reads the Atmel ATA6870N's status registers to check each IC and to acknowledge the interrupt. When Atmel ATA6870N is in NORM mode, the MCU can be active or in idle mode. In order to wake-up the MCU by an interrupt, the Low Frequency Timer (LFT) can be activated in Atmel ATA6870N. Interrupt is signaled with a high level on IRQ pin. The LFT is re-programmable on the fly and can be reset through SPI, but is not stoppable.

Figure 7-2. Atmel ATA6870N in NORM Mode

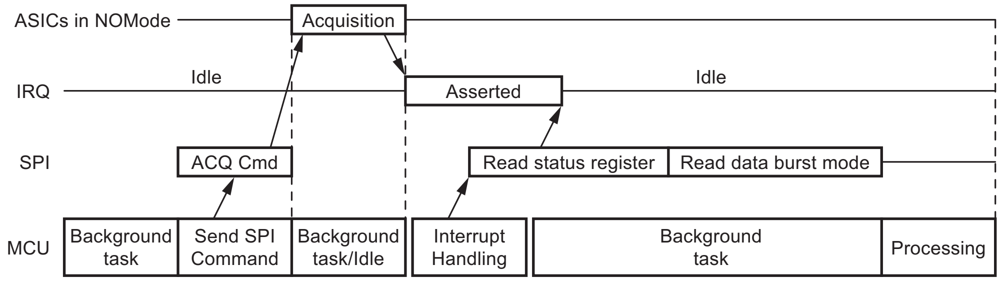


Table 7-2. Electrical Characteristics

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
2.1	Supply voltage		VDDHV	V_{VDDHV}	6.9		30	V	A
2.2	Current consumption IVDDHV (normal mode)		VDDHV	I_{VDDHV}			15	mA	A
2.3	Current consumption in power-down mode (PDmode) I_{VDDHV} + $I_{MBAT(i)}max$(1)	$V_{MBAT(i+1)}$ – $V_{MBAT(i)}$ = 3.7V	VDDHV				10	µA	A
2.4	Imbalance from battery cell to battery cell in power-down mode (PDN Mode)	$V_{MBAT(i+1)}$ – $V_{MBAT(i)}$ = 3.7V	MBAT(i+1)	$I_{MBAT(i+1)}$			10	µA	A

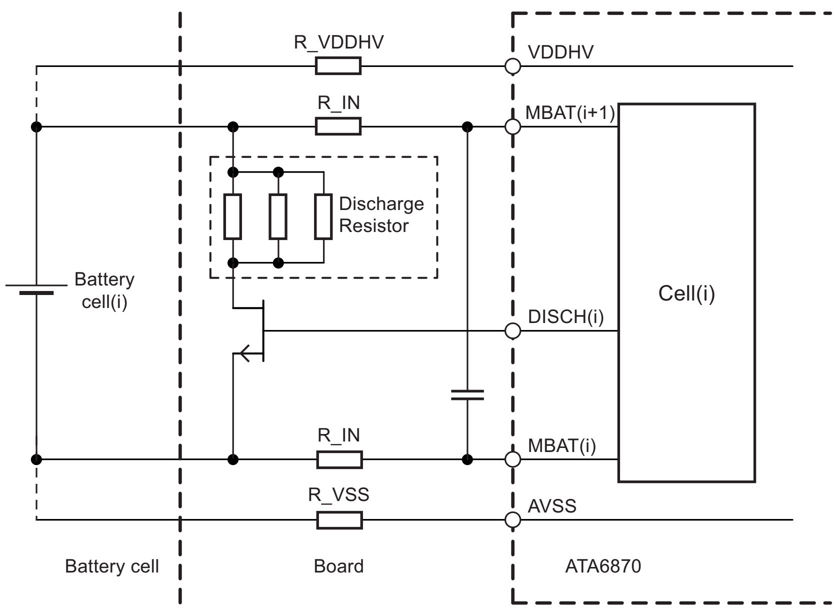
*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Largest input current of the cell inputs MBAT(i)

7.2 Interface to Battery Cells

Each input line MBAT(i) and the supply lines VDDHV, AVSS can be protected by additional resistors and a filter capacitor as shown below.

Figure 7-3. External Components between Atmel ATA6870N and the Battery Cells



$MBAT_{(i)}$ are high impedance input (~2MΩ). Thus, external components can be added to protect ATA6870N chip against current spikes and overvoltage at battery cell level.

Table 7-3. Electrical Characteristics

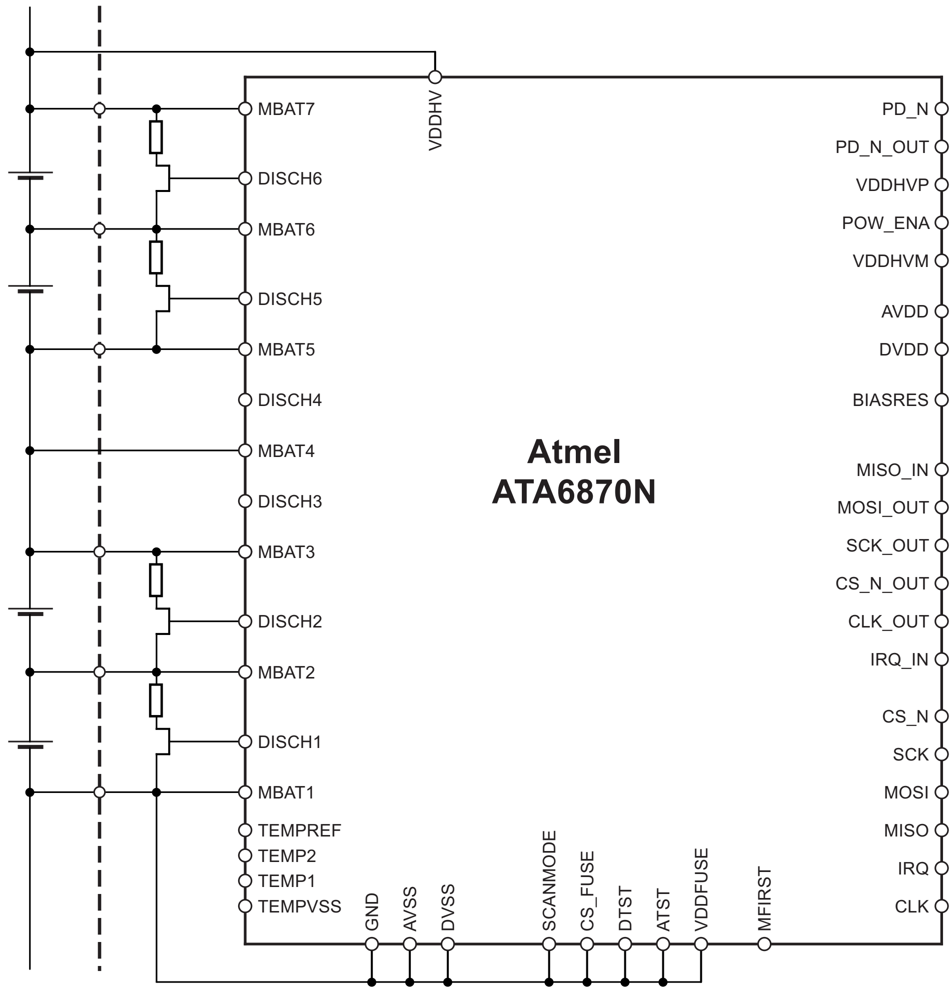
No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
3.1	R_IN		MBAT(i)				1	kΩ	D
3.2	R_VDDHV		VDDHV				50	Ω	D
3.3	R_VSS		AVSS				50	Ω	D

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

7.3 Reduced Number of Battery Cells Configuration

It is possible for Atmel® ATA6870N to operate with a reduced number of cells: 3, 4, 5, and 6 cell operation are possible. In these cases, the cell-chip inputs corresponding to the missing cells should be connected to the upper cell potential of the module.

Figure 7-4. Connection with 4 Cells only



Battery cell 1 (MBAT1, MBAT2) and battery cell 6 (MBAT6, MBAT7) must always be used for the lowest/highest cell.

7.4 ATA6870N External MCU Supply

The Atmel® ATA6870N provides a 3.3V power-supply for external components such as the microcontroller unit (MCU). The input pin for this supply is pin VDDHVP, and the output pin is VDDHVM. This regulator is able to supply the MCU directly from the topmost battery cell of a string. The power regulators of all stacked Atmel ATA6870N are therefore put in serial configuration to avoid imbalance.The regulator can be disabled with the digital input pin POW_ENA.

Table 7-4. Truth Table

Pin	Symbol	Value	Function
POW_ENA	V_{POW_ENA}	Low	Voltage regulator disabled
		High	Voltage regulator enabled

Logic levels: Low = V_{DVSS}, High = V_{DVDD}

Figure 7-5. MCU Supply with the Internal Power Supply

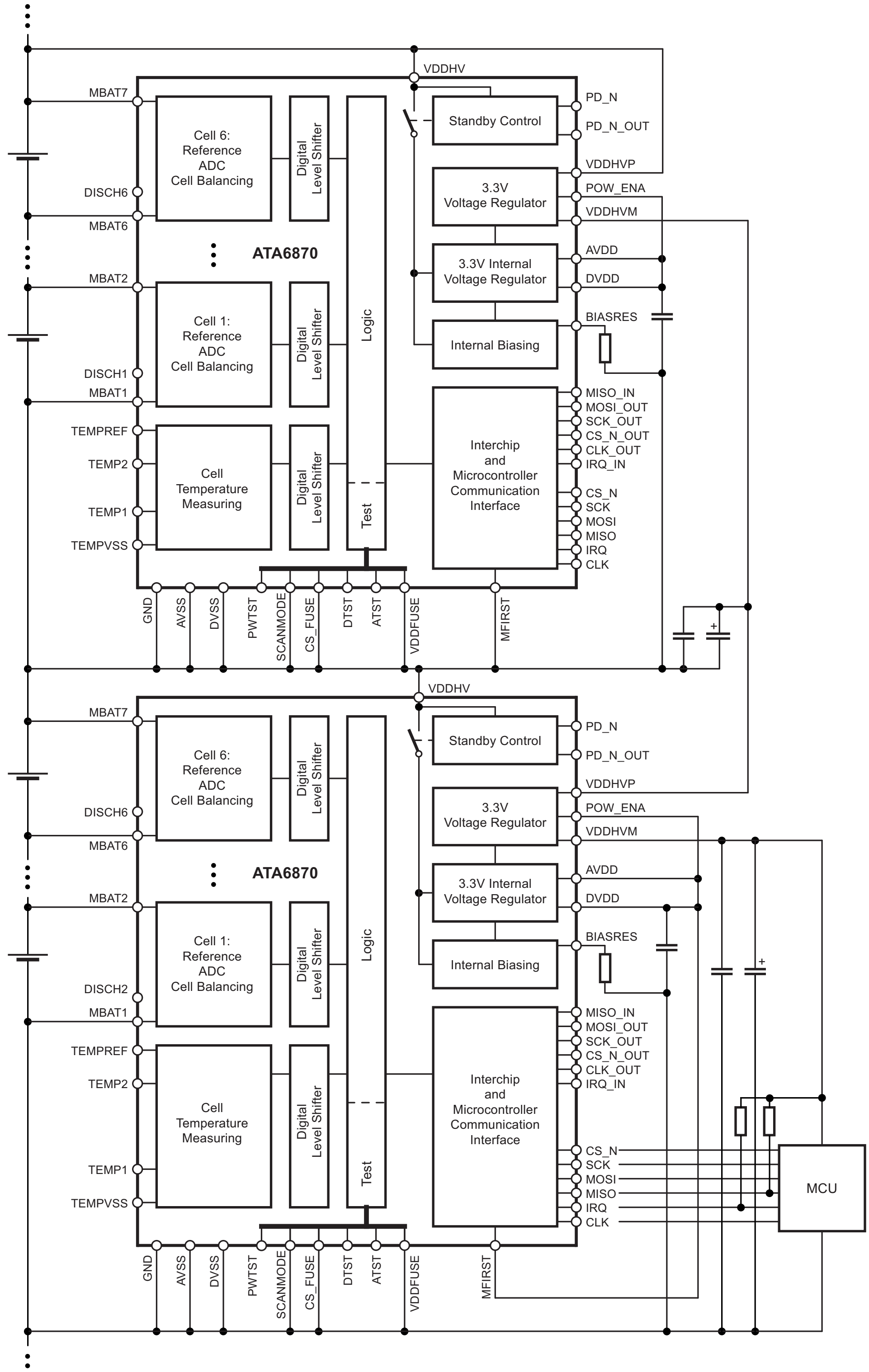


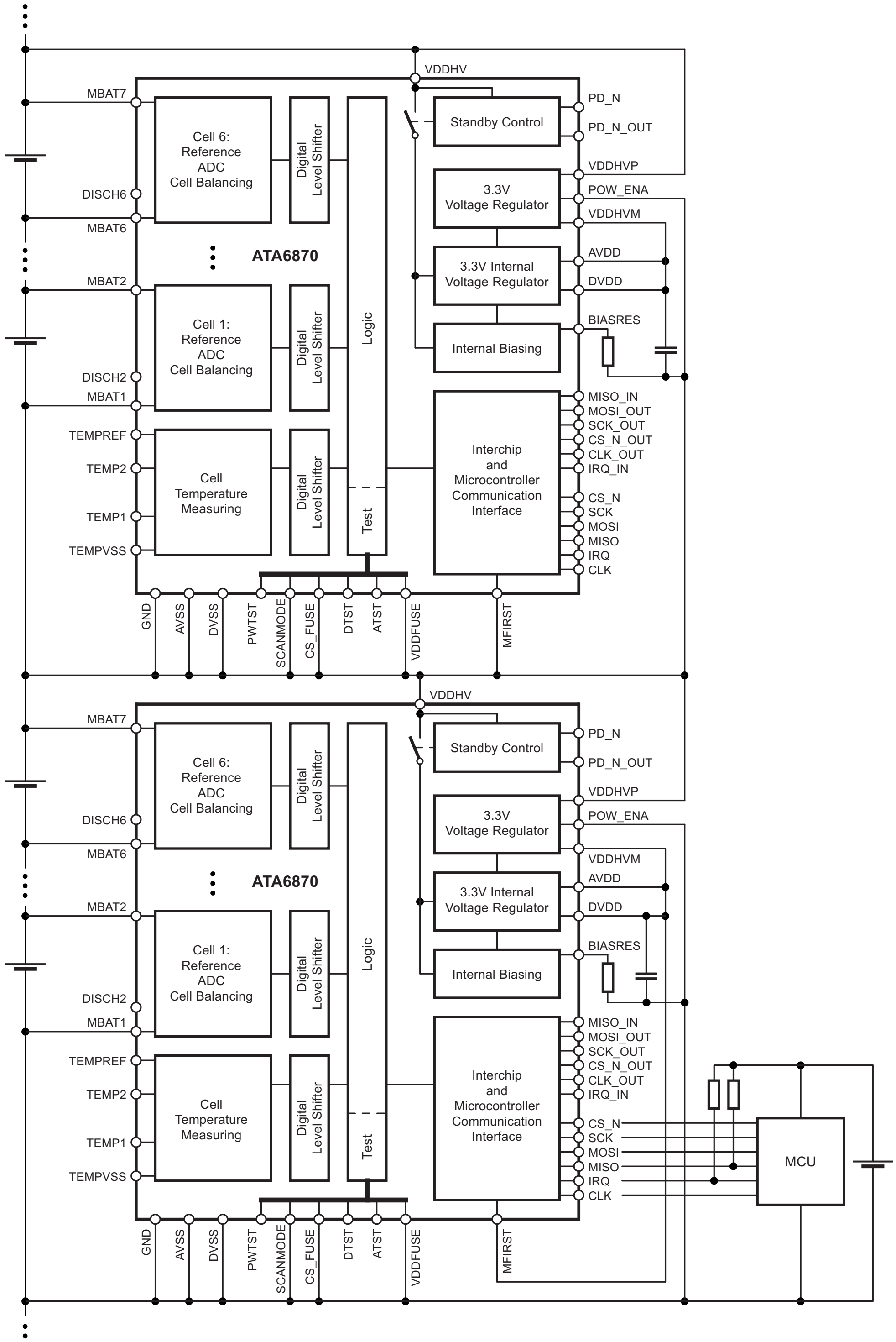
Table 7-5. Electrical Characteristics

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
4.1	Supply voltage		VDDHVP	V_{VDDHVP}	6.9		33.3	V	A
4.2	Output voltage		VDDHVM	V_{VDDHVM}	3.1	3.3	3.5	V	A
4.3	DC output current		VDDHVM	I_{VDDHVM}			20	mA	A
4.4	Peak output current(1)		VDDHVM	I_{VDDHVM}			50	mA	A
4.5	Capacitor load(2)		VDDHVM		30	33		µF	D
4.6	Capacitor load(2)		VDDHVM		200	220		nF	D
4.7	High level input voltage		POW_ENA	V_{POW_ENA}	$0.7 \times V_{DVDD}$			V	A
4.8	Low level input voltage		POW_ENA	V_{POW_ENA}			$0.3 \times V_{DVDD}$	V	A
4.9	Hysteresis		POW_ENA	V_{POW_ENA}	$0.05 \times V_{DVDD}$			V	C
4.10	Input current	V_{POW_ENA} = 0V to V_{DVDD}	POW_ENA	I_{POW_ENA}	–1		+1	µA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes: 1. Maximum current the power regulator can provide, time limited by thermal consideration only
2. These capacitors are mandatory

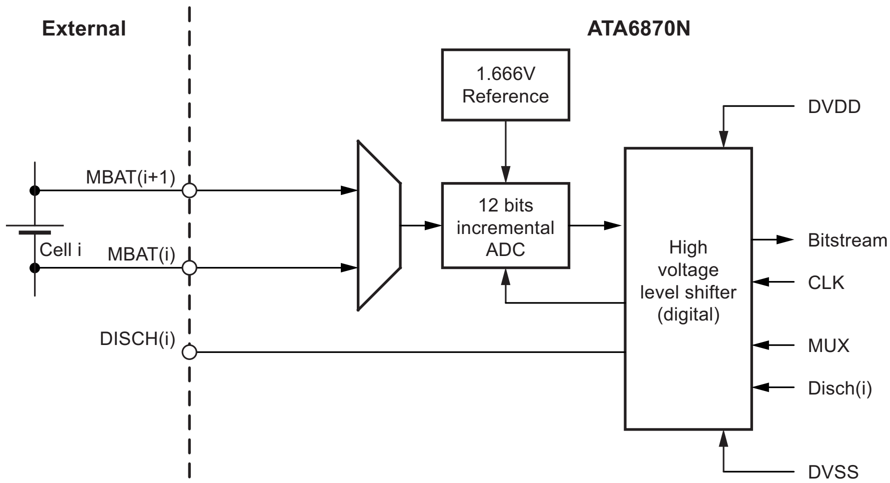
Figure 7-6. MCU Supply with an External Power Supply



7.5 Analog Blocks

7.5.1 Battery Voltage Measuring

Figure 7-7. Block Diagram Battery Voltage Measurement



The battery voltage measurement block contains

- a 2-input multiplexer
- a voltage reference,
- a 12-bit ADC
- the upper part of digital voltage level shifters

7.5.1.1 Input Multiplexer

The multiplexer has 3 inputs. Each of the functions are described in the table below:

Table 7-6. Inputs of the Multiplexer

Input	Function
$V(MBAT_{(i+1)}, MBAT_{(i)})$	Input voltage measurement
$V(MBAT_{(i)}, MBAT_{(i)})$	Offset error acquisition of ADC

The multiplexer inputs are controlled by SPI.

7.5.1.2 12 Bits Incremental ADC

The purpose of this cell is to convert an analog input into a 12-bit digital word.

Table 7-7. Electrical Characteristics

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
5.1	Accuracy of voltage channel(1)	Maximum input noise 0.5mVrms $2.2V < V_{MBAT(i+1)} - V_{MBAT(i)} < 4.5V$	MBAT(i+1), MBAT(i)		–10		+10	mV	A
		Maximum input noise 0.5mVrms $0V < V_{MBAT(i+1)} - V_{MBAT(i)} < 5V$	MBAT(i+1), MBAT(i)		–20		+20	mV	A
		Maximum input noise 0.5mVrms $V_{MBAT(i+1)} - V_{MBAT(i)} = 3.7V$ $T_J = -20°C$ to $+65°C$	MBAT(i+1), MBAT(i)		–7		+7	mV	A
		Maximum input noise 0.5mVrms Aging(3)	MBAT(i+1), MBAT(i)		–11		+11	mV	C
		Maximum input noise 0.5mVrms Aging(4)	MBAT(i+1), MBAT(i)		–17		+17	mV	C
5.2	Input voltage range		MBAT(i+1), MBAT(i)	$V_{MBAT(i+1)}$, $V_{MBAT(i)}$	0		5	V	A
5.3	Input resolution (1 LSB)			V_{LSB}		1.5		mV	D
5.4	Reference voltage			V_{Ref}		1.667		V	D
5.5	Offset voltage		MBAT(i+1), MBAT(i)	$V_{MBAT(i+1)}$, $V_{MBAT(i)}$		410		LSB	A
5.6	Gain voltage		MBAT(i+1), MBAT(i)	$V_{MBAT(i+1)}$, $V_{MBAT(i)}$		655		LSB/V	A
5.7	System clock		CLK	f_{CLK}	450	500	550	kHz	D
5.8	SPI interface clock		SCK	f_{SCK}			$0.5 \times f_{CLK}$		D
5.9	Conversion rate(2)	$t_{conv} = (2^{12} + 1) / f_{CLK}$		t_{conv}		8.194		ms	D
5.10	Input bandwidth		MBAT(i+1), MBAT(i)	f_{BW}		50		Hz	D

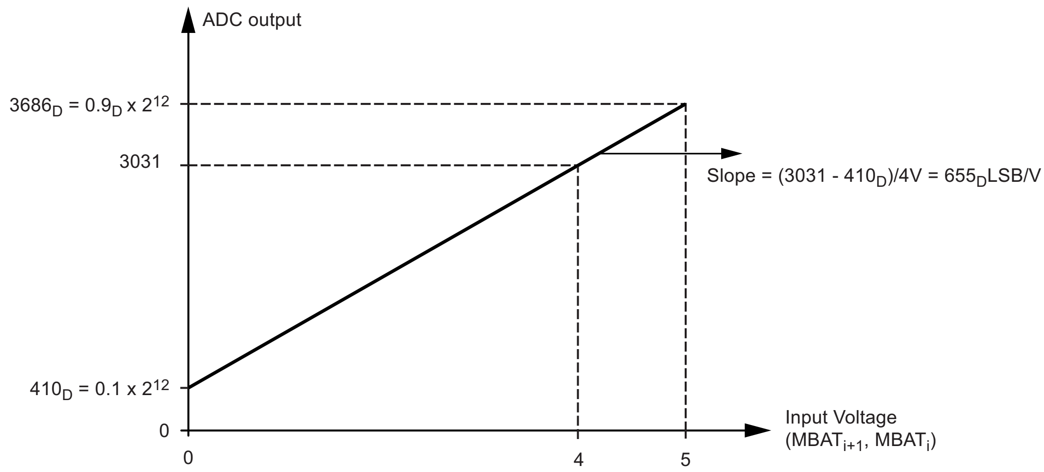
*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes:
1. The accuracy of the voltage channels is guaranteed with no external resistor in the MBAT(i), MBAT(i+1) lines.
2. Conversion rate without readout times of SPI
3. Aging temperature $T_J = 125°C$, drift measured at 25°C and 85°C
4. Aging temperature $T_J = 125°C$, drift measured at –40°C

Converting ADC Results to Voltage

The silicon is factory adjusted by measuring offset voltage (VOffset) with both ADC inputs connected to MBATi and calibration of the adc($MBAT_{i+1}$) value to 3031 at $MBAT_{i+1}$ = 4.0V (see Figure 7-8).

Figure 7-8. Characteristics of AD-converter



adc(VOffset): ADC result with both ADC inputs connected to $MBAT_i$ (0V input voltage)

adc($VMBAT_{i+1}$-$VMBAT_i$): Uncorrected ADC result of the ADC input voltage

Standard Procedure with Frequent Offset Adjustment

To use the frequent offset adjustment of the ADC the following parameters need to be measured:

adc(VOffset) ADC result with both ADC inputs connected to $MBAT_i$ (0V input voltage)
adc($VMBAT_{i+1}$-$VMBAT_i$) Uncorrected ADC result of the ADC input voltage

Calculation of the battery cell voltage:

$VIn = 4V \times (adc(VMBAT_{i+1}-VMBAT_i) - adc(VOffset)) / (3031 - adc(VOffset))$
with $VIn = V(MBAT_{i+1})-V(MBAT_i)$

It's not necessary to measure VOffset during every measuring cycle.

Regular updates are sufficient.

Standard Procedure without Offset Adjustment

With increasing input voltages the failure caused by the ADC can be ignored. In this case the battery cell voltage can be calculated by the following equation:

$\mathbf{VIn = 4V \times (adc(VMBAT_{i+1}-VMBAT_i) - 0.1 \times 2^{12}) / (3031 - 0.1 \times 2^{12})}$

The following simplification can be done with less than 1mV rounding error:

$\mathbf{VIn = 1.52656 \times 10^{-3} \times (adc(VMBAT_{i+1}-VMBAT_i) - 410)}$

7.5.1.3 Acquisition Time and Clocking

The acquisition time depends on the number of Atmel® ATA6870Ns to be addressed.

Table 7-8. Electrical Characteristics

Number of ATA6870N	SCK Frequency (kHz)	CLK Frequency (kHz)	Conversion Time (ms)	Total Acquisition Duration (ms)(1)
1	250	500	8.2	9.5
2	250	500	8.2	10.2
3	250	500	8.2	10.8
4	250	500	8.2	11.5
5	250	500	8.2	12.2
6	125	500	8.2	17.0
7	125	500	8.2	18.4
8	125	500	8.2	19.7
9	125	500	8.2	21.1
10	62.5	500	8.2	36.1
11	62.5	500	8.2	38.8
12	62.5	500	8.2	41.5
13	62.5	500	8.2	44.2
14	62.5	500	8.2	46.8
15	62.5	500	8.2	49.5
16	62.5	500	8.2	52.2

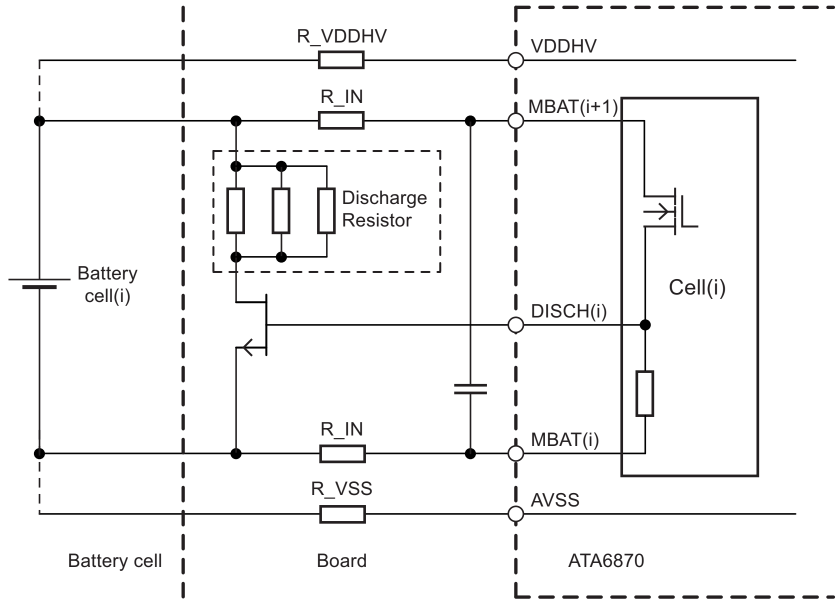
Notes: 1. The total acquisition time takes the following into account:
- ADC conversion
- Reading of voltage values in burst mode for all ATA6870N devices,
- Reading of temperature values for all ATA6870N devices (only one temperature input is read).

SPI clock (pin SCK) must a maximum of half the frequency of the system clock CLK.

7.5.2 Battery Cell Discharge

Each battery cell can be discharged with an external resistor and an NMOS transistor.

Figure 7-9. External Circuit for Cell Balancing



The pin DISCH(i) (Discharge for battery cell i) is intended to switch on the external discharge resistor in parallel to the battery cell to bypass charge current for cell balancing reasons.

The pin DISCH(i) is a digital output:

No discharge: $V_{DISCH(i)} = V_{MBAT(i)}$

Discharge: $V_{DISCH(i)} = V_{MBAT(i+1)}$

Table 7-9. Electrical Characteristics

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
6.1	Operating voltage range		MBAT(i)	$MBAT_{(i+1)} - MBAT_{(i)}$	1.5		5	V	A
6.2	High-level output voltage	$I_{DISCH(i)} = -10\mu A$, $MBAT_{(i+1)} - MBAT_{(i)}$ = 1.5V to 5V	DISCH(i)	$V_{DISCH(i)} - V_{MBAT(i)}$	$V_{MBAT(i+1)} -$ 50 mV			V	A
6.3	High-level output voltage	$I_{DISCH(i)} = -1mA$ $MBAT_{(i+1)} - MBAT_{(i)}$ = 3V to 5V	DISCH(i)	$V_{DISCH(i)} - V_{MBAT(i)}$	$V_{MBAT(i+1)} -$ 0.6V			V	A
6.4	Pull-down resistor(1)		DISCH(i)-MBAT(i)		60		140	kΩ	A

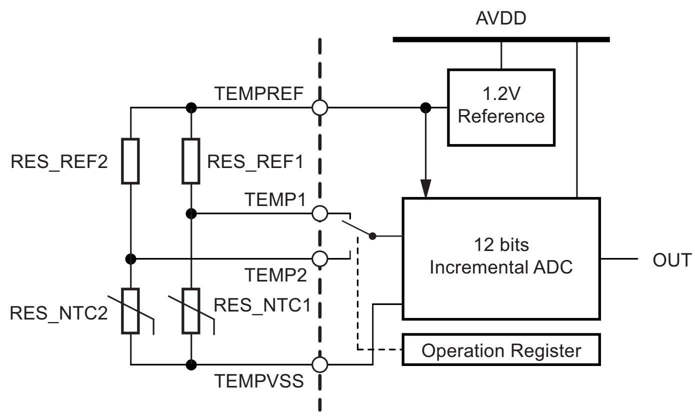
*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Integrated pull-down resistor between pins DISCH(i) and MBAT(i)

7.5.3 Temperature Channel

The temperature sensors are based on a resistor divider using a standard resistor and an NTC resistor. This resistor divider is connected to the reference of the ADC for temperature measuring. As the ADC is sharing same reference value, the output of temperature measurement with ADC is ratio metric.

Figure 7-10. Battery Cell Temperature Measurement



During one measuring cycle only one temperature input can be measured by the ADC. The channel can be selected in the Operation Register (0x02) by the TempMode bit (bit 3).

The ADC output is equal to:

$$\text{out} = 2048 \times \left(1 + \frac{\text{RES\_NTC(1)}}{(\text{RES\_NTC(1)} + \text{RES\_REF(1)})} \times \frac{8}{15} - \frac{8}{10}\right)$$

Table 7-10. Electrical Characteristics

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
7.1	Reference voltage		TEMPREF	$V_{TEMPREF} - V_{TEMPVSS}$	1.1	1.2	1.3	V	A
7.2	Reference voltage output current		TEMPREF	$I_{TEMPREF}$			2	mA	A
7.3	Input voltage range		TEMP1	V_{TEMP1}	0		$V_{TEMPREF}$	V	A
7.4	Input voltage range		TEMP2	V_{TEMP2}	0		$V_{TEMPREF}$	V	A
7.5	Input current	VTEMPx = 1.2V	TEMPx	I_{TEMPx}			1	µA	A
7.6	Code output for value(RES_NTCx) = value (RES_REFx)	V(TEMPi, TEMPVSS) = 0.5 × V(TEMPREF, TEMPVSS)			931_D	956_D	981_D		A
7.7	Code output for value(RES_NTC) = 0	V(TEMPi, TEMPVSS) = 0			385_D	410_D	435_D		A
7.8	Code output for value(RES_NTC) = infinite	V(TEMPi, TEMPVSS) = V(TEMPREF)			1477_D	1502_D	1527_D		A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

7.5.4 Internal Voltage Regulator

The regulator output is pin AVDD. The pins AVDD and DVDD have to be connected together. An external filtering capacitor (10nF recommended) is used to filter and stabilize the function. The regulator output can be used to supply outside functions at the price of power supply imbalance between battery cells.

Table 7-11. Electrical Characteristics

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
8.1	Supply voltage range		VDDHV	V_{VDDHV}	6.9		30	V	A
8.2	Regulated output voltage		AVDD	V_{AVDD}	3.1	3.3	3.5	V	A
8.3	Output current		AVDD	I_{AVDD}	0		5	mA	A
8.4	C_{load} (load capacitor)		C_{load}		9	10		nF	D
*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter									

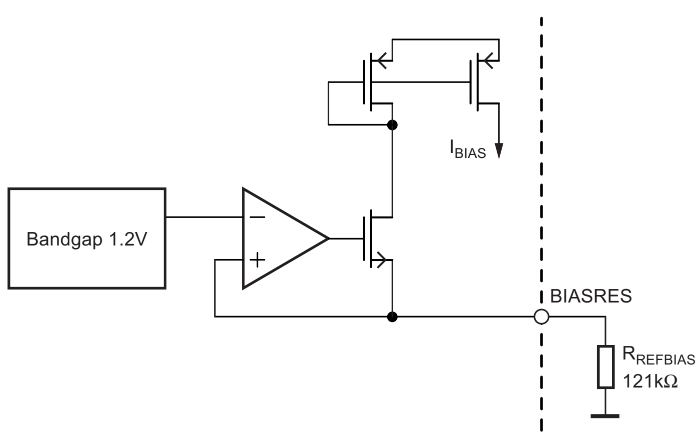
7.5.5 Central Biasing

This block generates a precise bias current to supply internal blocks of the IC. Connection of any external loads to this pin is not allowed.

Table 7-12. Electrical Characteristics

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
9.1	Biasing voltage		BIASRES	$V_{BIASRES}$		1.2		V	A
9.2	External resistor			$R_{Refbias}$		121		kΩ	D
9.3	Tolerance			$\Delta R_{Refbias}$	–1		+1	%	D
9.4	Maximum external parasitic capacitor		BIASRES	$C_{External}$			50	pF	D
*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter									

Figure 7-11. Internal Bias Current Generation



7.5.6 RC Oscillator

Table 7-13. Internal RC Oscillator Frequency

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
10.1	Oscillator frequency			f_{Osc}	45	50	55	kHz	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

7.5.7 Power On Reset

The power on reset is used to initialize the digital part at power-up.

The power on reset circuit is functional when the voltage at pin DVDD is larger than V_{POROP}.

There are two reset sources:

System “hard reset”
System hard reset occurs when the voltage at pin DVVD goes below the power on reset threshold.

ATA6870N registers are set to their initial values.

After t = t_{RESET}, the MCU can access the Atmel® ATA6870N.

Figure 7-12. Power On Reset

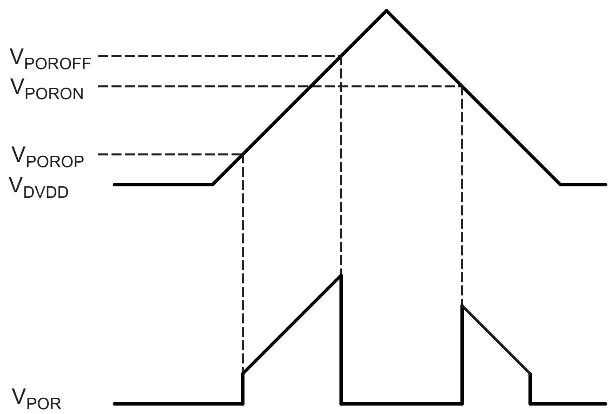


Table 7-14. Electrical Characteristics

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
11.1	Power on reset functional		DVDD	V_{POROP}			0.8	V	A
11.2	Power on reset off		DVDD	V_{POROFF}	1.5		2.5	V	A
11.3	Power on reset hysteresis		DVDD	$V_{POROFF} - V_{PORON}$	0.03			V	C
11.4	Power on reset time			t_{RESET}			800	µs	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

7.6 Digital Part

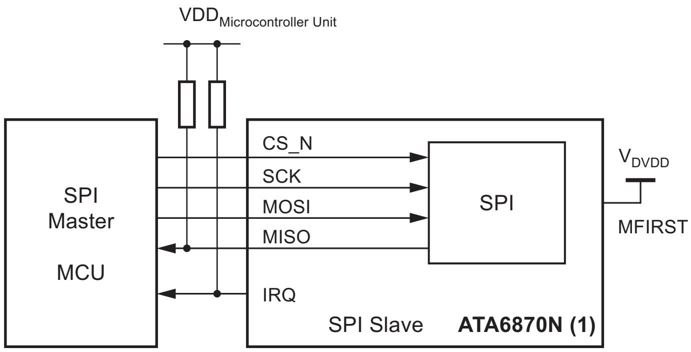
7.6.1 General Features

The digital parts of the ATA6870N includes the following blocks:

- 4-wire-SPI full duplex communication with external host MCU
- SPI system protocol management (frames decoding) and configuration registers bank
- Interrupt to MCU management
- Operations decoding (voltage and/or temperature acquisition) and analog part control
- Low frequency timer (50kHz) for wake-up management

7.6.2 Host Interface

Figure 7-13. Host Interface



The communication between Atmel® ATA6870N (1) and its host MCU, as well as ATA6870N (n) and ATA6870N(n-1) is based on a 4 wire serial/parallel SPI interface (CS_N, SCK, MISO, MOSI) and an interrupt line (IRQ). The SPI interface allows register read and write operations. The interrupt line indicates events that require host intervention.

Atmel ATA6870N(n)'s 4 wire-SPI bus inputs (CS_N, SCK, MOSI) are up-shifted through level shifters. They are internally connected to the outputs CS_N_OUT, SCK_OUT, MOSI_OUT and connected to ATA6870N(n+1) (CS_N, SCK, MOSI).

Atmel ATA6870N(n)'s 4 wire-SPI bus output (MISO) and ATA6870N(n)'s interrupt (IRQ) are down-shifted through level shifters and connected to ATA6870N(n-1) (MOSI_IN, IRQ_IN) or host MCU (n = 1).