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ATA8203/ATA8204/ATA8205

Industrial UHF ASK/FSK Receiver

DATASHEET

Features

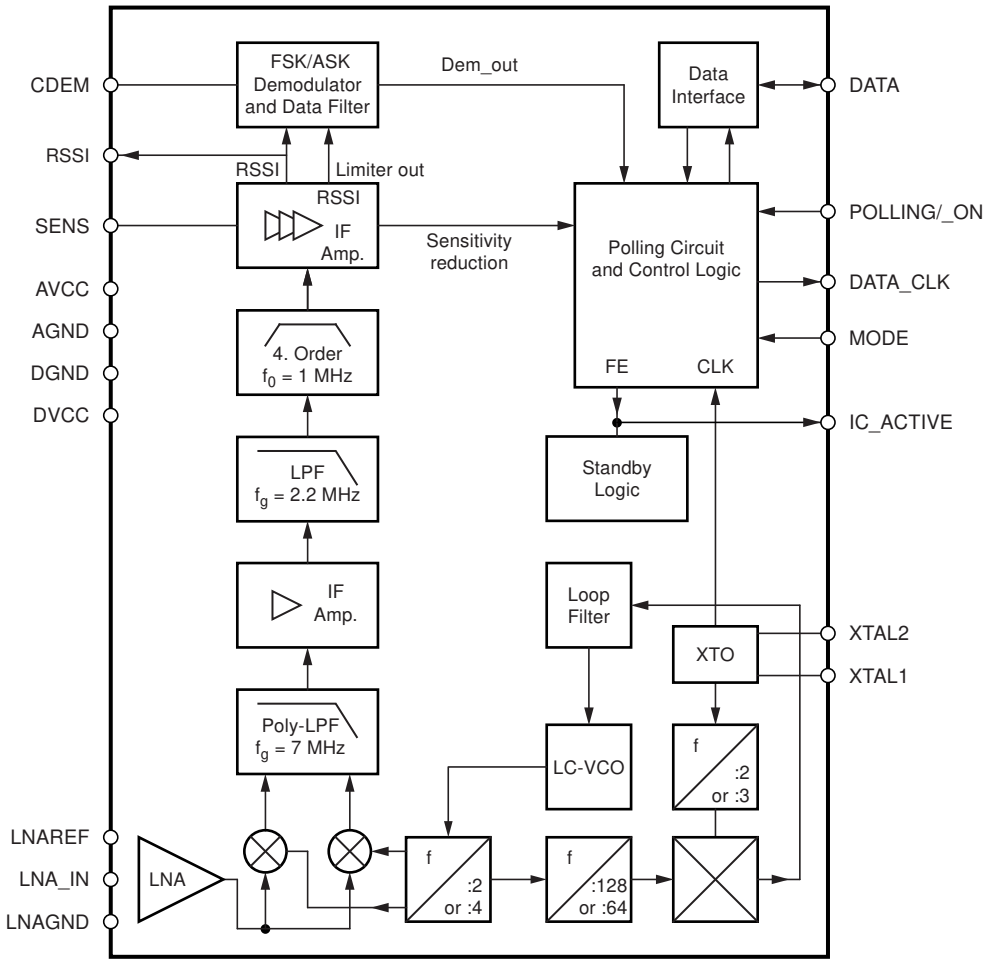
- Frequency receiving range of (3 versions)
  - f_0 = 312.5MHz to 317.5MHz or
  - f_0 = 431.5MHz to 436.5MHz or
  - f_0 = 868MHz to 870MHz
- 30dB image rejection
- Receiving bandwidth
  - B_{IF} = 300kHz for 315MHz/433MHz version
  - B_{IF} = 600kHz for 868MHz version
- Fully integrated LC-VCO and PLL loop filter
- Very high sensitivity with power matched LNA
  - Atmel® ATA8203/ATA8204:
    - –107dBm, FSK, BR_0 (1.0Kbit/s to 1.8Kbit/s), Manchester, BER 10E-3
    - –113dBm, ASK, BR_0 (1.0Kbit/s to 1.8Kbit/s), Manchester, BER 10E-3
  - Atmel ATA8205:
    - –105dBm, FSK, BR_0 (1.0Kbit/s to 1.8Kbit/s), Manchester, BER 10E-3
    - –111dBm, ASK, BR_0 (1.0Kbit/s to 1.8Kbit/s), Manchester, BER 10E-3
- High system IIP3
  - –18dBm at 868MHz
  - –23dBm at 433MHz
  - –24dBm at 315MHz
- System 1-dB compression point
  - –27.7dBm at 868MHz
  - –32.7dBm at 433MHz
  - –33.7dBm at 315MHz
- High large-signal capability at GSM band (blocking –33dBm at +10MHz, IIP3 = –24dBm at +20MHz)
- Logarithmic RSSI output
- XTO start-up with negative resistor of 1.5kΩ
- 5V to 20V automotive compatible data interface
- Data clock available for manchester and bi-phase-coded signals
- Programmable digital noise suppression
- Low power consumption due to configurable polling

- Temperature range –40°C to +85°C
- ESD protection 2kV HBM, All pins
- Communication to microcontroller possible using a single bi-directional data line
- Low-cost solution due to high integration level with minimum external circuitry requirements
- Supply voltage range 4.5V to 5.5V

Benefits

- Low BOM list due to high integration
- Use of low-cost 13MHz crystal
- Lowest average current consumption for application due to self polling feature
- Reuse of Atmel ATA5743 software
- World-wide coverage with one PCB due to 3 versions are pin compatible

Figure 1-2. Block Diagram



2. Pin Configuration

Figure 2-1. Pinning SSO20

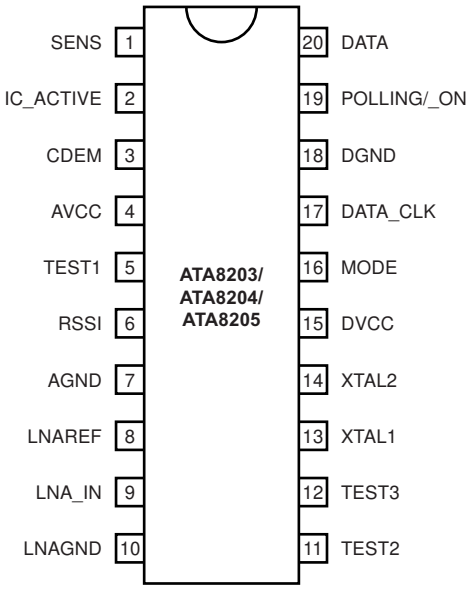


Table 2-1. Pin Description

Pin	Symbol	Function
1	SENS	Sensitivity-control resistor
2		

3. RF Front-end

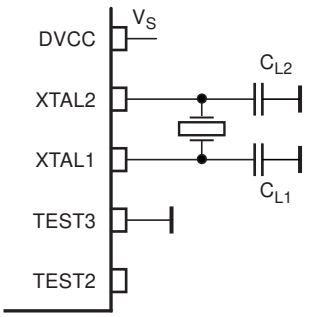
The RF front-end of the receiver is a low-IF heterodyne configuration that converts the input signal into about 1MHz IF signal with a typical image rejection of 30dB. According to Figure Figure 1-2 on page 4 the front-end consists of an LNA (Low Noise Amplifier), LO (Local Oscillator), I/Q mixer, polyphase low-pass filter and an IF amplifier.

The PLL generates the drive frequency f_{LO} for the mixer using a fully integrated synthesizer with integrated low noise LC-VCO (Voltage Controlled Oscillator) and PLL-loop filter. The XTO (crystal oscillator) generates the reference frequency $f_{REF} = f_{XTO}/2$ (868MHz and 433MHz versions) or $f_{REF} = f_{XTO}/3$ (315MHz version). The integrated LC-VCO generates two or four times the mixer drive frequency f_{VCO}. The I/Q signals for the mixer are generated with a divide by two or four circuit ($f_{LO} = f_{VCO}/2$ for 868MHz version, $f_{LO} = f_{VCO}/4$ for 433MHz and 315MHz versions). f_{VCO} is divided by a factor of 128 or 64 and feeds into a phase frequency detector and is compared with f_{REF}. The output of the phase frequency detector is fed into an integrated loop filter and thereby generates the control voltage for the VCO. If f_{LO} is determined, f_{XTO} can be calculated using the following formula: $f_{REF} = f_{LO}/128$ for 868MHz band, $f_{REF} = f_{LO}/64$ for 433MHz bands, $f_{REF} = f_{LO}/64$ for 315MHz bands.

The XTO is a two-pin oscillator that operates at the series resonance of the quartz crystal with high current but low voltage signal, so that there is only a small voltage at the crystal oscillator frequency at pins XTAL1 and XTAL2. According to Figure 3-1, the crystal should be connected to GND with two capacitors C_{L1} and C_{L2} from XTAL1 and XTAL2 respectively. The value of these capacitors are recommended by the crystal supplier. Due to an inductive impedance at steady state oscillation and some PCB parasitics, a lower value of C_{L1} and C_{L2} is normally necessary.

The value of C_{Lx} should be optimized for the individual board layout to achieve the exact value of f_{XTO} and hence of f_{LO}. (The best way is to use a crystal with known load resonance frequency to find the right value for this capacitor.) When designing the system in terms of receiving bandwidth and local oscillator accuracy, the accuracy of the crystal and the XTO must be considered.

Figure 3-1. XTO Peripherals



The nominal frequency f_{LO} is determined by the RF input frequency f_{RF} and the IF frequency f_{IF} using the following formula (low-side injection):

$$f_{LO} = f_{RF} - f_{IF}$$

To determine f_{LO}, the construction of the IF filter must be considered. The nominal IF frequency is f_{IF} = 950kHz. To achieve a good accuracy of the filter corner frequencies, the filter is tuned by the crystal frequency f_{XTO}. This means that there is a fixed relationship between f_{IF} and f_{LO}.

$f_{IF} = f_{LO}/318$ for the 315MHz band (Atmel® ATA8203)
$f_{IF} = f_{LO}/438$ for the 433.92MHz band (Atmel ATA8204)
$f_{IF} = f_{LO}/915$ for the 868.3MHz band (Atmel ATA8205)

The relationship is designed to achieve the nominal IF frequency of:

f_{IF} = 987Hz for the 315MHz and B_{IF} = 300kHz (Atmel ATA8203)
f_{IF} = 987kHz for the 433.92MHz and B_{IF} = 300kHz (Atmel ATA8204)
f_{IF} = 947.8kHz for the 868.3MHz and B_{IF} = 600kHz (Atmel ATA8205)

The RF input either from an antenna or from an RF generator must be transformed to the RF input pin LNA_IN. The input impedance of this pin is provided in the electrical parameters. The parasitic board inductances and capacitances influence the input matching. The RF receiver Atmel ATA8203/ATA8204/ATA8205 exhibits its highest sensitivity if the LNA is power matched. Because of this, matching to a SAW filter, a 50Ω or an antenna is easier.

Figure 14-1 on page 30 “Application Circuit” shows a typical input matching network for f_{RF} = 315MHz, f_{RF} = 433.92MHz or f_{RF} = 868.3MHz to 50Ω. The input matching network shown in Table 14-2 on page 30 is the reference network for the parameters given in the electrical characteristics.

4. Analog Signal Processing

4.1 IF Filter

The signals coming from the RF front-end are filtered by the fully integrated 4th-order IF filter. The IF center frequency is:

f_{IF} = 987kHz for the 315 MHz and B_{IF} = 300kHz (Atmel® ATA8203)
f_{IF} = 987kHz for the 433.92 MHz and B_{IF} = 300kHz (Atmel ATA8204)
f_{IF} = 947.9kHz for the 868.3 MHz and B_{IF} = 600kHz (Atmel ATA8205)

The nominal bandwidth is 300 kHz for ATA8203 and ATA8204 and 600 kHz for ATA8205.

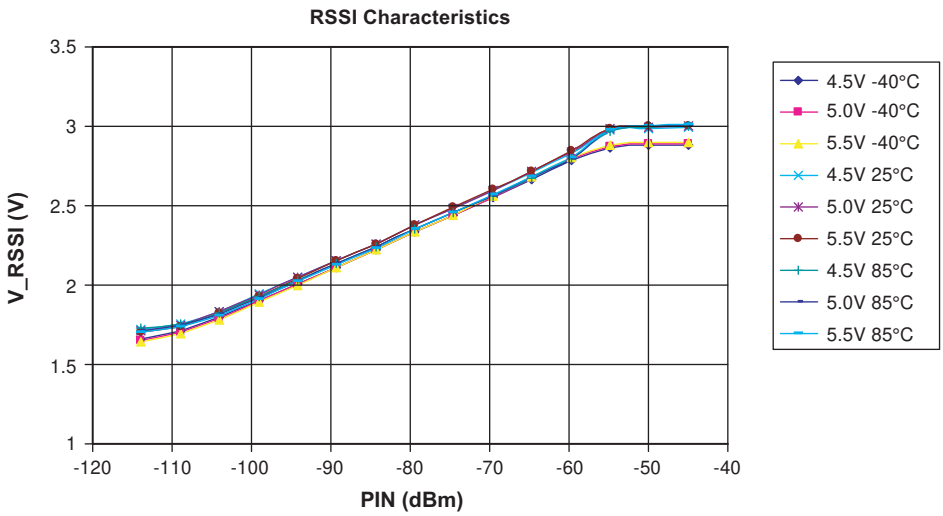
4.2 Limiting RSSI Amplifier

The subsequent RSSI amplifier enhances the output signal of the IF amplifier before it is fed into the demodulator. The dynamic range of this amplifier is ΔR_{RSSI} = 60dB. If the RSSI amplifier is operated within its linear range, the best S/N ratio is maintained in ASK mode. If the dynamic range is exceeded by the transmitter signal, the S/N ratio is defined by the ratio of the maximum RSSI output voltage and the RSSI output voltage due to a disturber. The dynamic range of the RSSI amplifier is exceeded if the RF input signal is approximately 60 dB higher compared to the RF input signal at full sensitivity.

The S/N ratio is not affected by the dynamic range of the RSSI amplifier in FSK mode because only the hard limited signal from a high-gain limiting amplifier is used by the demodulator.

The output voltage of the RSSI amplifier (VRSSI) is available at pin RSSI. Using the RSSI output signal, the signal strength of different transmitters can be distinguished. The usable input power range P_{Ref} is –100dBm to –55dBm.

Figure 4-1. RSSI Characteristics Atmel ATA8204



The output voltage of the RSSI amplifier is internally compared to a threshold voltage V_{Th_red}. V_{Th_red} is determined by the value of the external resistor R_{Sens}. R_{Sens} is connected between pin SENS and GND or V_S. The output of the comparator is fed into the digital control logic. By this means, it is possible to operate the receiver at a lower sensitivity.

If R_{Sens} is connected to GND, the receiver switches to full sensitivity. It is also possible to connect the pin SENS directly to GND to get the maximum sensitivity.

If R_{Sens} is connected to V_S, the receiver operates at a lower sensitivity. The reduced sensitivity is defined by the value of R_{Sens}, and the maximum sensitivity is defined by the signal-to-noise ratio of the LNA input. The reduced sensitivity depends on the signal strength at the output of the RSSI amplifier.

Since different RF input networks may exhibit slightly different values for the LNA gain, the sensitivity values given in the electrical characteristics refer to a specific input matching. This matching is described and illustrated in Section 14. “Data Interface” on page 30.

R_{Sens} can be connected to V_S or GND using a microcontroller. The receiver can be switched from full sensitivity to reduced sensitivity or vice versa at any time. In polling mode, the receiver does not wake up if the RF input signal does not exceed the selected sensitivity. If the receiver is already active, the data stream at pin DATA disappears when the input signal is lower than defined by the reduced sensitivity. Instead of the data stream, the pattern according to Figure 4-2 “Steady L State Limited DATA Output Pattern” is issued at pin DATA to indicate that the receiver is still active (see Figure 13-2 on page 28 “Data Interface”).

Figure 4-2. Steady L State Limited DATA Output Pattern

4.3 FSK/ASK Demodulator and Data Filter

The signal coming from the RSSI amplifier is converted into the raw data signal by the ASK/FSK demodulator. The operating mode of the demodulator is set using the bit ASK/_FSK in the OPMODE register. Logic L sets the demodulator to FSK, applying H to ASK mode.

In ASK mode an automatic threshold control circuit (ATC) is employed to set the detection reference voltage to a value where a good signal to noise ratio is achieved. This circuit also implements the effective suppression of any kind of in-band noise signals or competing transmitters. If the S/N (ratio to suppress in-band noise signals) exceeds about 10dB the data signal can be detected properly. However, better values are found for many modulation schemes of the competing transmitter.

The FSK demodulator is intended to be used for an FSK deviation of 10kHz ≤ Δf ≤ 100kHz. The data signal in FSK mode can be detected if the S/N (ratio to suppress in-band noise signals) exceeds about 2dB. This value is valid for all modulation schemes of a disturber signal.

The output signal of the demodulator is filtered by the data filter before it is fed into the digital signal processing circuit. The data filter improves the S/N ratio as its pass-band can be adopted to the characteristics of the data signal. The data filter consists of a 1st order high-pass and a 2nd order low-pass filter.

The high-pass filter cut-off frequency is defined by an external capacitor connected to pin CDEM. The cut-off frequency of the high-pass filter is defined by the following formula:

In self-polling mode the data filter must settle very rapidly to achieve a low current consumption. Therefore, CDEM cannot be increased to very high values if self-polling is used. On the other hand, CDEM must be large enough to meet the data filter requirements according to the data signal. Recommended values for CDEM are given in the electrical characteristics.

The cut-off frequency of the low-pass filter is defined by the selected baud-rate range (BR_Range). The BR_Range is defined in the OPMODE register (refer to Section 11. “Configuring the Receiver” on page 23). The BR_Range must be set in accordance to the baud-rate used.

The Atmel® ATA8203/ATA8204/ATA8205 is designed to operate with data coding where the DC level of the data signal is 50%. This is valid for Manchester and Bi-phase coding. If other modulation schemes are used, the DC level should always remain within the range of V_{DC_min} = 33% and V_{DC_max} = 66%. The sensitivity may be reduced by up to 2dB in that condition.

Each BR_Range is also defined by a minimum and a maximum edge-to-edge time (t_{ee_sig}). These limits are defined in the electrical characteristics. They should not be exceeded to maintain full sensitivity of the receiver.

5. Receiving Characteristics

The RF receiver Atmel® ATA8203/ATA8204/ATA8205 can be operated with and without a SAW front-end filter. In a typical automotive application, a SAW filter is used to achieve better selectivity and large signal capability. The receiving frequency response without a SAW front-end filter is illustrated in Figure 5-1 “Narrow Band Receiving Frequency Response ATA8204”. This example relates to ASK mode. FSK mode exhibits a similar behavior. The plots are printed relatively to the maximum sensitivity. If a SAW filter is used, an insertion loss of about 3dB must be considered, but the overall selectivity is much better.

When designing the system in terms of receiving bandwidth, the LO deviation must be considered as it also determines the IF center frequency. The total LO deviation is calculated, to be the sum of the deviation of the crystal and the XTO deviation of the Atmel ATA8203/ATA8204/ATA8205. Low-cost crystals are specified to be within ±90ppm over tolerance, temperature, and aging. The XTO deviation of the Atmel ATA8203/ATA8204/ATA8205 is an additional deviation due to the XTO circuit. This deviation is specified to be ±10ppm worst case for a crystal with CM = 7fF. If a crystal of ±90ppm is used, the total deviation is ±100ppm in that case. Note that the receiving bandwidth and the IF-filter bandwidth are equivalent in ASK mode but not in FSK mode.

Figure 5-1. Narrow Band Receiving Frequency Response ATA8204

6. Polling Circuit and Control Logic

The receiver is designed to consume less than 1 mA while being sensitive to signals from a corresponding transmitter. This is achieved using the polling circuit. This circuit enables the signal path periodically for a short time. During this time the bit-check logic verifies the presence of a valid transmitter signal. Only if a valid signal is detected, the receiver remains active and transfers the data to the connected microcontroller. If there is no valid signal present, the receiver is in sleep mode most of the time resulting in low current consumption. This condition is called polling mode. A connected microcontroller is disabled during that time.

All relevant parameters of the polling logic can be configured by the connected microcontroller. This flexibility enables the user to meet the specifications in terms of current consumption, system response time, data rate etc.

7. Basic Clock Cycle of the Digital Circuitry

The complete timing of the digital circuitry and the analog filtering is derived from one clock. This clock cycle T_{Clk} is derived from the crystal oscillator (XTO) in combination with a divide by 28 or 30 circuit. According to Section 3. “RF Front-end” on page 6, the frequency of the crystal oscillator (f_{XTO}) is defined by the RF input signal (f_{RFin}) which also defines the operating frequency of the local oscillator (f_{LO}). The basic clock cycle for Atmel® ATA8204 and Atmel ATA8205 is T_{Clk} 28/f_{XTO} giving T_{Clk} = 2.066µs for f_{RF} = 868.3MHz and T_{Clk} = 2.069µs for f_{RF} = 433.92MHz. For Atmel ATA8203 the basic clock cycle is T_{Clk} = 30/f_{REF} giving T_{Clk} = 2.0382µs for f_{RF} = 315MHz.

T_{Clk} controls the following application-relevant parameters:

- Timing of the polling circuit including bit check
- Timing of the analog and digital signal processing
- Timing of the register programming
- Frequency of the reset marker
- IF filter center frequency (fIF0)

Most applications are dominated by three transmission frequencies: $f_{Transmit}$ = 315MHz is mainly used in USA, $f_{Transmit}$ = 868.3MHz and 433.92MHz in Europe. All timings are based on T_{Clk}. For the aforementioned frequencies, T_{Clk} is given as:

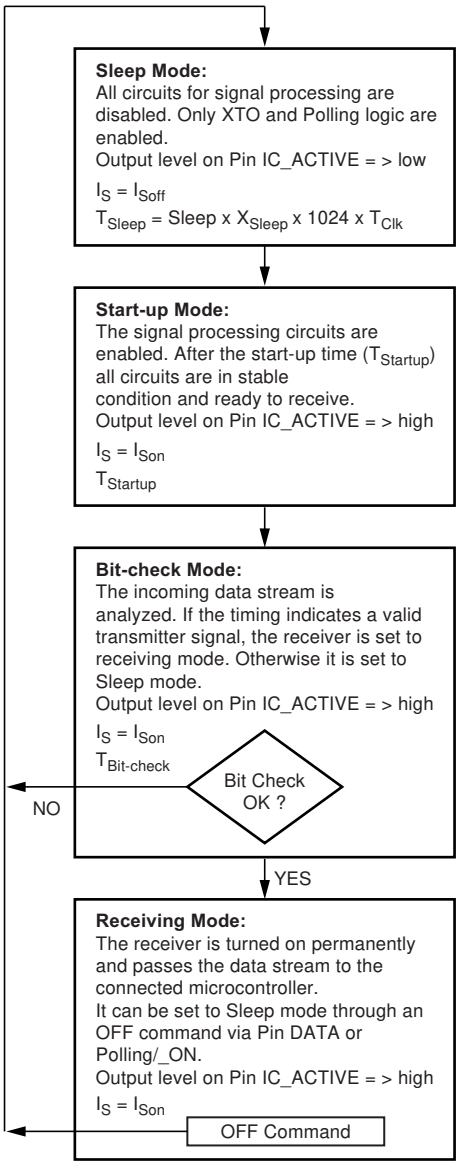
- Application 315MHz band (f_{XTO} = 14.71875MHz, f_{LO} = 314.13MHz, T_{Clk} = 2.0382µs)
- Application 868.3MHz band (f_{XTO} = 13.55234MHz, f_{LO} = 867.35MHz, T_{Clk} = 2.066µs)
- Application 433.92MHz band (f_{XTO} = 13.52875MHz, f_{LO} = 432.93MHz, T_{Clk} = 2.0696µs)

For calculation of T_{Clk} for applications using other frequency bands, see table in Section 18. “Electrical Characteristics Atmel ATA8204, ATA8205” on page 35.

The clock cycle of some function blocks depends on the selected baud-rate range (BR_Range), which is defined in the OPMODE register. This clock cycle T_{XClk} is defined by the following formulas:

BR_Range =	BR_Range0:	$T_{XClk} = 8 \times T_{Clk}$
	BR_Range1:	$T_{XClk} = 4 \times T_{Clk}$
	BR_Range2:	$T_{XClk} = 2 \times T_{Clk}$
	BR_Range3:	$T_{XClk} = 1 \times T_{Clk}$

Figure 8-1. Polling Mode Flow Chart



Sleep: 5-bit word defined by Sleep 0 to Sleep 4 in OPMODE register

X_{Sleep}: Extension factor defined by XSleepStd according to Table 11-8

T_{Clk}: Basic clock cycle defined by f_{XTO} and Pin MODE

$T_{Startup}$: Is defined by the selected baud rate range and TClk. The baud-rate range is defined by Baud 0 and Baud 1 in the OPMODE register.

$T_{Bit\text{-}check}$: Depends on the result of the bit check

If the bit check is ok, $T_{Bit\text{-}check}$ depends on the number of bits to be checked ($N_{Bit\text{-}check}$) and on the data rate used.

If the bit check fails, the average time period for that check depends on the selected baud-rate range and on T_{Clk}. The baud-rate range is defined by Baud 0 and Baud 1 in the OPMODE register.

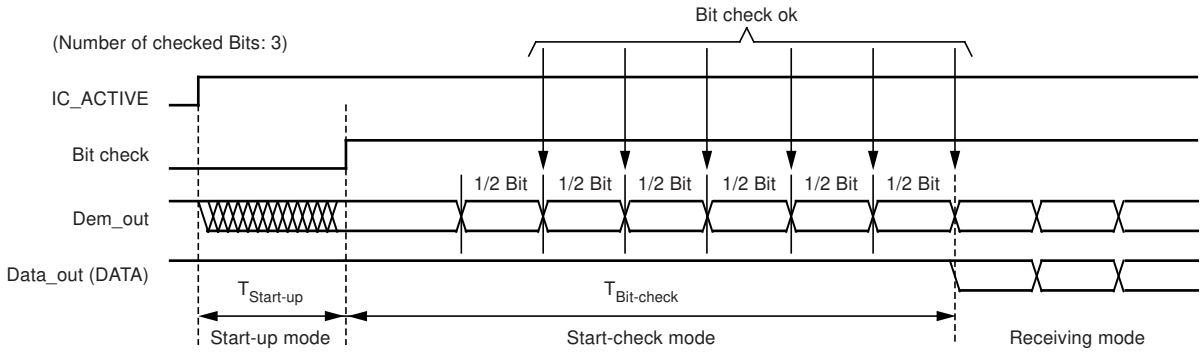
8.2 Bit-check Mode

In bit-check mode the incoming data stream is examined to distinguish between a valid signal from a corresponding transmitter and signals due to noise. This is done by subsequent time frame checks where the distances between 2 signal edges are continuously compared to a programmable time window. The maximum number of these edge-to-edge tests, before the receiver switches to receiving mode, is also programmable.

8.3 Configuring the Bit Check

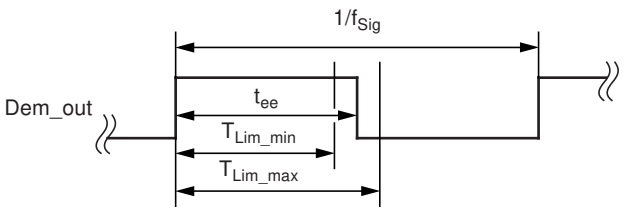
Assuming a modulation scheme that contains two edges per bit, two time frame checks verify one bit. This is valid for Manchester, Bi-phase, and most other modulation schemes. The maximum count of bits to be checked can be set to 0, 3, 6, or 9 bits using the variable $N_{Bit\text{-}check}$ in the OPMODE register. This implies 0, 6, 12, and 18 edge-to-edge checks respectively. If $N_{Bit\text{-}check}$ is set to a higher value, the receiver is less likely to switch to receiving mode due to noise. In the presence of a valid transmitter signal, the bit check takes less time if $N_{Bit\text{-}check}$ is set to a lower value. In polling mode, the bit-check time is not dependent on NBit-check. Figure 8-2 shows an example where three bits are tested successfully and the data signal is transferred to pin DATA.

Figure 8-2. Timing Diagram for Complete Successful Bit Check



According to Figure 8-3, the time window for the bit check is defined by two separate time limits. If the edge-to-edge time t_{ee} is in between the lower bit-check limit T_{Lim_min} and the upper bit-check limit T_{Lim_max}, the check continues. If t_{ee} is smaller than T_{Lim_min} or t_{ee} exceeds T_{Lim_max}, the bit check is terminated and the receiver switches to sleep mode.

Figure 8-3. Valid Time Window for Bit Check



For best noise immunity using a low span between T_{Lim_min} and T_{Lim_max} is recommended. This is achieved using a fixed frequency at a 50% duty cycle for the transmitter preburst. A “11111...” or a “10101...” sequence in Manchester or Bi-phase is suitable for this. A good compromise between receiver sensitivity and susceptibility to noise is a time window of ±30% regarding the expected edge-to-edge time t_{ee}. Using pre-burst patterns that contain various edge-to-edge time periods, the bit-check limits must be programmed according to the required span.

The bit-check limits are determined by means of the formula below.

$T_{Lim\_min} = Lim\_min \times T_{XClk}$
$T_{Lim\_max} = (Lim\_max - 1) \times T_{XClk}$

Lim_min and Lim_max are defined by a 5-bit word each within the LIMIT register.

Using above formulas, Lim_min and Lim_max can be determined according to the required T_{Lim_min}, T_{Lim_max} and T_{XClk}. The time resolution defining T_{Lim_min} and T_{Lim_max} is T_{XClk}. The minimum edge-to-edge time t_{ee} ($t_{DATA\_L\_min}$, $t_{DATA\_H\_min}$) is defined according to the Section 8.6 “Digital Signal Processing” on page 15. The lower limit should be set to Lim_min ≥ 10. The maximum value of the upper limit is Lim_max = 63.

If the calculated value for Lim_min is < 19, it is recommended to check 6 or 9 bits ($N_{Bit\text{-}check}$) to prevent switching to receiving mode due to noise.

8.4 Duration of the Bit Check

If no transmitter signal is present during the bit check, the output of the ASK/FSK demodulator delivers random signals. The bit check is a statistical process and $T_{Bit\text{-}check}$ varies for each check. Therefore, an average value for $T_{Bit\text{-}check}$ is given in the electrical characteristics. $T_{Bit\text{-}check}$ depends on the selected baud-rate range and on T_{Clk}. A higher baud-rate range causes a lower value for $T_{Bit\text{-}check}$ resulting in a lower current consumption in polling mode.

In the presence of a valid transmitter signal, $T_{Bit\text{-}check}$ is dependent on the frequency of that signal, f_{Sig}, and the count of the checked bits, $N_{Bit\text{-}check}$. A higher value for $N_{Bit\text{-}check}$ thereby results in a longer period for $T_{Bit\text{-}check}$ requiring a higher value for the transmitter pre-burst $T_{Preburst}$.

8.5 Receiving Mode

If the bit check was successful for all bits specified by $N_{Bit\text{-}check}$, the receiver switches to receiving mode. According to Figure 8-2 on page 13, the internal data signal is switched to pin DATA in that case, and the data clock is available after the start bit has been detected (see Figure 9-1 on page 18). A connected microcontroller can be woken up by the negative edge at pin DATA or by the data clock at pin DATA_CLK. The receiver stays in that condition until it is switched back to polling mode explicitly.

8.6 Digital Signal Processing

The data from the ASK/FSK demodulator (Dem_out) is digitally processed in different ways and as a result converted into the output signal data. This processing depends on the selected baud-rate range (BR_Range). Figure 8-7 illustrates how Dem_out is synchronized by the extended clock cycle T_{XClk}. This clock is also used for the bit-check counter. Data can change its state only after T_{XClk} has elapsed. The edge-to-edge time period t_{ee} of the Data signal as a result is always an integral multiple of T_{XClk}.

The minimum time period between two edges of the data signal is limited to $t_{ee} \geq T_{DATA\_min}$. This implies an efficient suppression of spikes at the DATA output. At the same time it limits the maximum frequency of edges at DATA. This eases the interrupt handling of a connected microcontroller.

The maximum time period for DATA to stay low is limited to $T_{DATA\_L\_max}$. This function is employed to ensure a finite response time in programming or switching off the receiver via pin DATA. $T_{DATA\_L\_max}$ is therefore longer than the maximum time period indicated by the transmitter data stream. Figure 8-9 on page 16 gives an example where Dem_out remains Low after the receiver has switched to receiving mode.

Figure 8-7. Synchronization of the Demodulator Output

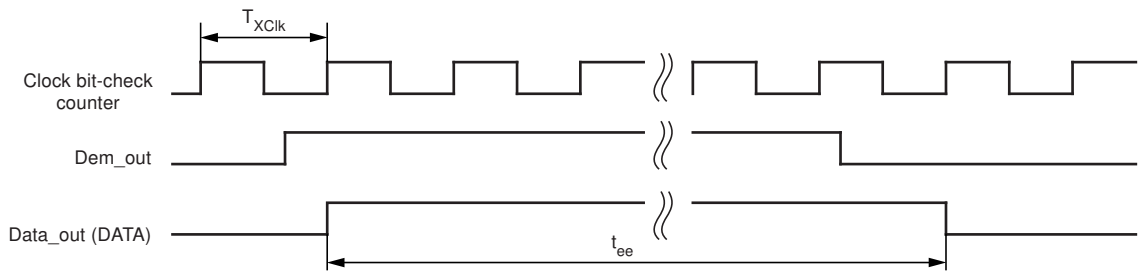


Figure 8-8. Debouncing of the Demodulator Output