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ATA8742

Microcontroller with UHF ASK/FSK Transmitter

DATASHEET

General Features

- Transmitter with microcontroller consisting of an AVR® microcontroller and RF transmitter PLL in a single QFN24 5mm × 5mm package (pitch 0.65mm)
  - f_0 = 429MHz to 439MHz
- Temperature range –40°C to +85°C
- Supply voltage 2.0V to 4.0V allowing usage of single li-cell power supply
- Low power consumption
  - Active mode: Typical 9.8mA at 3.0V and 4MHz microcontroller-clock
  - Power-down mode: Typical 200nA at 3.0V
- Modulation scheme ASK/FSK
- Integrated PLL loop filter
- Output power of 7.5dBm at 433.92MHz
- Easy to design-in due to excellent isolation of the PLL from the PA and power supply
- Single-ended antenna output with high efficient power amplifier
- Very robust ESD protection: HBM 2500V, MM100V, CDM 1000V
- High performance, low power AVR 8-bit microcontroller, similar to popular Atmel® ATtiny44
- Well known and market-accepted RISC architecture
- Non-volatile program and data memories
  - 4KBytes of in-system programmable program memory flash
  - 256Bytes in-system programmable EEPROM
  - 256Bytes internal SRAM
- Programming lock for self-programming flash program and EEPROM data security
- Peripheral features
  - Two Timer/Counter, 8- and 16-bit counters with Two PWM channels on both
  - 10-bit ADC
  - On-chip analog comparator
  - Programmable watchdog timer with separate on-chip oscillator
  - Universal serial interface (USI)

- Special microcontroller features
  - debugWIRE on-chip debug system
  - In-system programmable via SPI port
  - External and internal interrupt sources
  - Pin change interrupt on 12 pins
  - Enhanced power-on reset circuit
  - Programmable brown-out detection circuit
  - Internal calibrated oscillator
  - On-chip temperature sensor
- 12 programmable I/O lines

1. General Description

The Atmel® ATA8742 is a highly flexible programmable transmitter containing the AVR® microcontroller Atmel ATtiny44V and the UHF PLL transmitters a small QFN24 5mm × 5mm package. This device is a member of a transmitter family covering several operating frequency ranges, which has been specifically developed for the demands of RF low-cost data transmission systems with data rates of up to 32kBit/s. Its primary applications are in the areas of industrial/aftermarket remote keyless-entry (RKE) systems, alarm, telemetering, energy metering systems, home automotion/entertainment and toys. The Atmel ATA8742 can be used in the frequency band of f_0 = 433MHz for ASK or FSK data transmission.

Figure 1-1. ASK System Block Diagram

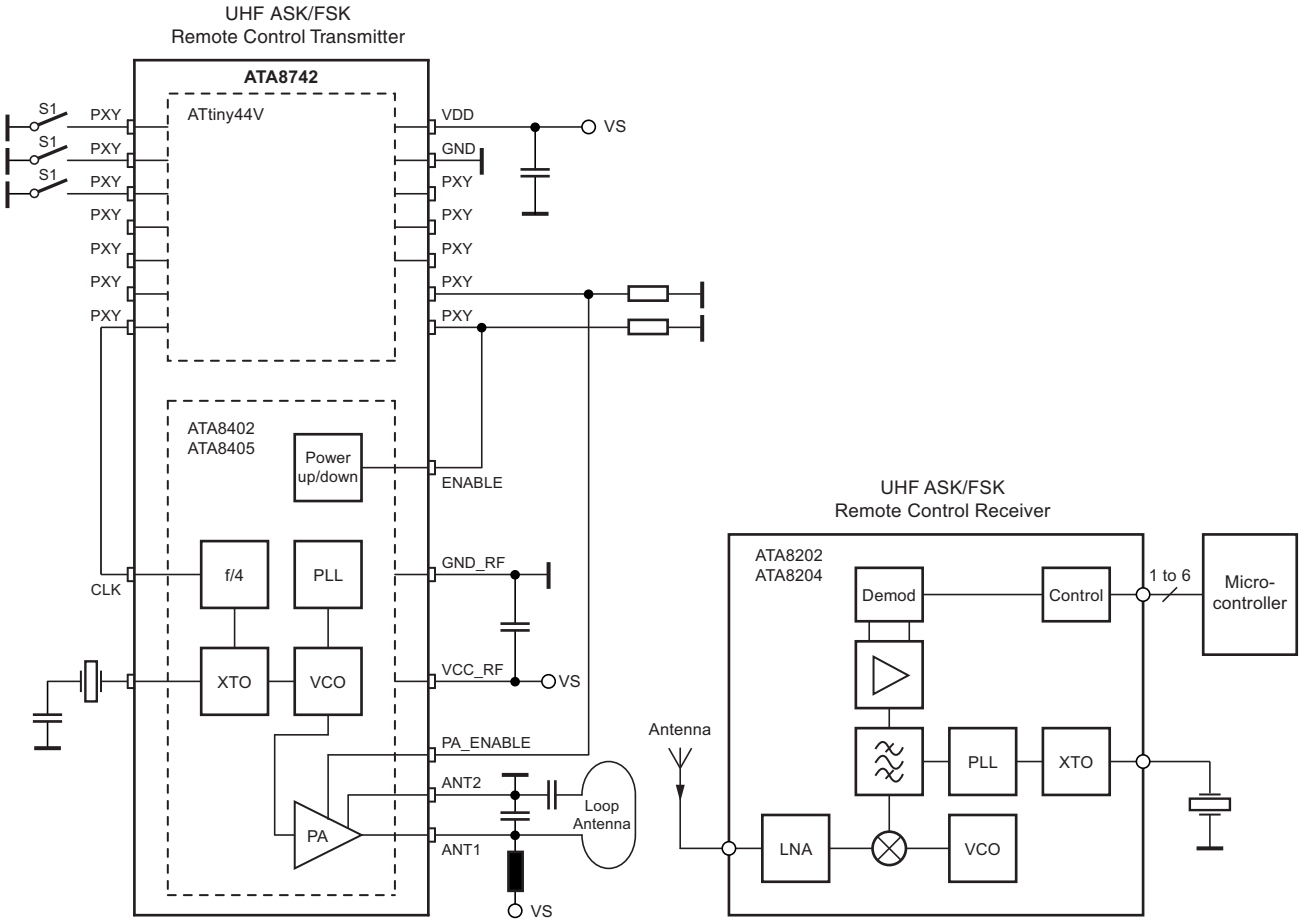
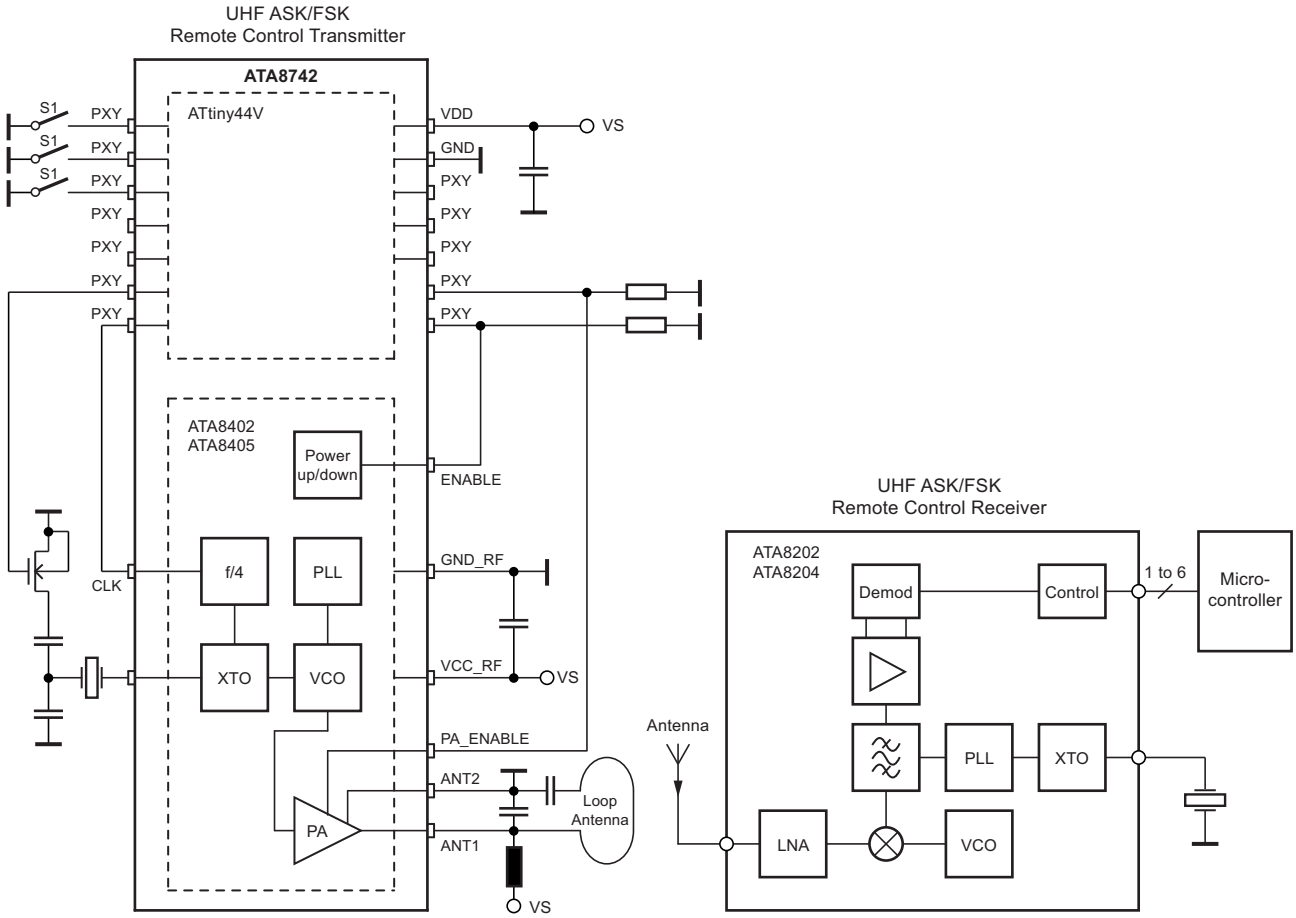


Figure 1-2. FSK System Block Diagram



2. Pin Configuration

Figure 2-1. Pinning QFN24 5 mm x 5 mm

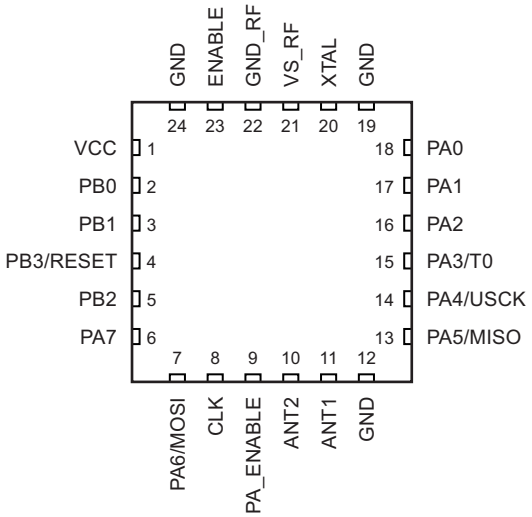


Table 2-1. Pin Description

Pin	Symbol	Function
1	VCC	Microcontroller supply voltage
2	PB0	Port B is a 4-bit bi-directional I/O port with internal pull-up resistor
3	PB1	Port B is a 4-bit bi-directional I/O port with internal pull-up resistor
4	PB3/RESET	Port B is a 4-bit bi-directional I/O port with internal pull-up resistor/reset input
5	PB2	Port B is a 4-bit bi-directional I/O port with internal pull-up resistor
6	PA7	Port A is a 4-bit bi-directional I/O port with internal pull-up resistor
7	PA6 / MOSI	Port A is a 4-bit bi-directional I/O port with internal pull-up resistor
8	CLK	Clock output signal for microcontroller. The clock output frequency is set by the crystal to $f_{XTAL}/4$
9	PA_ENABLE	Switches on power amplifier. Used for ASK modulation
10	ANT2	Emitter of antenna output stage
11	ANT1	Open collector antenna output
12	GND	Ground
13	PA5/MISO	Port A is a 4-bit bi-directional I/O port with internal pull-up resistor
14	PA4/SCK	Port A is a 4-bit bi-directional I/O port with internal pull-up resistor
15	PA3/T0	Port A is a 4-bit bi-directional I/O port with internal pull-up resistor
16	PA2	Port A is a 4-bit bi-directional I/O port with internal pull-up resistor
17	PA1	Port A is a 4-bit bi-directional I/O port with internal pull-up resistor
18	PA0	Port A is a 4-bit bi-directional I/O port with internal pull-up resistor
19	GND	Microcontroller ground
20	XTAL	Connection for crystal
21	VS_RF	Transmitter supply voltage
22	GND_RF	Transmitter ground
23	ENABLE	Enable input
24	GND	Ground
	GND	Ground/backplane (exposed die pad)

2.1 Pin Configuration of RF Pins

Table 2-2. Pin Description

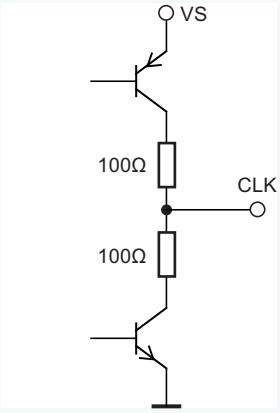
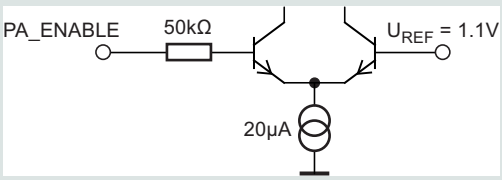
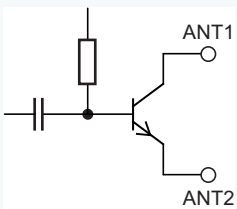
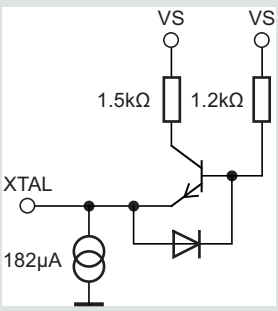
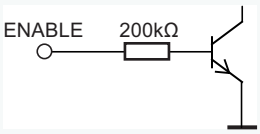
Pin	Symbol	Function	Configuration
8	CLK	Clock output signal for microconroller. The clock output frequency is set by the crystal to $f_{XTAL}/4$.	
9	PA_ENABLE	Switches on power amplifier. Used for ASK modulation.	
10 11	ANT2 ANT1	Emitter of antenna output stage. Open collector antenna output.	
20	XTAL	Connection for crystal.	

Table 2-2. Pin Description (Continued)

Pin	Symbol	Function	Configuration
21	VS	Supply voltage	See ESD protection circuitry (see Figure 8-1 on page 12).
22	GND	Ground	See ESD protection circuitry (see Figure 8-1 on page 12).
23	ENABLE	Enable input	

3. Functional Description

For a typical application 3 to 4 interconnections between the AVR® and the transmitter are required (see Figure 1-1 on page 3 and Figure 1-2 on page 4). The CLK line is used to allow the microcontroller to generate an XTAL-based transmitter signal. The ENABLE line is used to start the XTO, PLL, and clock output of the transmitter. The PA_ENABLE line is used to enable the power amplifier in ASK and FSK mode. In FSK mode a fourth line is necessary to modulate the load capacity of the XTAL. To wake up the system from standby mode at least one key input is required. After pressing the key, the microcontroller starts up with the internal RC oscillator. For TX operation user software must control ENABLE, PA_ENABLE, and XTAL load capacity as described in the following section.

If ENABLE = L and PA_ENABLE = L the transmitter and the microcontroller (MCU) are in standby mode, reducing the power consumption so that a lithium cell can be used as power supply for several years.

If ENABLE = H and PA_ENABLE = L, the XTO, PLL, and the CLK driver from the transmitter are activated. The crystal oscillator together with the PLL from the RF transmitter typically require < 1ms until the PLL is locked and the clock output (Pin 8) is stable.

If ENABLE = H and PA_ENABLE = H, the XTO, PLL, CLK driver, and the power amplifier (PA) are switched on. ASK modulation is achieved by switching on and off the power amplifier via PA_ENABLE. FSK modulation is achieved by switching on and off an additional capacitor between the XTAL load capacitor and GND, thus changing the reference frequency of the PLL. This is done using a MOS switch controlled by a microcontroller output. The power amplifier is switched on via PA_ENABLE = H.

The MCU has to wait at least > 1ms after setting ENABLE = H, before the external clock can be used. The external clock is connected via the timer0 input pin that clocks the USI from the MCU to achieve an accurate data transfer. The frequency of the internal RC oscillator is affected by ambient temperature and operating voltage.

The USI provides two serial synchronous data transfer modes, with different physical I/O ports for the data output. The two wire mode is used for ASK and the three wire mode is used for FSK.

If ENABLE = L and the PA_ENABLE = L, the circuit is in standby mode consuming only a very small amount of current so that a lithium cell used as power supply can work for several years.

With ENABLE = H the XTO, PLL, and the CLK driver are switched on. If PA_ENABLE remains L only the PLL and the XTO are running and the CLK signal is delivered to the microcontroller. The VCO locks to 32 times the XTO frequency.

With ENABLE = H and PA_ENABLE = H the PLL, XTO, CLK driver, and the power amplifier are on. With PA_ENABLE the power amplifier can be switched on and off, which is used to perform the ASK modulation.

3.1 Description of RF Transmitter

The integrated PLL transmitter is particularly suitable for simple, low-cost RF applications. The VCO is locked to $32f_{XTAL}$ hence a 13.56MHz crystal is needed for a 433.92MHz transmitter. All other PLL and VCO peripheral elements are integrated.

The XTO is a series resonance oscillator so that only one capacitor together with a crystal connected in series to GND are needed as external elements.

The crystal oscillator together with the PLL typically needs < 1ms until the PLL is locked and the CLK output is stable. There is a wait time of ≥ 1ms until the CLK is used for the microcontroller and the PA is switched on.

The power amplifier is an open-collector output delivering a current pulse, which is nearly independent from the load impedance. Thus, the delivered output power is controllable via the connected load impedance.

This output configuration enables simple matching to any kind of antenna or to 50Ω. This results in a high power efficiency of $\eta = P_{out}/(I_{S,PA} \ V_S)$ of 36% for the power amplifier when an optimized load impedance of $Z_{Load} = (166 + j223)\Omega$ is used at 3V supply voltage.

3.2 ASK Transmission

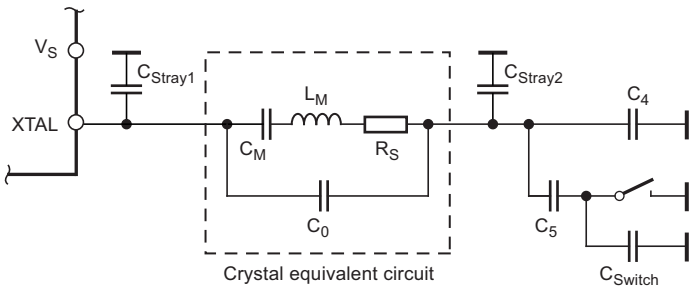
The RF TX block is activated by ENABLE = H. PA_ENABLE must remain L for t ≥1ms, then the CLK signal is taken to clock the AVR and the output power can be modulated by means of pin PA_ENABLE. After transmission, PA_ENABLE is switched to L and the microcontroller switches back to internal clocking. The RF TX is switched back to standby mode with ENABLE = L.

3.3 FSK Transmission

The RF TX is activated by ENABLE = H. PA_ENABLE must remain L for t ≥ 1ms, then the CLK signal is taken to clock the AVR® and the power amplifier is switched on with PA_ENABLE = H. The chip is then ready for FSK modulation. The AVR starts to switch on and off the capacitor between the XTAL load capacitor and GND with an open-drain output port, thus changing the reference frequency of the PLL. When the switch is closed, the output frequency is lower than when the switch is open. After transmission, PA_ENABLE is switched to L and the microcontroller switches back to internal clocking. The RF TX is switched back to standby mode with ENABLE = L.

The accuracy of the frequency deviation with XTAL pulling method is about ±25% when the following tolerances are considered.

Figure 3-1. Tolerances of Frequency Modulation



Using C_4 = 9.2pF ±2%, C_5 = 6.8pF ±5%, a switch port with C_{Switch} = 3pF ±10%, stray capacitances on each side of the crystal of C_{Stray1} = C_{Stray2} = 1pF ±10%, a parallel capacitance of the crystal of C_0 = 3.2pF ±10% and a crystal with C_M = 13fF ±10%, results in a typical FSK deviation of ±21kHz typical with worst case tolerances of ±16.3kHz to ±28.8kHz.

3.4 CLK Output

An output CLK signal is provided for the integrated AVR. The delivered signal is CMOS compatible if the load capacitance is lower than 10pF.

3.4.1 Clock Pulse Take-over

The clock of the crystal oscillator can be used for clocking the microcontroller. Atmel® AVR microcontroller starts with an integrated RC-oscillator to switch on the RF TX with ENABLE = H, and after 1ms assumes the clock signal of the transmission IC, so that the message can be sent with crystal accuracy.

3.4.2 Output Matching and Power Setting

The output power is set by the load impedance of the antenna. The maximum output power is achieved with a load impedance of $Z_{Load,opt}$ = (166 + j223)Ω. There must be a low resistive path to V_S to deliver the DC current.

The delivered current pulse of the power amplifier is 9mA and the maximum output power is delivered to a resistive load of 465Ω if the 1.0pF output capacitance of the power amplifier is compensated by the load impedance.

An optimum load impedance of:
Z_{Load} = 465Ω || j/(2 × π 1.0pF) = (166 + j223)Ω is achieved for the maximum output power of 7.5dBm.

The load impedance is defined as the impedance seen from the RF TX's ANT1, ANT2 into the matching network. This large signal load impedance should not be confused with the small signal input impedance delivered as input characteristic of RF amplifiers and measured from the application into the IC instead of from the IC into the application for a power amplifier.

Less output power is achieved by lowering the real parallel part of 465Ω where the parallel imaginary part should be kept constant.

Output power measurement can be done using the circuit shown in Figure 8-4 on page 15. Note that the component values must be changed to compensate the individual board parasitics until the RF TX has the right load impedance $Z_{Load,opt}$ = (166 + j223)Ω. In addition, the damping of the cable used to measure the output power must be calibrated out.

4. Microcontroller Block

More detailed information about the microcontroller block can be found in the appendix.

5. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Minimum	Maximum	Unit
Supply voltage	V_S		5	V
Power dissipation	P_{tot}		100	mW
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	–55	125	°C
Ambient temperature	T_{amb}	–55	125	°C
Input voltage	V_{maxPA_ENABLE}	–0.3	$(V_S + 0.3)^{(1)}$	V

Note: If V_S + 0.3 is higher than 3.7V, the maximum voltage will be reduced to 3.7V.

6. Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	35	K/W

7. Electrical Characteristics

V_S = 2.0V to 4.0V, T_{amb} = 25°C unless otherwise specified.
Typical values are given at V_S = 3.0V and T_{amb} = 25°C. All parameters are referred to GND (pin 7).

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Supply current	Power down, microcontroller watchdog timer disabled	I_{S_Off}		210	 24.35	nA µA
Supply current	Power up, 4MHz internal RC oscillator	$I_{S\_Transmit}$		9.8		mA
Output power	V_S = 3.0V, T_{amb} = 25°C, f = 433.92MHz, Z_{Load} = (166 + j233)Ω	P_{Ref}	5.5	7.5	10	dBm
Output power variation for the full temperature range	T_{amb} = 25°C, V_S = 3.0V V_S = 2.0V	 ΔP_{Ref} ΔP_{Ref}			 –1.5 –4.0	 dB dB
Output power variation for the full temperature range	T_{amb} = 25°C, V_S = 3.0V V_S = 2.0V $P_{Out} = P_{Ref} + \Delta P_{Ref}$	 ΔP_{Ref} ΔP_{Ref}			 –2.0 –4.5	 dB dB
Achievable output-power range	Selectable by load impedance	P_{Out_typ}	0		7.5	dBm
Spurious emission	$f_{CLK} = f_0/128$ Load capacitance at pin CLK = 10pF $f_O \pm 1 \times f_{CLK}$ $f_O \pm 4 \times f_{CLK}$ other spurious are lower			 –55 –52		 dBc dBc

Notes: 1. If V_S is higher than 3.6V, the maximum voltage will be reduced to 3.6V.

7. Electrical Characteristics (Continued)

V_S = 2.0V to 4.0V, T_{amb} = 25°C unless otherwise specified.
Typical values are given at V_S = 3.0V and T_{amb} = 25°C. All parameters are referred to GND (pin 7).

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Oscillator frequency XTO (= phase comparator frequency)	$f_{XTO} = f_0/32$ f_{XTAL} = resonant frequency of the XTAL, $C_M \leq 10fF$, load capacitance selected accordingly T_{amb} = 25°C	f_{XTO}	–30	f_{XTAL}	+30	ppm
PLL loop bandwidth				250		kHz
Phase noise of phase comparator	Referred to $f_{PC} = f_{XT0}$, 25kHz distance to carrier			–116	–110	dBc/Hz
In-loop phase noise PLL	25kHz distance to carrier			–86	–80	dBc/Hz
Phase noise VCO	at 1MHz at 36MHz			–94 –125	–90 –121	dBc/Hz dBc/Hz
Frequency range of VCO		f_{VCO}	429		439	MHz
Clock output frequency (CMOS microcontroller compatible)				$f_0/128$		MHz
Voltage swing at pin CLK	$C_{Load} \leq 10pF$	V_{0h} V_{0l}	$V_S \times 0.8$		 $V_S \times 0.2$	V V
Series resonance R of the crystal		Rs			110	Ω
Capacitive load at pin XT0					7	pF
FSK modulation frequency rate	Duty cycle of the modulation signal = 50%		0		32	kHz
ASK modulation frequency rate	Duty cycle of the modulation signal = 50%		0		32	kHz
ENABLE input	Low level input voltage High level input voltage Input current high	V_{Il} V_{Ih} I_{In}	 1.7		0.25 20	V V µA
PA_ENABLE input	Low level input voltage High level input voltage Input current high	V_{Il} V_{Ih} I_{In}	 1.7		0.25 V_S(1) 5	V V µA

Notes: 1. If V_S is higher than 3.6V, the maximum voltage will be reduced to 3.6V.

8. Application

For the supply-voltage blocking capacitor C_3, a value of 68nF/X7R is recommended. C_1 and C_2 are used to match the loop antenna to the power amplifier, where C_1 typically is 8.2pF/NP0 and C_2 is 6pF/NP0 (10pF + 15pF in series); for C_2 two capacitors in series should be used to achieve a better tolerance value and to have the possibility of realizing the $Z_{Load,opt}$ by using standard valued capacitors.

Together with the pins and the PCB board wires C_1 forms a series resonance loop that suppresses the 1st harmonic, hence the position of C_1 on the PCB is important. Normally the best suppression is achieved when C_1 is placed as close as possible to the pins ANT1 and ANT2.

The loop antenna should not exceed a width of 1.5mm, otherwise the Q-factor of the loop antenna is too high.

L_1 (50nH to 100nH) can be printed on PCB. C_4 should be selected that the XTO runs on the load resonance frequency of the crystal. Normally, a value of 12pF results for a 15pF load-capacitance crystal.

Figure 8-1. ESD Protection Circuit

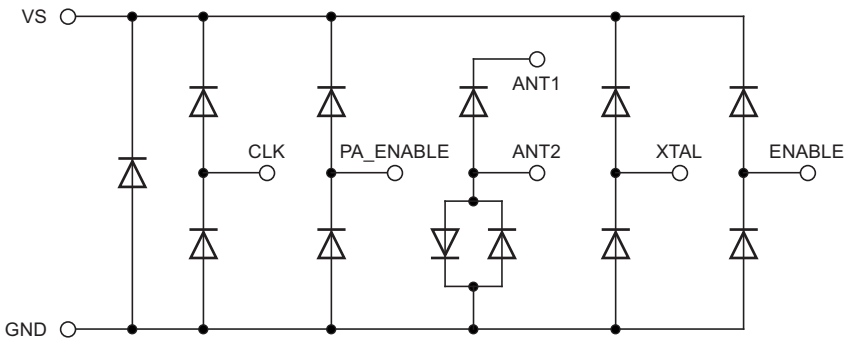


Figure 8-2. Typical ASK Application ATA8742

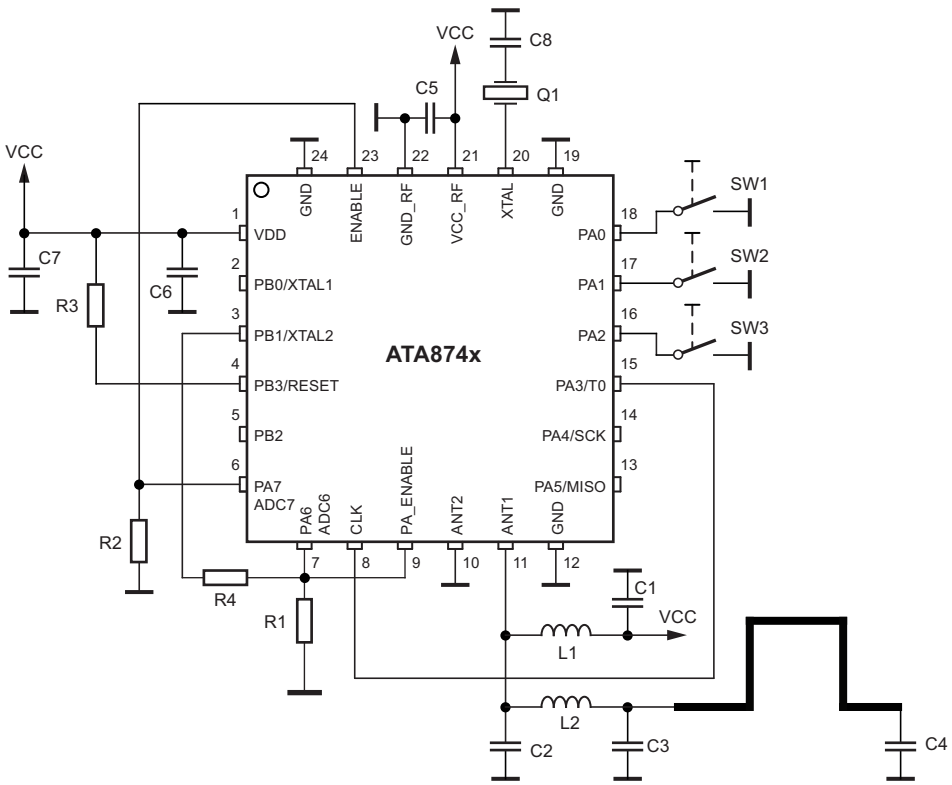
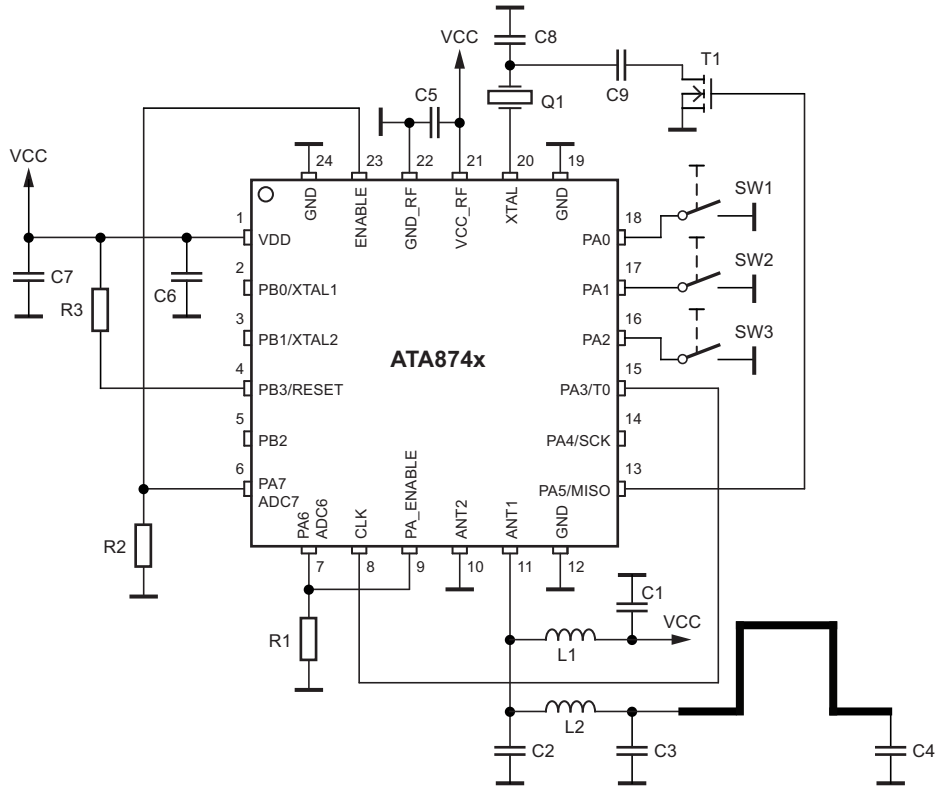


Table 8-1. Bill of Material

Component	Value			Type/ Manufacturer	Note
	315MHz	433.92MHz	868.3MHz		
L1	100nH	82nH	22nH	LL1608-FSL/ TOKO	
L2	39nH	27nH	2.2nH	LL1608-FSL/ TOKO	
C1	1nF	1nF	1nF	GRM1885C/ Murata	
C2	3.9pF	2.7pF	1.5pF	GRM1885C/ Murata	This cap must be placed as close as possible to the pin Ant1 and Ant2
C3	27pF	16pF	4.3pF	GRM1885C/ Murata	On the demo board 2 capacitors in series are used to reduce the tolerance
C4	3.9pF	1.6pF	0.3pF	GRM1885C/ Murata	On the demo board 2 capacitors in series are used to reduce the tolerance
C5	68nF	68nF	68nF	GRM188R71C /Murata	This cap must placed as close as possible to the VCC_RF
C6	100nF	100nF	100nF	GRM188R71C /Murata	This cap must placed as close as possible to the VDD
C7	100nF	100nF	100nF	GRM188R71C /Murata	
C8	10pF	12pF	12pF	GRM1885C/ Murata	
Q1	9.843750 MHz	13.56MHz	13.567187 MHz	DSX530GK/ KDS	
R1	100kΩ	100kΩ	100kΩ		
R2	100kΩ	100kΩ	100kΩ		
R3	10kΩ	10kΩ	10kΩ		
R4	1.8kΩ	1.8kΩ	1.8kΩ		This resistor can be resigned if the ASK modulation is performed using PA5 (MISO).

Figure 8-3. Typical FSK Application ATA8742



Note: FSK modulation is achieved by switching on and off an additional capacitor between the XTAL load capacitor and GND. This is done using a MOS switch controlled by a microcontroller output.

Table 8-2. Bill of Material

Component	Value			Type/ Manufacturer	Note
	315MHz	433.92MHz	868.3MHz		
L1	100nH	82nH	22nH	LL1608-FSL/ TOKO	
L2	39nH	27nH	2.2nH	LL1608-FSL/ TOKO	
C1	1nF	1nF	1nF	GRM1885C/ Murata	
C2	3.9pF	2.7pF	1.5pF	GRM1885C/ Murata	This cap must be placed as close as possible to the pin Ant1 and Ant2
C3	27pF	16pF	4.3pF	GRM1885C/ Murata	On the demo board 2 capacitors in series are used to reduce the tolerance
C4	3.9pF	1.6pF	0.3pF	GRM1885C/ Murata	On the demo board 2 capacitors in series are used to reduce the tolerance
C5	68nF	68nF	68nF	GRM188R71C / Murata	This cap must placed as close as possible to the VCC_RF
C6	100nF	100nF	100nF	GRM188R71C / Murata	This cap must placed as close as possible to the VDD
C7	100nF	100nF	100nF	GRM188R71C / Murata	

Table 8-2. Bill of Material (Continued)

Component	Value			Type/ Manufacturer	Note
C8	3.9pF	4.7pF	5.6pF	GRM1885C/ Murata	Frequency deviation of ±16kHz will be performed using the combination of C8 and C9
C9	18pF	8.2pF	5.6pF	GRM1885C/ Murata	Frequency deviation of ±16kHz will be performed using the combination of C8 and C9
T1				BSS83	
Q1	9.843750 MHz	13.56MHz	13.567187 MHz	DSX530GK/ KDS	
R1	100kΩ	100kΩ	100kΩ		
R2	100kΩ	100kΩ	100kΩ		
R3	10kΩ	10kΩ	10kΩ		
R4	1.8kΩ	1.8kΩ	1.8kΩ		

Table 8-3. Transmitter Pin Cross Reference List

Pin Name	Pin Number ATA8401/02/03	Pin Number ATA8741/42/43
CLK	1	8
PA_ENABLE	2	9
ANT2	3	10
ANT1	4	11
XTAL	5	20
VS	6	21
GND	7	22
ENABLE	8	23

Note: For the Atmel® ATA8742, the following points differs from the datasheets:
- The temperature range is limited to –40°C to +85°C
- ESD protection: HBM 2500V, MM 100V, CDM 1000V
- Figure 8-4: Two output power measurement
- For FSK modulation, an additional MOS switch is required

Figure 8-4. Output Power Measurement ATA8742

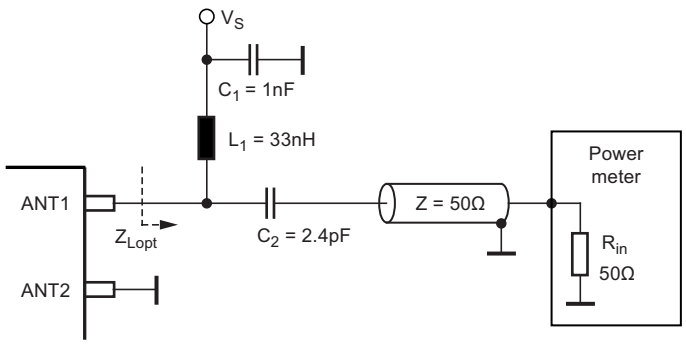


Table 8-4. Microcontroller Cross Reference List

Pin Name	Pin Number ATtiny44V	Pin Number ATA8741/ATA8742/ATA8743
VCC	1	1
PB0	2	2
PB1	3	3
PB3/NRESET	4	4
PB2	5	5
PA7	6	6
PA6/MOSI	7	7
PA5/MISO	8	13
PA4/USCK	9	14
PA3/T0	10	15
PA2	11	16
PA1	12	17
PA0	13	18
GND	14	19

Note: For the Atmel® ATA8741/ATA8742/ATA8743, the following points differs from the Atmel ATtiny44V datasheet:
- The temperature range is limited to –40°C to +85°C
- The supply voltage range is limited from 2.0V to 4.0V

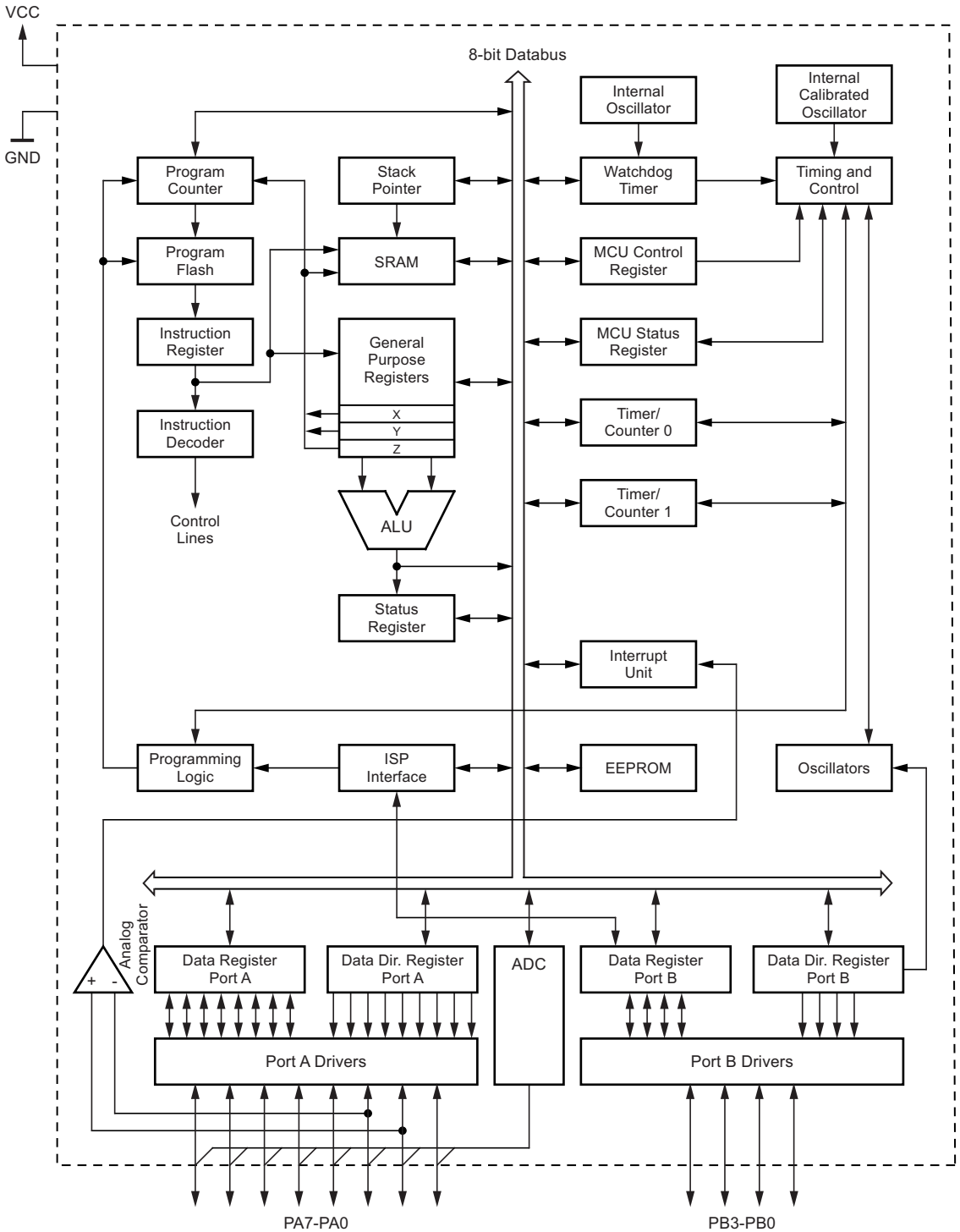
Appendix 1: Microcontroller ATtiny24/44/84

9. Overview

The Atmel® ATtiny24/44/84 is a low-power CMOS 8-bit microcontroller based on the AVR® enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATtiny24/44/84 achieves throughputs approaching 1MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

9.1 Block Diagram

Figure 9-1. Block Diagram



The AVR® core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The Atmel® ATtiny24/44/84 provides the following features: 2/4/8K byte of in-system programmable flash, 128/256/512 bytes EEPROM, 128/256/512 bytes SRAM, 12 general purpose I/O lines, 32 general purpose working registers, a 8-bit Timer/Counter with two PWM channels, a 16-bit Timer/Counter with two PWM channels, internal and external interrupts, a 8-channel 10-bit ADC, programmable gain stage (1x, 20x) for 12 differential ADC channel pairs, a programmable watchdog timer with internal oscillator, internal calibrated oscillator, and three software selectable power saving modes. The idle mode stops the CPU while allowing the SRAM, Timer/Counter, ADC, analog comparator, and interrupt system to continue functioning. The power-down mode saves the register contents, disabling all chip functions until the next interrupt or hardware reset. The ADC noise reduction mode stops the CPU and all I/O modules except ADC, to minimize switching noise during ADC conversions. In standby mode, the crystal/resonator oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low power consumption.

The device is manufactured using Atmel high density non-volatile memory technology. The on-chip ISP flash allows the program memory to be re-programmed in-system through an SPI serial interface, by a conventional non-volatile memory programmer or by an on-chip boot code running on the AVR core.

The Atmel ATtiny24/44/84 AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

9.2 Automotive Quality Grade

The ATtiny24/44/84 have been developed and manufactured according to the most stringent requirements of the international standard ISO-TS-16949 grade 1. This data sheet contains limit values extracted from the results of extensive characterization (Temperature and Voltage). The quality and reliability of the ATtiny24/44/84 have been verified during regular product qualification as per AEC-Q100.

As indicated in the ordering information paragraph, the product is available in only one temperature grade,

Table 9-1. Temperature Grade Identification for Automotive Products

Temperature	Temperature Identifier	Comments
–40; +125	Z	Full automotive temperature range

9.3 Pin Descriptions

9.3.1 VCC

Supply voltage.

9.3.2 GND

Ground.

9.3.3 Port B (PB3...PB0)

Port B is a 4-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The port B output buffers have symmetrical drive characteristics with both high sink and source capability except PB3 which has the $\overline{\text{RESET}}$ capability.

To use pin PB3 as an I/O pin, instead of RESET pin, program (‘0’) RSTDISBL fuse. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the Atmel ATtiny24/44/84 as listed on Section 19.3 “Alternate Port Functions” on page 68.

9.3.4 $\overline{\text{RESET}}$

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in Figure 16-1 on page 50. Shorter pulses are not guaranteed to generate a reset.

9.3.5 Port A (PA7...PA0)

Port A is a 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The port A output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, port A pins that are externally pulled low will source current if the pull-up resistors are activated. The port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port A has an alternate functions as analog inputs for the ADC, analog comparator, Timer/Counter, SPI and pin change interrupt as described in Section 19.3 “Alternate Port Functions” on page 68

10. Resources

A comprehensive set of development tools, drivers and application notes, and datasheets are available for download on http://www.atmel.com/avr.

11. About Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

For I/O registers located in extended I/O map, “IN”, “OUT”, “SBIS”, “SBIC”, “CBI”, and “SBI” instructions must be replaced with instructions that allow access to extended I/O. Typically “LDS” and “STS” combined with “SBRS”, “SBRC”, “SBR”, and “CBR”.

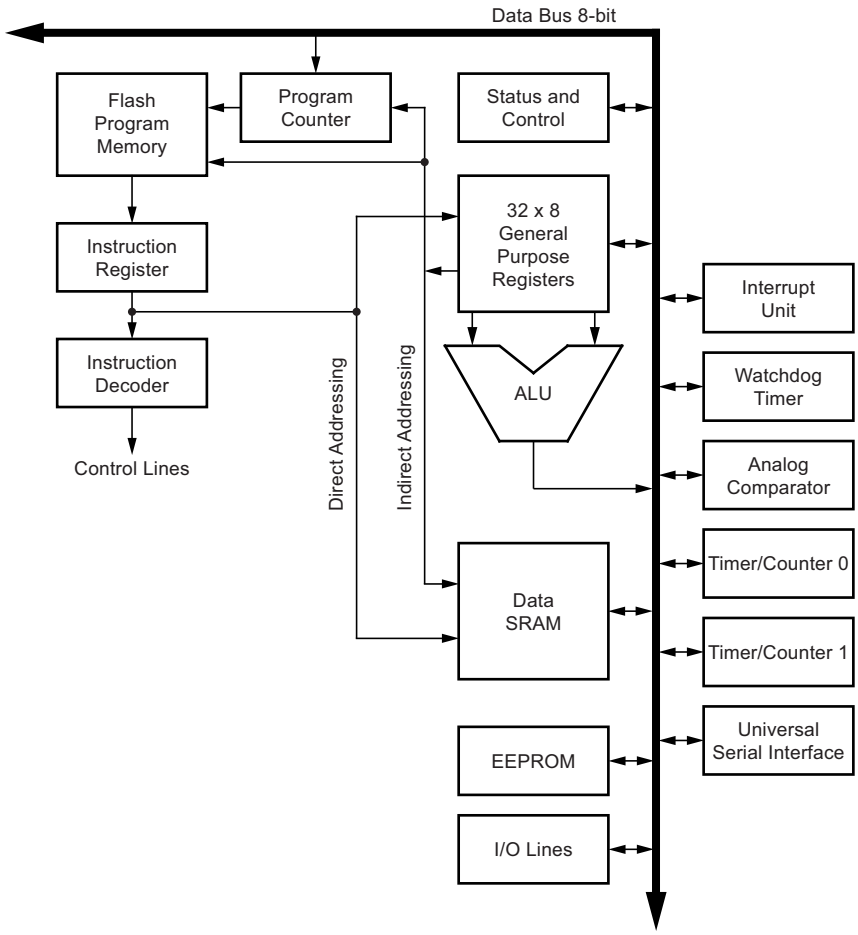
12. CPU Core

12.1 Overview

This section discusses the AVR® core architecture in general. The main function of the CPU core is to ensure correct program execution. The CPU must therefore be able to access memories, perform calculations, control peripherals, and handle interrupts.

12.2 Architectural Overview

Figure 12-1. Block Diagram of the AVR Architecture



In order to maximize performance and parallelism, the AVR uses a Harvard architecture – with separate memories and buses for program and data. Instructions in the program memory are executed with a single level pipelining. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This concept enables instructions to be executed in every clock cycle. The program memory is in-system reprogrammable flash memory.

The fast-access register file contains 32 x 8-bit general purpose working registers with a single clock cycle access time. This allows single-cycle arithmetic logic unit (ALU) operation. In a typical ALU operation, two operands are output from the register file, the operation is executed, and the result is stored back in the register file – in one clock cycle.

Six of the 32 registers can be used as three 16-bit indirect address register pointers for data space addressing – enabling efficient address calculations. One of the these address pointers can also be used as an address pointer for look up tables in flash program memory. These added function registers are the 16-bit X-, Y-, and Z-register, described later in this section.

The ALU supports arithmetic and logic operations between registers or between a constant and a register. Single register operations can also be executed in the ALU. After an arithmetic operation, the status register is updated to reflect information about the result of the operation.

Program flow is provided by conditional and unconditional jump and call instructions, able to directly address the whole address space. Most AVR® instructions have a single 16-bit word format. Every program memory address contains a 16- or 32-bit instruction.

During interrupts and subroutine calls, the return address program counter (PC) is stored on the stack. The stack is effectively allocated in the general data SRAM, and consequently the stack size is only limited by the total SRAM size and the usage of the SRAM. All user programs must initialize the SP in the reset routine (before subroutines or interrupts are executed). The stack pointer (SP) is read/write accessible in the I/O space. The data SRAM can easily be accessed through the five different addressing modes supported in the AVR architecture.

The memory spaces in the AVR architecture are all linear and regular memory maps.

A flexible interrupt module has its control registers in the I/O space with an additional global interrupt enable bit in the status register. All interrupts have a separate interrupt vector in the interrupt vector table. The interrupts have priority in accordance with their interrupt vector position. The lower the interrupt vector address, the higher the priority.

The I/O memory space contains 64 addresses for CPU peripheral functions as control registers, SPI, and other I/O functions. The I/O memory can be accessed directly, or as the data space locations following those of the register file, 0x20 - 0x5F.

12.3 ALU – Arithmetic Logic Unit

The high-performance AVR ALU operates in direct connection with all the 32 general purpose working registers. Within a single clock cycle, arithmetic operations between general purpose registers or between a register and an immediate are executed. The ALU operations are divided into three main categories – arithmetic, logical, and bit-functions. Some implementations of the architecture also provide a powerful multiplier supporting both signed/unsigned multiplication and fractional format. See the “Instruction Set” section for a detailed description.

12.4 Status Register

The status register contains information about the result of the most recently executed arithmetic instruction. This information can be used for altering program flow in order to perform conditional operations. Note that the status register is updated after all ALU operations, as specified in the instruction set reference. This will in many cases remove the need for using the dedicated compare instructions, resulting in faster and more compact code.

The status register is not automatically stored when entering an interrupt routine and restored when returning from an interrupt. This must be handled by software.

12.4.1 SREG – AVR Status Register

Bit	7	6	5	4	3	2	1	0	
0x3F (0x5F)	**I**	**T**	**H**	**S**	**V**	**N**	**Z**	**C**	**SREG**
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – I: Global Interrupt Enable**

The global interrupt enable bit must be set for the interrupts to be enabled. The individual interrupt enable control is then performed in separate control registers. If the global interrupt enable register is cleared, none of the interrupts are enabled independent of the individual interrupt enable settings. The I-bit is cleared by hardware after an interrupt has occurred, and is set by the RETI instruction to enable subsequent interrupts. The I-bit can also be set and cleared by the application with the SEI and CLI instructions, as described in the instruction set reference.

- **Bit 6 – T: Bit Copy Storage**

The bit copy instructions BLD (Bit LoaD) and BST (Bit STore) use the T-bit as source or destination for the operated bit. A bit from a register in the register file can be copied into T by the BST instruction, and a bit in T can be copied into a bit in a register in the register file by the BLD instruction.

- **Bit 5 – H: Half Carry Flag**

The half carry flag H indicates a half carry in some arithmetic operations. Half carry is useful in BCD arithmetic. See the “Instruction Set Description” for detailed information.

- **Bit 4 – S: Sign Bit, S = N ⊕ V**

The S-bit is always an exclusive or between the negative flag N and the two’s complement overflow flag V. See the “Instruction Set Description” for detailed information.

- **Bit 3 – V: Two’s Complement Overflow Flag**

The two’s complement overflow flag V supports two’s complement arithmetics. See the “Instruction Set Description” for detailed information.

- **Bit 2 – N: Negative Flag**

The negative flag N indicates a negative result in an arithmetic or logic operation. See the “Instruction Set Description” for detailed information.

- **Bit 1 – Z: Zero Flag**

The zero flag Z indicates a zero result in an arithmetic or logic operation. See the “Instruction Set Description” for detailed information.

- **Bit 0 – C: Carry Flag**

The carry flag C indicates a carry in an arithmetic or logic operation. See the “Instruction Set Description” for detailed information.

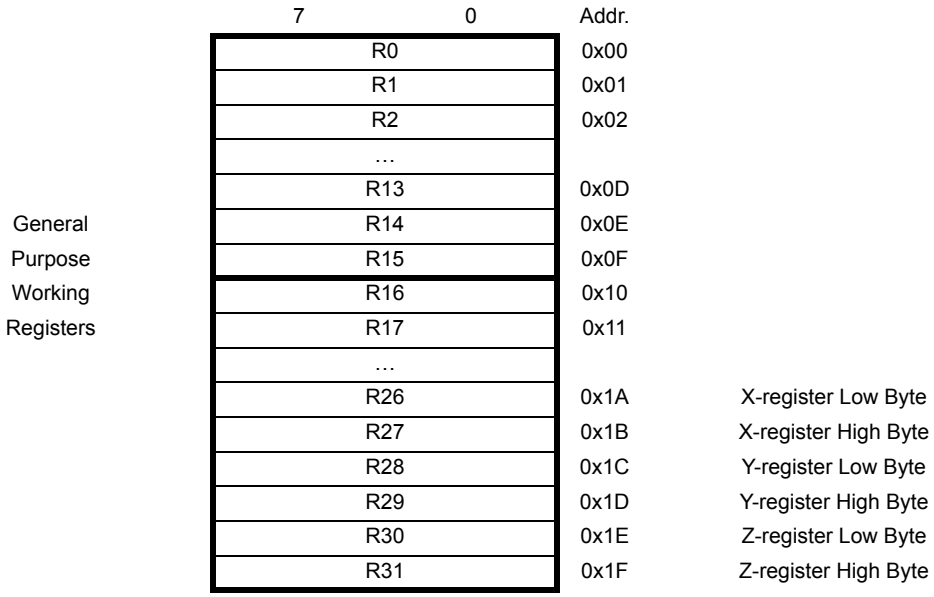
12.5 General Purpose Register File

The register file is optimized for the AVR® enhanced RISC instruction set. In order to achieve the required performance and flexibility, the following input/output schemes are supported by the register file:

- One 8-bit output operand and one 8-bit result input
- Two 8-bit output operands and one 8-bit result input
- Two 8-bit output operands and one 16-bit result input
- One 16-bit output operand and one 16-bit result input

Figure 12-2 shows the structure of the 32 general purpose working registers in the CPU.

Figure 12-2. AVR CPU General Purpose Working Registers



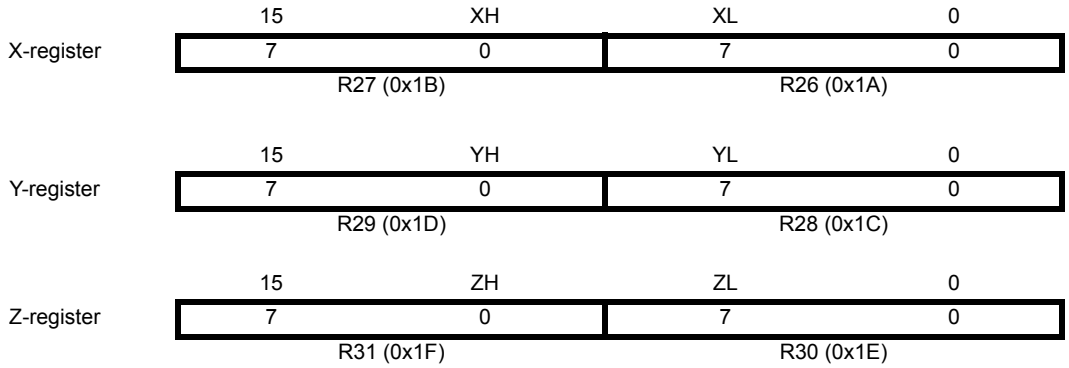
Most of the instructions operating on the register file have direct access to all registers, and most of them are single cycle instructions.

As shown in Figure 12-2 on page 24, each register is also assigned a data memory address, mapping them directly into the first 32 locations of the user data space. Although not being physically implemented as SRAM locations, this memory organization provides great flexibility in access of the registers, as the X-, Y- and Z-pointer registers can be set to index any register in the file.

12.5.1 The X-register, Y-register, and Z-register

The registers R26..R31 have some added functions to their general purpose usage. These registers are 16-bit address pointers for indirect addressing of the data space. The three indirect address registers X, Y, and Z are defined as described in Figure 12-3 on page 25.

Figure 12-3. The X-, Y-, and Z-registers



In the different addressing modes these address registers have functions as fixed displacement, automatic increment, and automatic decrement (see the instruction set reference for details).

12.6 Stack Pointer

The stack is mainly used for storing temporary data, for storing local variables and for storing return addresses after interrupts and subroutine calls. The stack pointer register always points to the top of the stack. Note that the stack is implemented as growing from higher memory locations to lower memory locations. This implies that a stack PUSH command decreases the stack pointer.

The stack pointer points to the data SRAM stack area where the subroutine and interrupt stacks are located. This stack space in the data SRAM must be defined by the program before any subroutine calls are executed or interrupts are enabled. The stack pointer must be set to point above 0x60. The stack pointer is decremented by one when data is pushed onto the stack with the PUSH instruction, and it is decremented by two when the return address is pushed onto the stack with subroutine call or interrupt. The stack pointer is incremented by one when data is popped from the stack with the POP instruction, and it is incremented by two when data is popped from the stack with return from subroutine RET or return from interrupt RETI.

The AVR® stack pointer is implemented as two 8-bit registers in the I/O space. The number of bits actually used is implementation dependent. Note that the data space in some implementations of the AVR architecture is so small that only SPL is needed. In this case, the SPH register will not be present.

12.6.1 SPH and SPL – Stack Pointer High and Low

Bit	15	14	13	12	11	10	9	8	
0x3E (0x5E)	**SP15**	**SP14**	**SP13**	**SP12**	**SP11**	**SP10**	**SP9**	**SP8**	**SPH**
0x3D (0x5D)	**SP7**	**SP6**	**SP5**	**SP4**	**SP3**	**SP2**	**SP1**	**SP0**	**SPL**
	7	6	5	4	3	2	1	0	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	