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ATBTLC1000 WLCSP SoC

Ultra Low Power BLE 4.1 SoC

DATASHEET

Description

The Atmel® ATBTLC1000 is an ultra-low power Bluetooth® SMART (BLE 4.1) System on a Chip with Integrated MCU, Transceiver, Modem, MAC, PA, TR Switch, and Power Management Unit (PMU). It can be used as a Bluetooth Low Energy link controller or data pump with external host MCU or as a standalone applications processor with embedded BLE connectivity and external memory.

The qualified Bluetooth Smart protocol stack is stored in dedicated ROM. The firmware includes L2CAP service layer protocols, Security Manager, Attribute protocol (ATT), Generic Attribute Profile (GATT), and the Generic Access Profile (GAP). Additionally, application profiles such as Proximity, Thermometer, Heart Rate, Blood Pressure, and many others are supported and included in the protocol stack.

Features

- Complies with Bluetooth V4.1, ETSI EN 300 328 and EN 300 440 Class 2, FCC CFR47 Part 15 and ARIB STD-T66
- 2.4GHz transceiver and modem
  - -95dBm/-93dBm programmable receiver sensitivity
  - -20 to +3.5dBm programmable TX output power
  - Integrated T/R switch
  - Single wire antenna connection
- ARM® Cortex®-M0 32-bit processor
  - Single wire Debug (SWD) interface
  - Four-channel DMA controller
  - Brownout detector and Power On Reset
  - Watch Dog Timer
- Memory
  - 128kB embedded RAM (96kB available for application)
  - 128kB embedded ROM
- Hardware Security Accelerators
  - AES-128
  - SHA-256
- Peripherals
  - 10 digital and one wakeup GPIOs with 96kΩ internal pull-up resistors, one Mixed Signal GPIO
  - 2x SPI Master/Slave
  - 2x I^2C Master/Slave and 1x I^2C Slave
  - 2x UART
  - 1x SPI Flash
  - Three-Axis quadrature decoder
  - 4x Pulse Width Modulation (PWM), three General Purpose Timers, and one Wakeup Timer

  - 1-channel 11-bit ADC
- Clock
  - Integrated 26MHz RC oscillator
  - 26MHz crystal oscillator
  - Integrated 2MHz sleep RC oscillator
  - 32.768kHz RTC crystal oscillator
- Ultra-low power
  - 1.1µA sleep current (8KB RAM retention and RTC running)
  - 3.0mA peak TX current (0dBm, 3.6V)
  - 4.0mA peak RX current (3.6V, -93dBm sensitivity)
  - 9.7µA average advertisement current (three channels, 1s interval)
- Integrated Power management
  - 1.8 to 4.3V battery voltage range
  - Fully integrated Buck DC/DC converter
- Bluetooth SIG Certification
  - QD ID Controller (see declaration D028678)
  - QD ID Host (see declaration D028679)

Table of Contents

1 Ordering Information

Ordering code	Package	Description
ATBTLC1000A-UU-T	31L WLCSP	ATBTLC1000 Tape and Reel

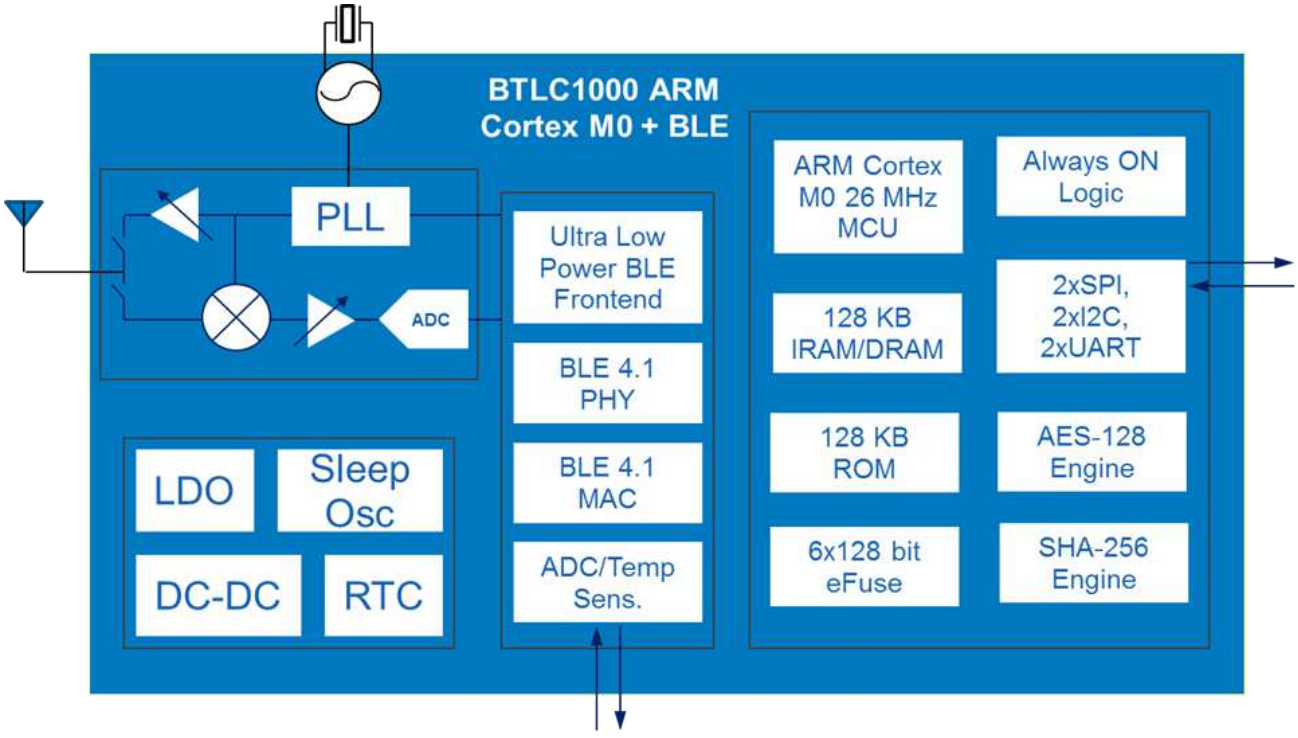
2 Package Information

Table 2-1. ATBTLC1000 31L WLCSP Package Information

Parameter	Value	Tolerance	Units
Package size	2.262 × 2.142	±0.03	mm
Total thickness	0.502	±0.039	
I/O pitch	0.35		
Ball diameter	0.2	±0.03	
Ball count	31		

3 Block Diagram

Figure 3-1. ATBTLC1000 Block Diagram



4 Pinout Information

The ATBTLC1000 is offered in a 0.35mm-pitch staggered SAC405 balls 31L WLCSP package. The WLCSP package pin assignment is shown in Figure 4-1. The color shading is used to indicate the pin type as follows:

- Red – analog
- Green – digital I/O (switchable power domain)
- Blue – digital I/O (always-on power domain)
- Yellow – digital power, purple – PMU
- Green/red – configurable mixed-signal GPIO (digital/analog)

The ATBTLC1000 pins are described in Table 4-1.

Figure 4-1. ATBTLC1000 WLCSP Pin Assignment

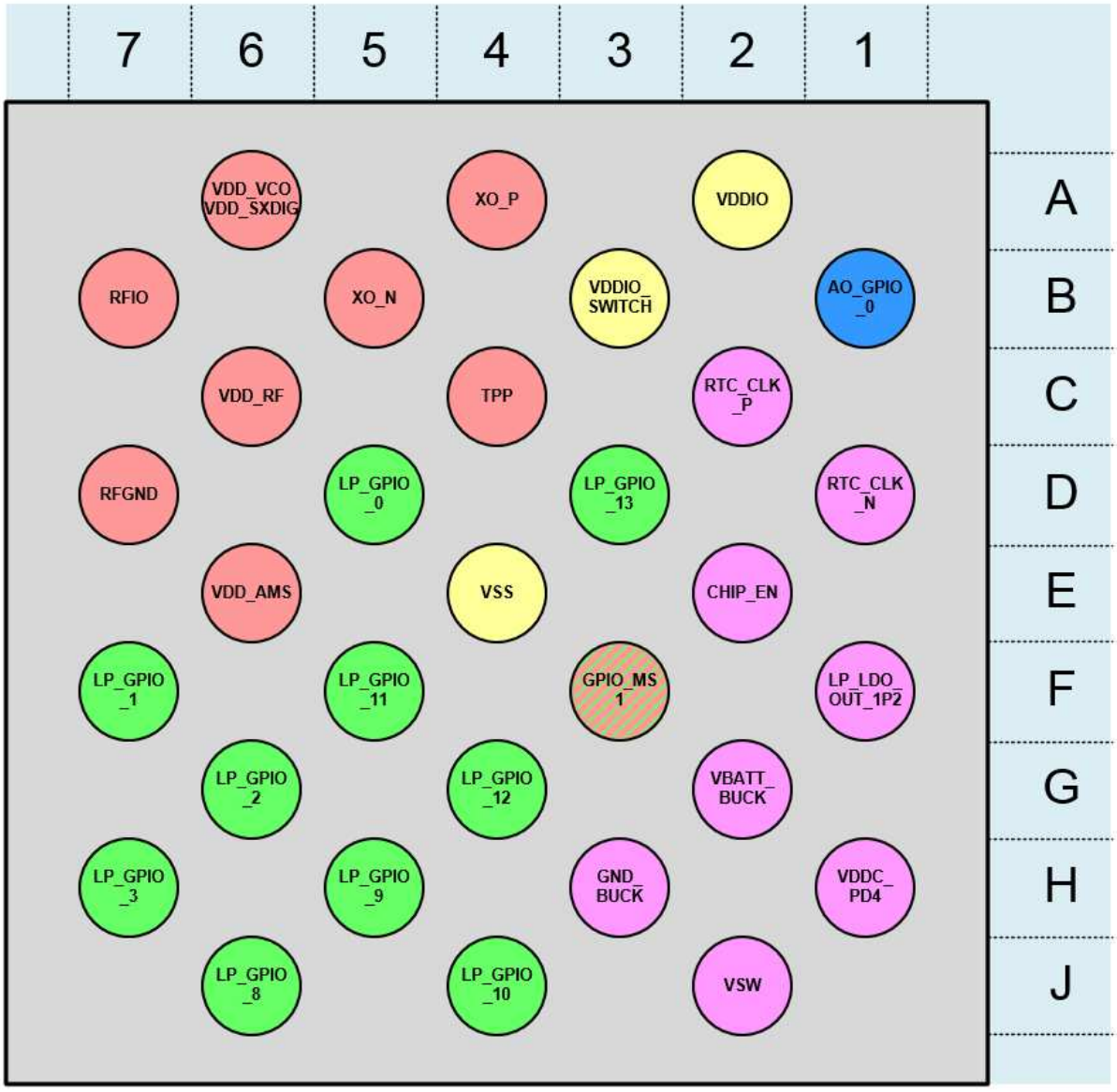


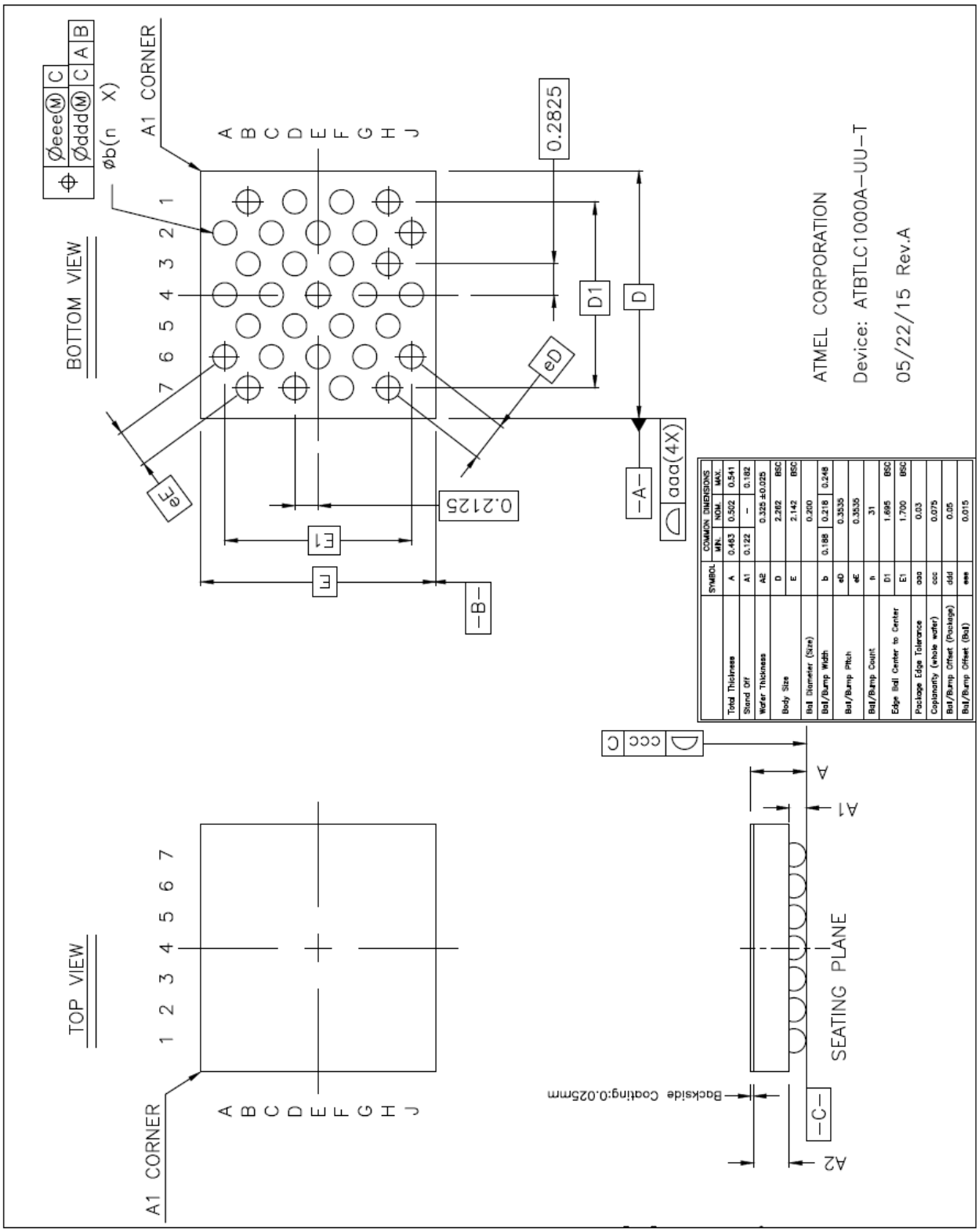
Table 4-1. ATBTLC1000 WLCSP Pin Description

Pin #	Pin Name	Pin Type	Description / Default Function
A2	VDDIO	Digital Power	I/O Supply, can be less than or equal to VBATT_BUCK
A4	XO_P	Analog/RF	XO Crystal +
A6	VDD_VCO & VDD_SXDIG	Analog/RF	Synthesizer VCO and Digital Supplies 1.2V
B1	AO_GPIO_0	Digital I/O	Always-on External Wakeup
B3	VDDIO_SWITCH	Digital Power	I/O supply switch for external flash
B5	XO_N	Analog/RF	XO Crystal -
B7	RFIO	Analog/RF	RX input and TX output
C2	RTC_CLK_P	PMU	RTC terminal + / 32.768kHz XTAL +
C4	TPP	Analog/RF	Test MUX + output
C6	VDD_RF	Analog/RF	RF Supply 1.2V
D1	RTC_CLK_N	PMU	RTC terminal – / 32.768kHz XTAL -
D3	LP_GPIO_13	Digital I/O	SPI MISO/SPI FLASH RXD
D5	LP_GPIO_0	Digital I/O	SWD Clock
D7	RFGND	Analog/RF	RF Ground
E2	CHIP_EN	PMU	Master Enable for chip
E4	VSS	Digital Power	Digital I/O and Core Ground
E6	VDD_AMS	Analog/RF	AMS Supply 1.2V
F1	LP_LDO_OUT_1P2	PMU	Low Power LDO output (connect to 1µF decoupling cap)
F3	GPIO_MS1	Mixed Signal I/O	Configurable to be a GPIO Mixed Signal only (ADC interface)
F5	LP_GPIO_11	Digital I/O	SPI MOSI/SPI FLASH TXD
F7	LP_GPIO_1	Digital I/O	SWD I/O
G2	VBATT_BUCK	PMU	DC/DC Converter Supply and General Battery Connection
G4	LP_GPIO_12	Digital I/O	SPI SSN/SPI FLASH SSN
G6	LP_GPIO_2	Digital I/O	UART RXD
H1	VDDC_PD4	PMU	DC/DC Converter 1.2V output and feedback node
H3	GND_BUCK	PMU	DC/DC Converter Ground
H5	LP_GPIO_9	Digital I/O	I^2C SCL (high-drive pad, see Table 13-3)
H7	LP_GPIO_3	Digital I/O	UART TXD
J2	VSW	PMU	DC/DC Converter Switching Node
J4	LP_GPIO_10	Digital I/O	SPI SCK/SPI FLASH SCK
J6	LP_GPIO_8	Digital I/O	I^2C SDA (high-drive pad, see Table 13-3)

5 Package Drawing

The ATBTLC1000 WLCSP package is RoHS/green compliant.

Figure 5-1. ATBTLC1000 31L WLCSP Package Outline Drawing



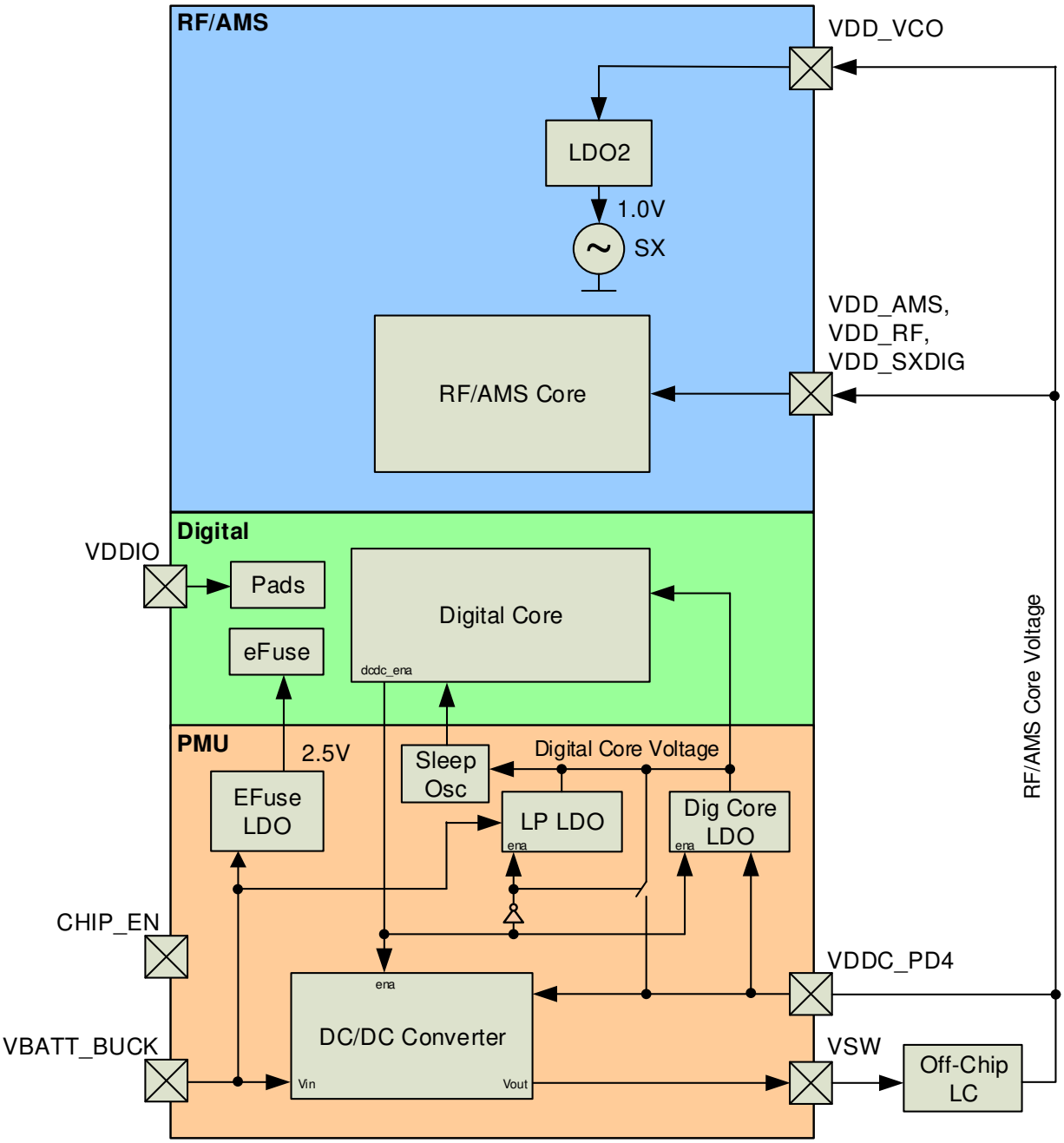
SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.
Total Thickness A	0.463	0.502	0.541
Stand Off A1	0.122	–	0.162
Wafer Thickness A2		0.325 ±0.025	
Body Size D		2.282	BSC
Body Size E		2.142	BSC
Ball Diameter (Size) b		0.200	
Ball/Bump Width b	0.188	0.218	0.248
Ball/Bump Pitch eD		0.3535	
Ball/Bump Pitch eE		0.3535	
Ball/Bump Count n		31	
Edge Ball Center to Center D1		1.695	BSC
Edge Ball Center to Center E1		1.700	BSC
Package Edge Tolerance aaa		0.03	
Coplanarity (whole wafer) ccc		0.075	
Ball/Bump Offset (Package) ddd		0.05	
Ball/Bump Offset (Ball) eee		0.015	

6 Power Management

6.1 Power Architecture

ATBTLC1000 uses an innovative power architecture to eliminate the need for external regulators and reduce the number of off-chip components. The integrated power management block includes a DC/DC buck converter and separate Low Drop out (LDO) regulators for different power domains. The DC/DC buck converter converts battery voltage to a lower internal voltage for the different circuit blocks and does this with high efficiency. The DC/DC requires three external components for proper operation (two inductors L 4.7µH and 9.1nH, and one capacitor C 4.7µF).

Figure 6-1. ATBTLC1000 Power Architecture



6.2 DC/DC Converter

The DC/DC Converter is intended to supply current to the BLE digital core and the RF transceiver core. The DC/DC consists of a power switch, 26MHz RC oscillator, controller, external inductor, and external capacitor. The DC/DC is utilizing pulse skipping discontinuous mode as its control scheme. The DC/DC specifications are shown in the following tables and figures.

Table 6-1. DC/DC Converter Specifications (Performance is Guaranteed for (L) 4.7µH and (C) 4.7µF

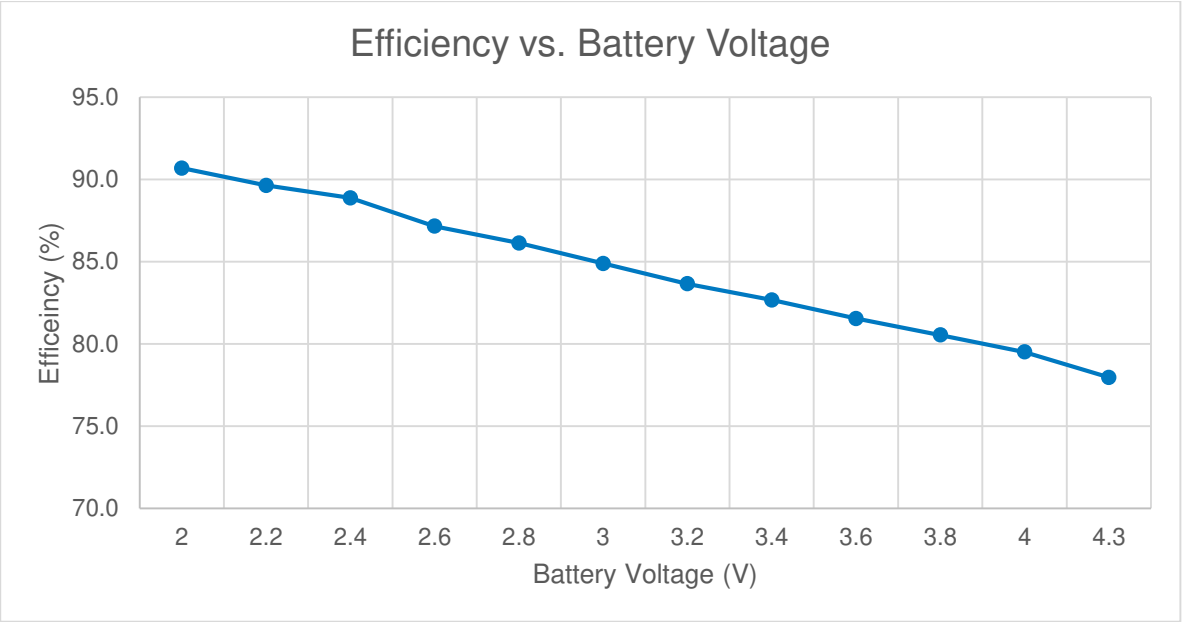
Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Output current capability	I_{REG}	0	10	30	mA	Dependent on external component values and DC/DC settings with acceptable efficiency
External capacitor range	C_{EXT}	4.7 -10%	4.7	20	µF	External capacitance range
External inductor range	L_{EXT}	2.2 -10%	4.7	4.7 +10%	µH	External inductance range
Battery voltage	V_{BAT}	2.35	3	4.3	V	Functionality and stability given
Output voltage range	V_{REG}	1.05	1.2	1.47		25mV step size
Current consumption	I_{DD}		125		µA	DC/DC quiescent current
Startup time	$t_{startup}$	50		600	µs	Dependent on external component values and DC/DC settings
Voltage ripple	ΔV_{REG}	5	10	30	mV	Dependent on external component values and DC/DC settings
Efficiency	η		85		%	Measured at 3V VBAT, at load of 10mA
Overshoot at startup	V_{OS}		0		mV	No overshoot, no output pre-charge
Line Regulation	ΔV_{REG}		10			From 1.8 to 4.3V
Load regulation	ΔV_{REG}		5			From 0 to 10mA

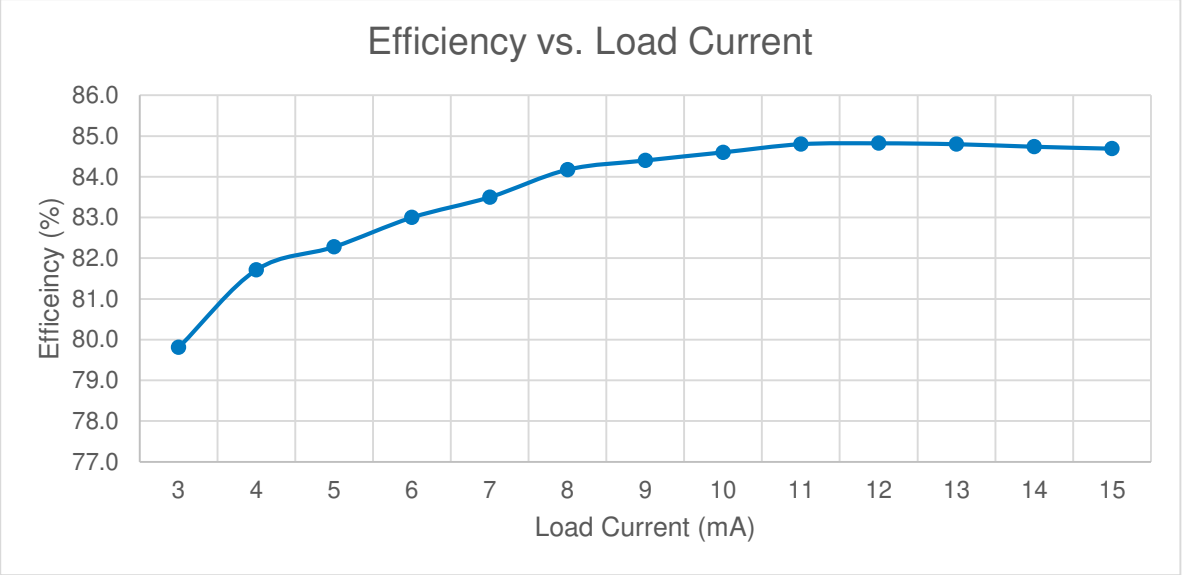
Table 6-2. DC/DC Converter Allowable Onboard Inductor and Capacitor Values (VBAT = 3V)

Inductor [µH]	Efficiency [%]	Vripple [mV]			RX Sensitivity (1) [dBm]
		C=2.2µF	C=4.7µF	C=10µF	
2.2	83	N/A	<5	<5	~1.5 dB degrade
4.7	85	9	5	<5	~0.7 dB degrade

Note: 1. Degradation relative to design powered by external LDO and DC/DC disabled.

Figure 6-2. DC/DC Converter Efficiency





6.3 Power Consumption

6.3.1 Description of Device States

ATBTLC1000 has multiple device states, depending on the state of the ARM processor and BLE subsystem.

Note: The ARM is required to be powered on if the BLE subsystem is active.

- BLE_On_Transmit – Device is actively transmitting a BLE signal (Application may or may not be active)
- BLE_On_Receive – Device is actively receiving a BLE signal (Application may or may not be active)
- MCU_Only – Device has ARM processor powered on and BLE subsystem powered down
- Ultra_Low_Power – BLE is powered down and Application is powered down (with or without RAM retention)
- Power_Down – Device core supply off

6.3.2 Controlling the Device States

The following pins are used to switch between the main device states:

- CHIP_EN – used to enable PMU
- VDDIO – I/O supply voltage from external supply

In Power_Down state, VDDIO is on and CHIP_EN is low (at GND level). To switch between Power_Down state and MCU_Only state CHIP_EN has to change between low and high (VDDIO voltage level). Once the device is MCU_Only state, all other state transitions are controlled entirely by software. When VDDIO is off and CHIP_EN is low, the chip is powered off with no leakage.

When no power is supplied to the device (the DC/DC Converter output and VDDIO are both off and at ground potential), a voltage cannot be applied to the ATBTLC1000 pins because each pin contains an ESD diode from the pin to supply. This diode will turn on when voltage higher than one diode-drop is supplied to the pin.

If a voltage must be applied to the signal pads while the chip is in a low power state, the VDDIO supply must be on, so the Power_Down state must be used. Similarly, to prevent the pin-to-ground diode from turning on, do not apply a voltage that is more than one diode-drop below ground to any pin.

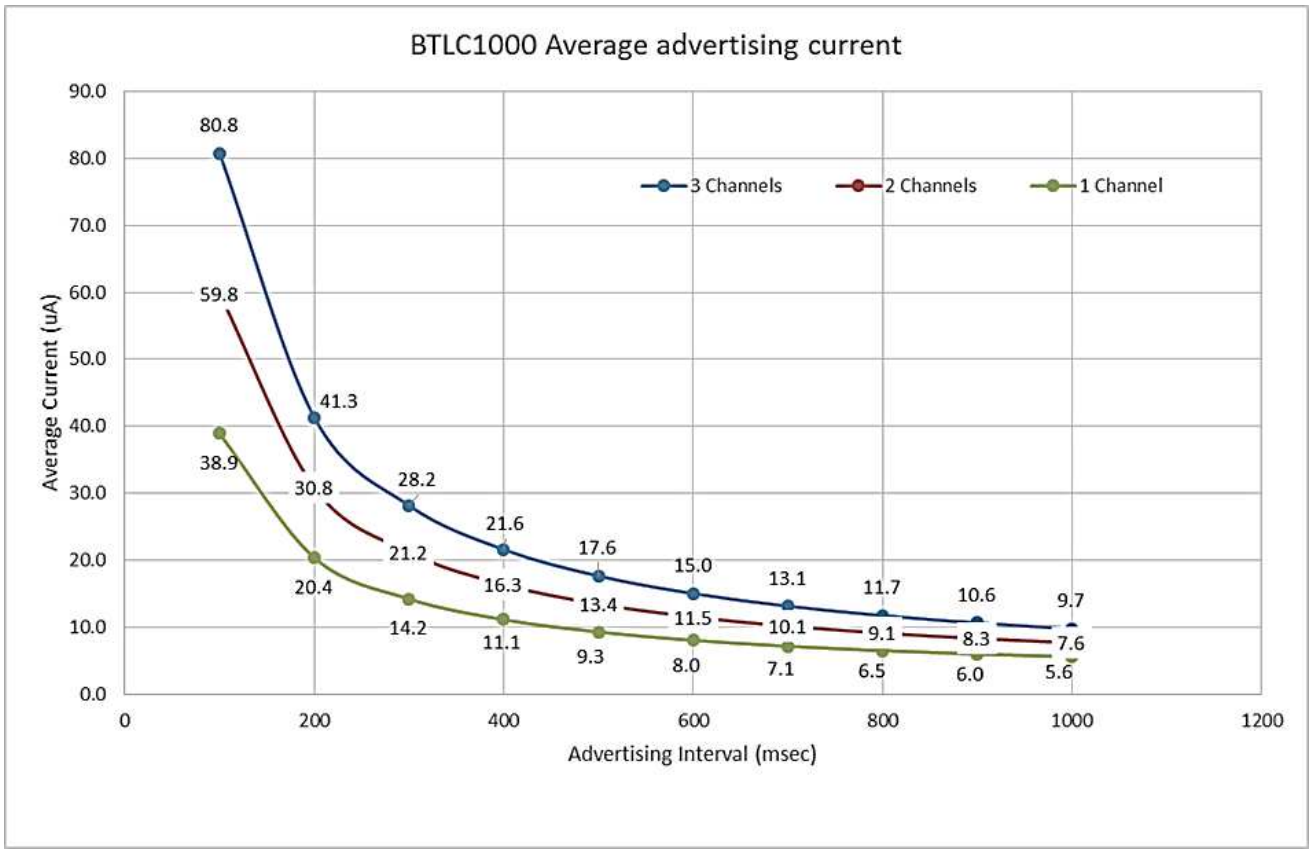
6.3.3 Current Consumption in Various Device States

Table 6-3. ATBTLC1000 Device Current Consumption at VBAT = 3.6V

Device state	CHIP_EN	VDDIO	I_{VBAT} (typical) (note 3)	I_{VDDIO} (typical) (note 3)	Remark
Power_Down	Off	On	<50nA	<50nA	
Ultra_Low_Power Standby	On	On	900nA	50nA	
Ultra_Low_Power with 8KB retention, BLE timer, no RTC (1)	On	On	1.1µA	0.2µA	
Ultra_Low_Power with 8KB retention, BLE timer, with RTC (2)	On	On	1.25µA	0.1uA	
MCU_Only, idle (waiting for interrupt)	On	On	.85mA	0.2µA	
BLE_On_Receive@-95dBm	On	On	4.2mA	0.2µA	
BLE_On_Transmit, 0dBm output power	On	On	3.0mA	0.2µA	
BLE_On_Transmit, 3.5dBm output power	On	On	4.0mA	0.2µA	

Notes:
1. Sleep clock derived from internal 32kHz RC oscillator.
2. Sleep clock derived from external 32.768kHz crystal specified for CL = 7pF, using the default on-chip capacitance only, without using external capacitance.
3. Expected values for production silicon.

Figure 6-3. ATBTLC1000 Average Advertising Current



Notes: 1. The Average advertising current is measured at VBAT = 3.6V, TX POUT=0dBm.

6.4 Power Sequences

The power sequences for ATBTLC1000 is shown in Figure 6-4. The timing parameters are provided in Table 6-4.

Figure 6-4. ATBTLC1000 Power Sequences

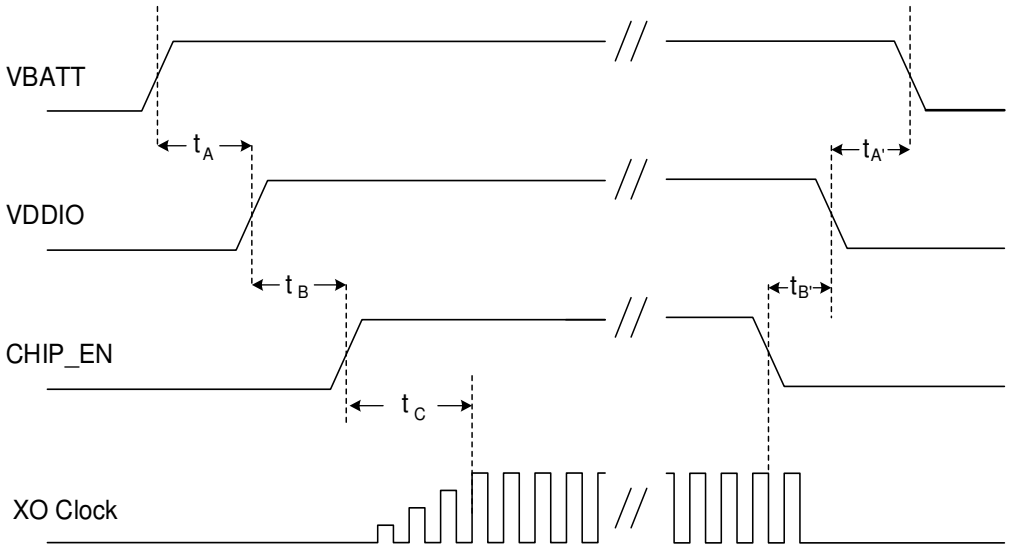


Table 6-4. ATBTLC1000 Sequence Timings

Parameter	Min.	Max.	Units	Description	Notes
t_A	0		ms	VBATT rise to VDDIO rise	VBATT and VDDIO can rise simultaneously or can be tied together
t_B	0			VDDIO rise to CHIP_EN rise	CHIP_EN must not rise before VDDIO. CHIP_EN must be driven high or low, not left floating.
t_C	10		µs	CHIP_EN rise to 31.25kHz (2MHz/64) oscillator stabilizing	
t_A[1]	0		ms	CHIP_EN fall to VDDIO fall	CHIP_EN must fall before VDDIO. CHIP_EN must be driven high or low, not left floating.
t_B[1]	0			VDDIO fall to VBATT fall	VBATT and VDDIO can fall simultaneously or be tied together

6.5 Power on Reset and Brown out Detector

The ATBTLC1000 has a Power on Reset (POR) circuit for proper system power bring up and a brown out detector to reset the system's operation when a drop in battery voltage is detected.

- POR is a power on reset circuit that outputs a HI logic value when the VBATT_BUCK is below a voltage threshold. The POR output becomes a LO logic value when the VBATT_BUCK is above a voltage threshold.
- Brown out Detector (BOD) is a brown out detector that outputs a HI logic value when the bandgap reference (BGR) voltage falls below a programmable voltage threshold. When the bandgap voltage reference voltage level is restored above a voltage threshold, the BOD output becomes a LO logic value.
- The counter creates a pulse that holds the chip in reset for 256*(64*T_2MHz) ~ 8.2ms

Figure 6-5 and Figure 6-6 illustrate the system block diagram and timing.

Figure 6-5. ATBTLC1000 POR and BOD Block Diagram

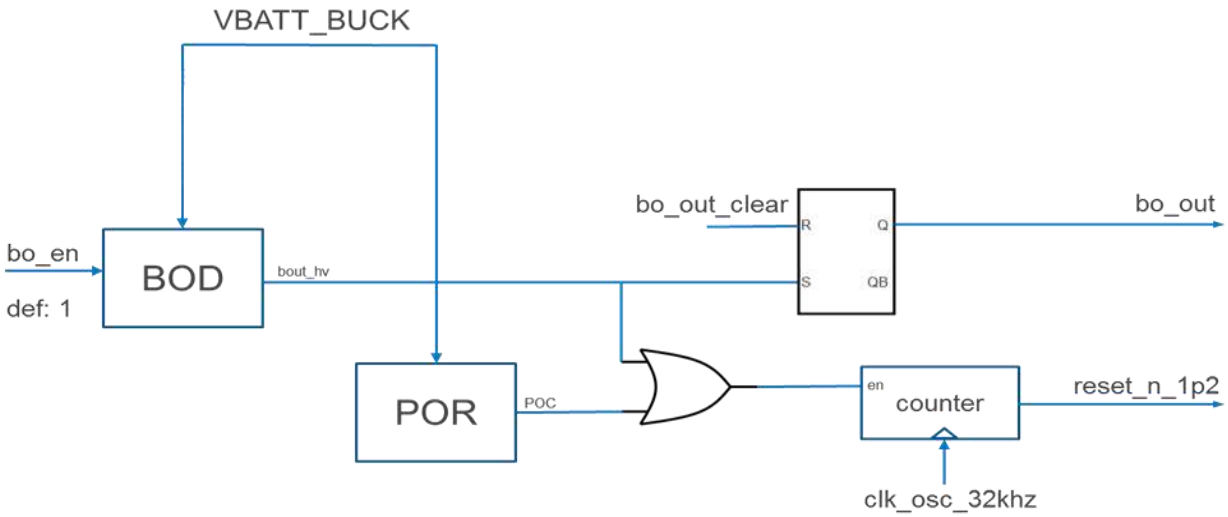


Figure 6-6. ATBTLC1000 POR and BOD Timing Sequence

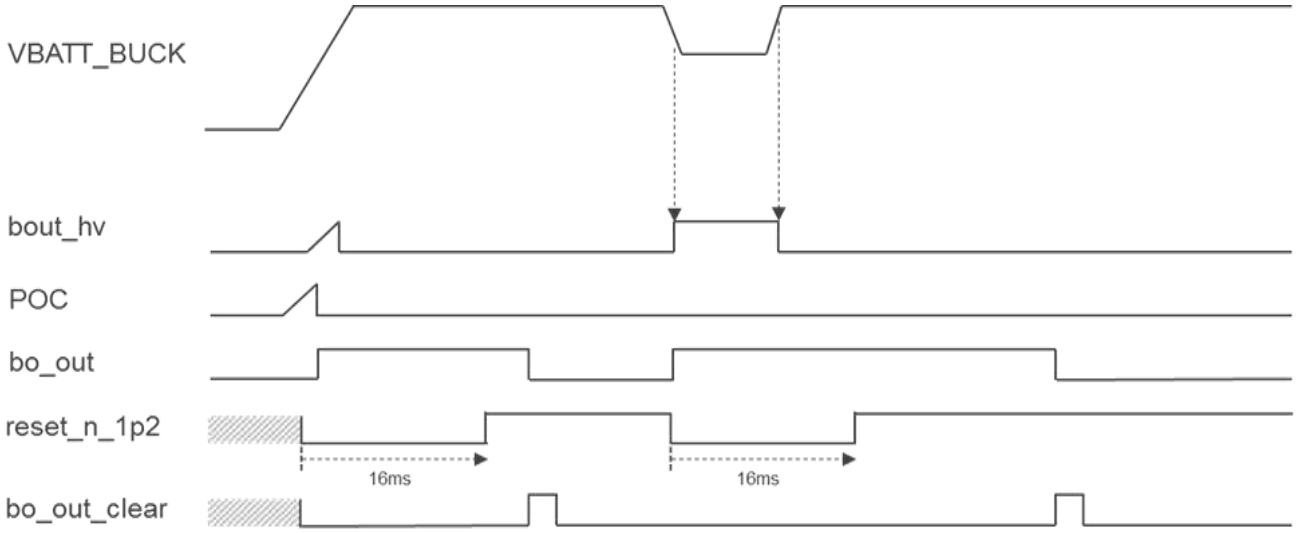


Table 6-5. ATBTLC1000 BOD Thresholds

Parameter	Min.	Typ.	Max.	Comment
BOD threshold	1.73V	1.80V	1.92V	
BOD threshold temperature coefficient		-1.09mV/C		
BOD current consumption		300nA		
t_{POR}		8.2ms		

7 Clocking

7.1 Overview

Figure 7-1. ATBTLC1000 Clock Architecture

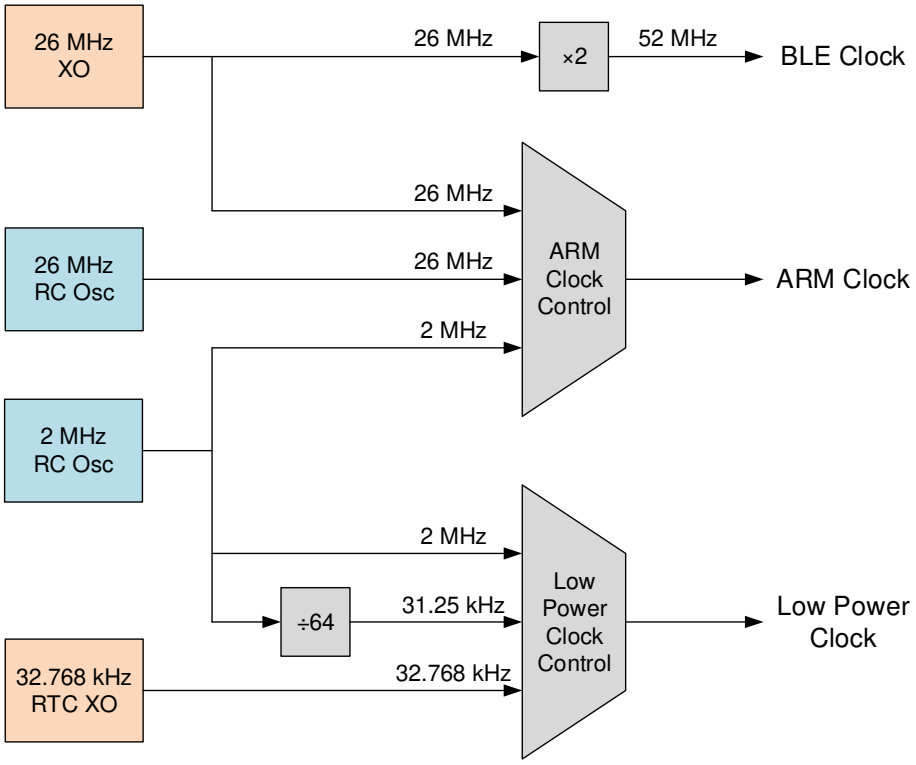


Figure 7-1 provides an overview of the clock tree and clock management blocks.

The BLE Clock is used to drive the BLE subsystem. The ARM clock is used to drive the Cortex-M0 MCU and its interfaces (UART, SPI, and I²C), the nominal MCU clock speed is 26MHz. The Low Power Clock is used to drive all the low power applications like BLE sleep timer, always-on power sequencer, always-on timer, and others.

The 26MHz Crystal Oscillator (XO) must be used for the BLE operations or in the event a very accurate clock is required for the ARM subsystem operations.

The 26MHz integrated RC Oscillator is used for most general purpose operations on the MCU and its peripherals. In cases when the BLE subsystem is not used, the RC oscillator can be used for lower power consumption. The frequency variation of this RC oscillator is up to ±50% over process, voltage, and temperature.

The 2MHz integrated RC Oscillator can be used as the Low Power Clock for applications that require fast wakeup of the ARM or for generating a ~31.25kHz clock for slower wakeup but lowest power in sleep mode. This 2MHz oscillator can also be used as the ARM Clock for low-power applications where the MCU needs to remain on but run at a reduced clock speed. The frequency variation of this RC oscillator is up to ±50% over process, voltage, and temperature.

The 32.768kHz RTC Crystal Oscillator (RTC XO) is recommended to be used for BLE operations (although optional) as it will reduce power consumption by providing the best timing for wakeup precision, allowing circuits to be in low power sleep mode for as long as possible until they need to wake up and connect during the BLE connection event. The ~31.25kHz clock derived from the 2MHz integrated RC Oscillator can be used instead of RTC XO but it has low accuracy over process, voltage and temperature variations (up to ±50%) and thus needs to be frequently calibrated to within ±500ppm if the RC oscillator is used for BLE timing during a connection event. Because this clock is less accurate than RTC XO, it will require waking up earlier to prepare for a connection event

and this will increase the average power consumption. Calibration of the RC Oscillator is described in the application note.

7.2 26MHz Crystal Oscillator (XO)

Table 7-1. ATBTLC1000 26MHz Crystal Oscillator Parameters

Parameter	Min.	Typ.	Max.	Units
Crystal Resonant Frequency	N/A	26	N/A	MHz
Crystal Equivalent Series Resistance		50	150	Ω
Stability - Initial Offset (1)	-50		50	ppm
Stability - Temperature and Aging	-40		40	

Note: 1. Initial offset must be calibrated to maintain ±25ppm in all operating conditions. This calibration is performed during final production testing and calibration offset values are stored in eFuse. More details are provided in the calibration application note.

The block diagram in Figure 7-2 (a) shows how the internal Crystal Oscillator (XO) is connected to the external crystal.

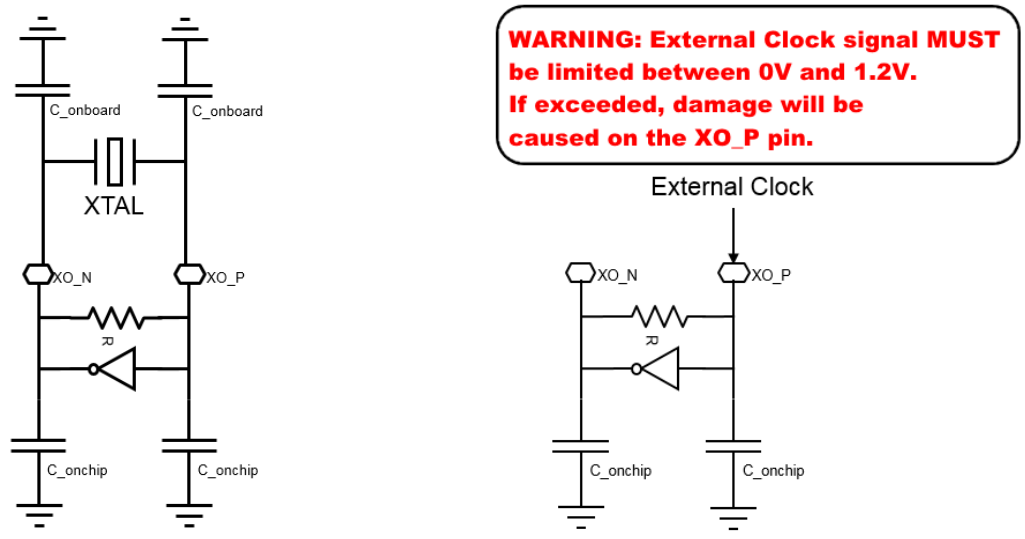
The XO has up to 10pF internal capacitance on each terminal XO_P and XO_N (programmable in steps of 1.25pF). To bypass the crystal oscillator, an external Signal capable of driving 10pF can be applied to the XO_P terminal as shown in Figure 7-2 (b).

The needed external bypass capacitors depend on the chosen crystal characteristics. Refer to the datasheet of the preferred crystal and take into account the on chip capacitance.

When bypassing XO_P from an external clock, XO_N is required to be floating.

It is recommended that only crystals specified for CL=8pF be used in customer designs since this affects the sleep/wake up timing of the device. CL other than 8pF may require upgraded firmware and device re-characterization.

Figure 7-2. ATBTLC1000 Connections to XO



(a) Crystal oscillator is used

(b) Crystal oscillator is bypassed

Table 7-2. ATBTLC1000 26MHz XTAL C_onchip Programming

Register	Cl_onchip	[pF]
rx_xo_regs[7,6,15] = 000	1.00	
rx_xo_regs[7,6,15] = 001	2.25	
rx_xo_regs[7,6,15] = 010	3.50	
rx_xo_regs[7,6,15] = 011	4.75	
rx_xo_regs[7,6,15] = 100	6.00	
rx_xo_regs[7,6,15] = 101	7.25	
rx_xo_regs[7,6,15] = 110	8.50	
rx_xo_regs[7,6,15] = 111	9.75	
If rx_reg7[1] = 1 add 5pF to above value		

Table 7-3 specifies the electrical and performance requirements for the external clock.

Table 7-3. ATBTLC1000 XO Bypass Clock Specification

Parameter	Min.	Max.	Unit	Comments
Oscillation frequency	26	26	MHz	Must be able to drive 5pF load @ desired frequency
Voltage swing	0.75	1.2	V_{pp}	
Stability – Temperature and Aging	-25	+25	ppm	
Phase Noise		-130	dBc/Hz	At 10kHz offset
Jitter (RMS)		<1psec		Based on integrated phase noise spectrum from 1kHz to 1MHz

7.3 32.768kHz RTC Crystal Oscillator (RTC XO)

7.3.1 General Information

ATBTLC1000 has a 32.768kHz RTC oscillator that is preferably used for BLE activities involving connection events. To be compliant with the BLE specifications for connection events, the frequency accuracy of this clock has to be within ±500ppm. Because of the high accuracy of the 32.768kHz crystal oscillator clock, the power consumption can be minimized by leaving radio circuits in low-power sleep mode for as long as possible until they need to wake up for the next connection timed event.

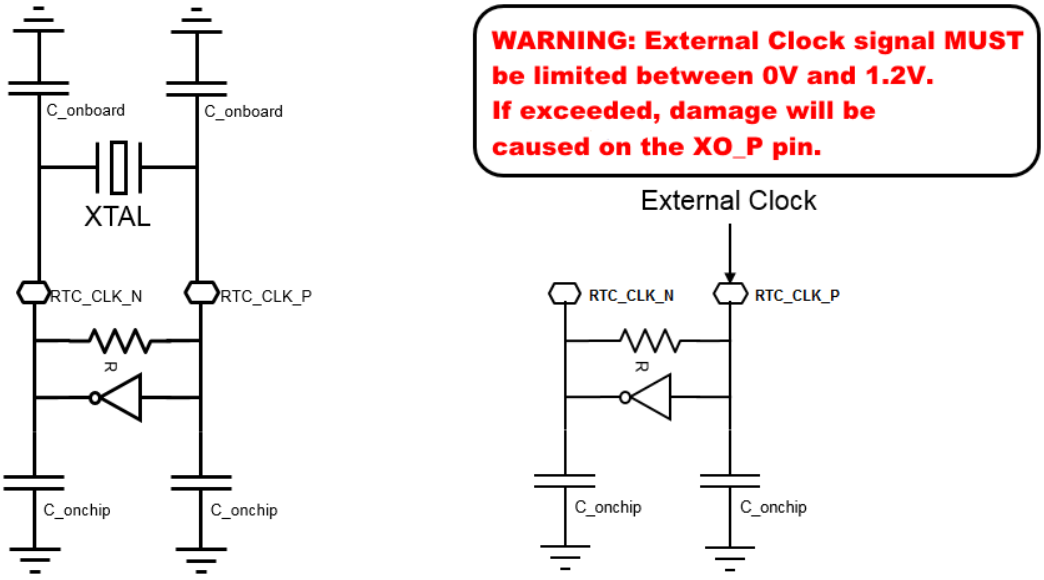
The block diagram in Figure 7-3(a) shows how the internal low frequency Crystal Oscillator (XO) is connected to the external crystal.

The RTC XO has a programmable internal capacitance with a maximum of 15pF on each terminal, RTC_CLK_P and RTC_CLK_N. When bypassing the crystal oscillator with an external signal, one can program down the internal capacitance to its minimum value (~1pF) for easier driving capability. The driving signal can be applied to the RTC_CLK_P terminal as shown in Figure 7-3 (b).

The need for external bypass capacitors depends on the chosen crystal characteristics. Refer to the datasheet of the preferred crystal and take into account the on-chip capacitance.

When bypassing RTC_CLK_P from an external clock, RTC_CLK_N is required to be floating.

Figure 7-3. ATBTLC1000 Connections to RTC XO



(a) Crystal oscillator is used

(b) Crystal oscillator is bypassed

Table 7-4. 32.768kHz XTAL C_onchip Programming

Register: pierce_cap_ctrl[3:0]	Cl_onchip	[pF]
0000	0.0	
0001	1.0	
0010	2.0	
0011	3.0	
0100	4.0	
0101	5.0	
0110	6.0	
0111	7.0	
1000	8.0	
1001	9.0	
1010	10.0	
1011	11.0	
1100	12.0	
1101	13.0	
1110	14.0	
1111	15.0	

7.3.2 RTC XO Design and Interface Specification

The RTC consists of two main blocks: The Programmable Gm stage and tuning capacitors. The programmable Gm stage is used to maintain a phase shift of 360°C with the motional arm and keep total negative resistance to sustain oscillation. Tuning capacitors are used to adjust the XO center frequency and control the XO precision for different crystal models. The output of the XO is driven to the digital domain via a digital buffer stage with supply voltage of 1.2V.

Table 7-5. RTC XO Interface

Pin name	Function	Register default
Digital Control Pins		
Pierce_res_ctrl	Control feedback resistance value: 0 = 20MΩ Feedback resistance 1 = 30MΩ Feedback resistance	0X4000F404<15>='1'
Pierce_cap_ctrl<3:0>	Control the internal tuning capacitors with step of 700fF: 0000=700fF 1111=11.2pF Refer to crystal datasheet to check for optimum tuning cap value	0X4000F404<23:20>="1000"
Pierce_gm_ctrl<3:0>	Controls the Gm stage gain for different crystal mode: 0011= for crystal with shunt cap of 1.2pF 1000= for crystal with shunt cap >3pF	0X4000F404<19:16>="1000"
Supply Pins		
VDD_XO	1.2V	

7.3.3 RTC Characterization with Gm Code Variation at Supply 1.2V and Temp. = 25°C

This section shows the RTC total drawn current and the XO accuracy versus different tuning capacitors and different GM codes, at supply voltage of 1.2V and temp. = 25°C.

Figure 7-4. RTC Drawn Current vs. Tuning Caps at 25°C

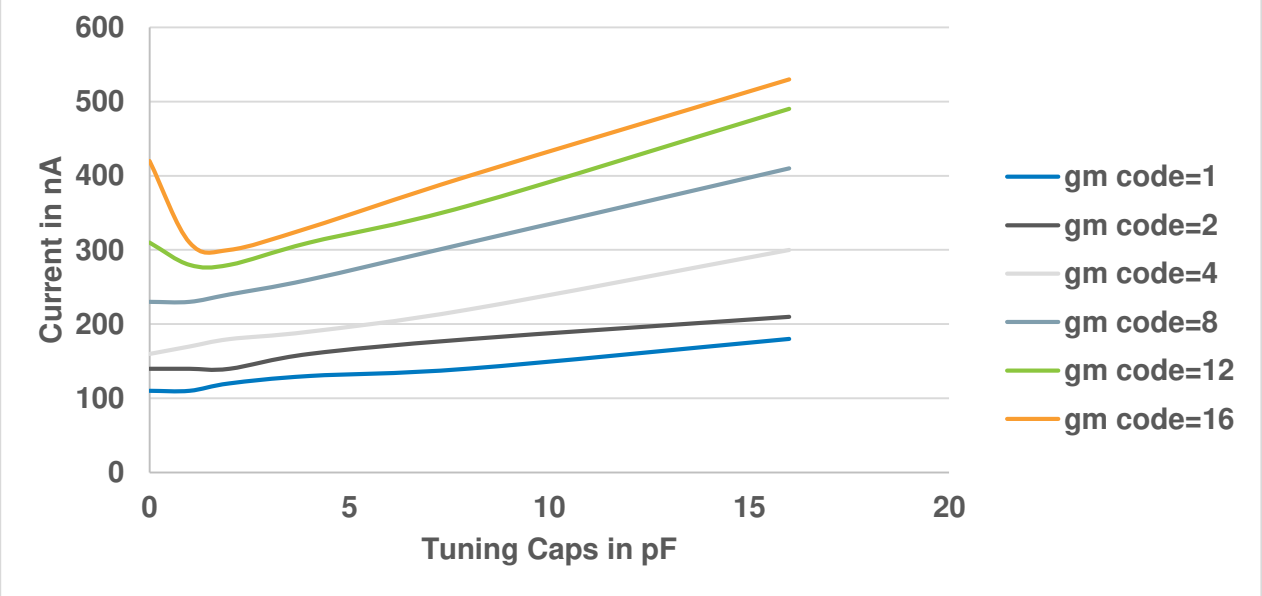
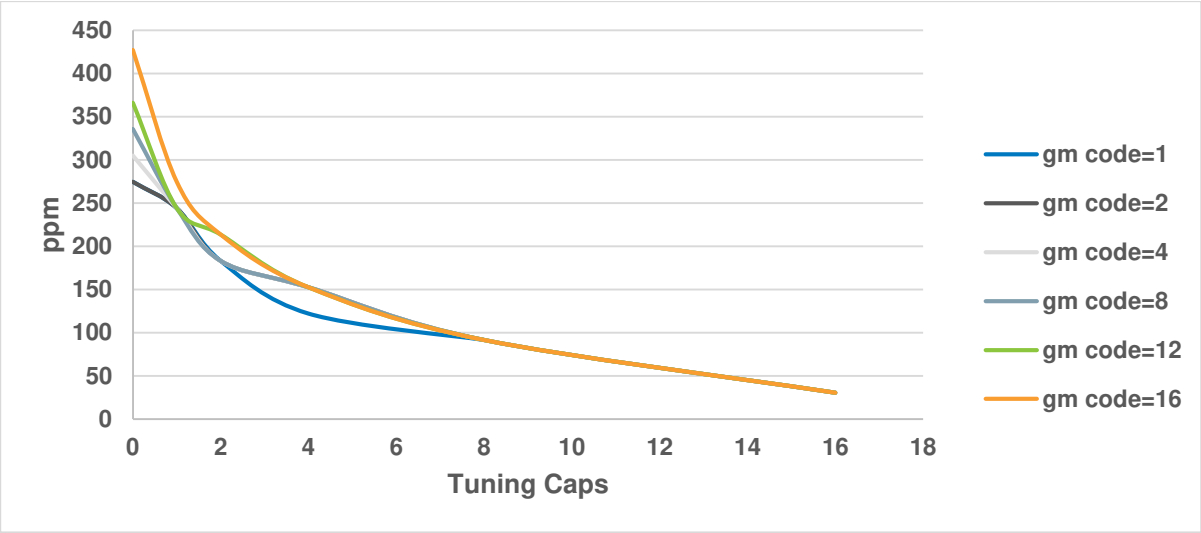


Figure 7-5. RTC Oscillation Frequency Deviation vs. Tuning Caps at 25°C



7.3.4 RTC Characterization with Supply Variation and Temp. = 25°C

Figure 7-6. RTC Drawn Current vs. Supply Variation

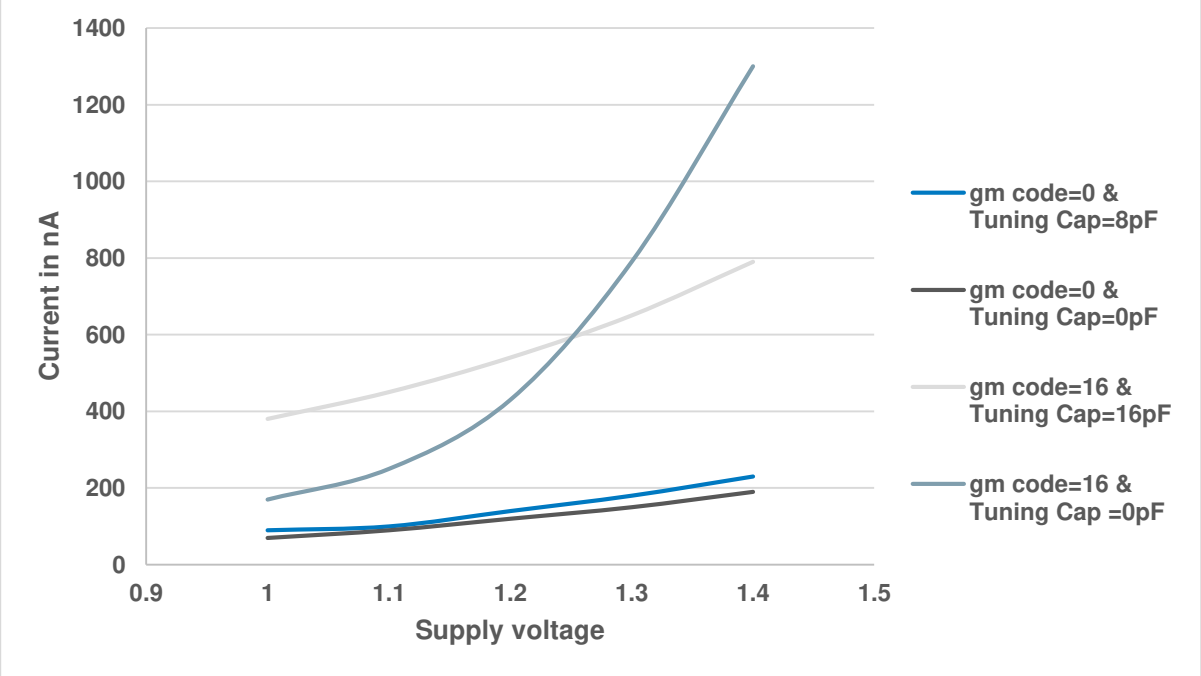
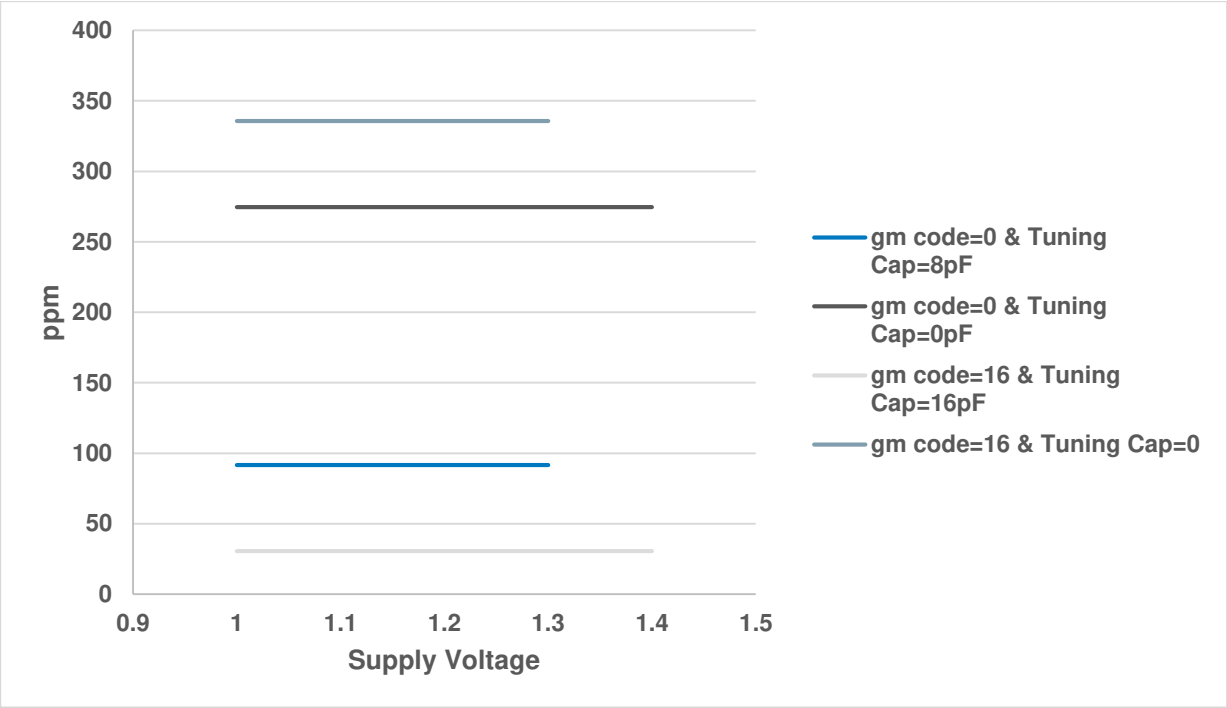


Figure 7-7. RTC Frequency Deviation vs. Supply Voltage



7.4 2MHz and 26MHz Integrated RC Oscillators

The 2MHz integrated RC Oscillator circuit without calibration has a frequency variation of 50% over process, temperature, and voltage variation. The ~31.25kHz clock is derived from the 2MHz clock by dividing by 64 and provides for lowest sleep power mode with a real-time clock running. As described above, calibration over process, temperature, and voltage are required to maintain the accuracy of this clock.

Figure 7-8. 32kHz RC Oscillator PPM Variation vs. Calibration Time at Room Temperature

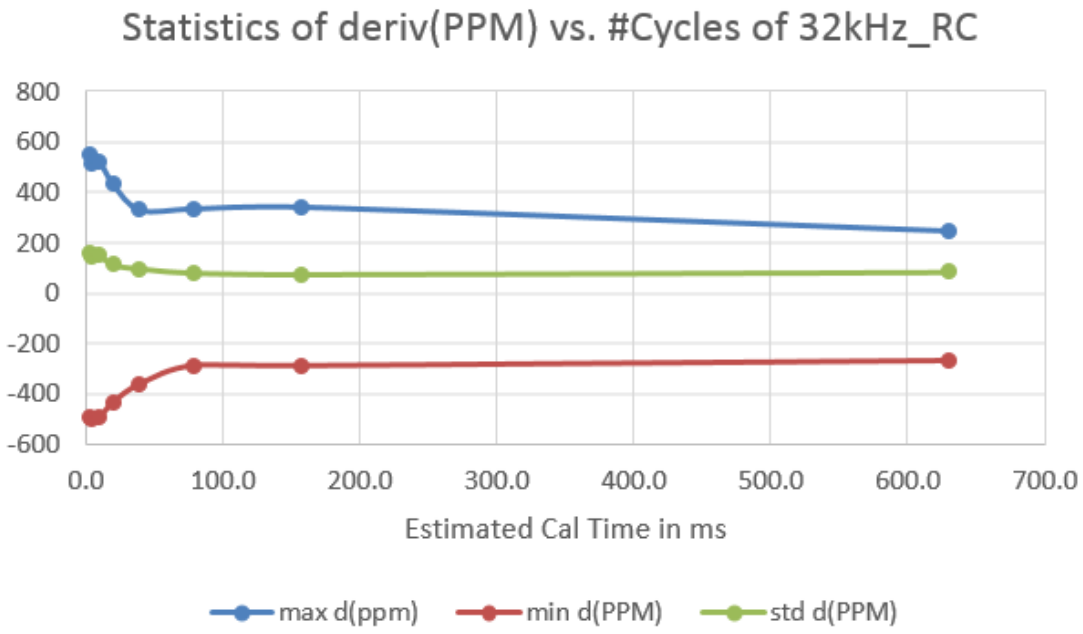
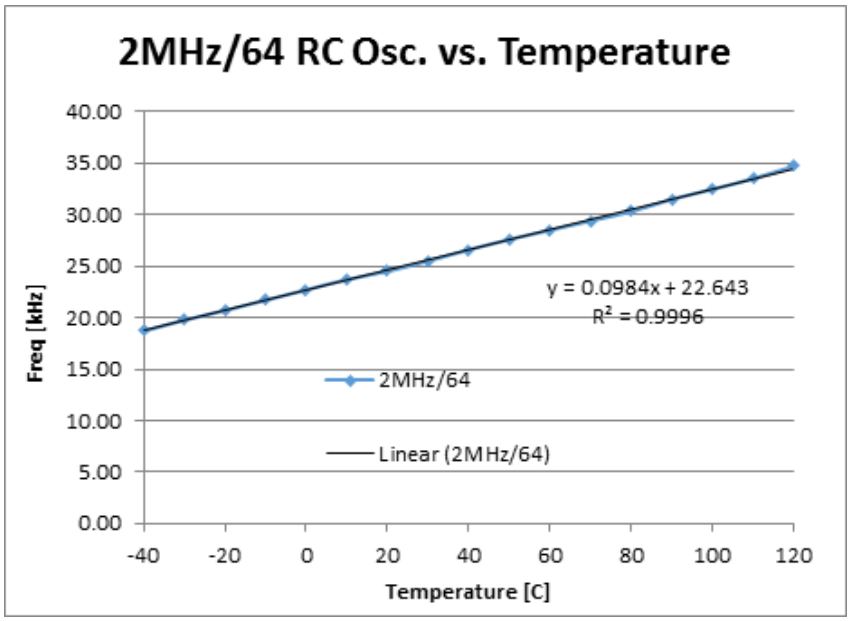


Figure 7-9. 32kHz RC Oscillator Frequency Variation over Temperature



The 26MHz integrated RC Oscillator circuit has a frequency variation of 50% over process, temperature, and voltage variation.

8 CPU and Memory Subsystem

8.1 ARM Subsystem

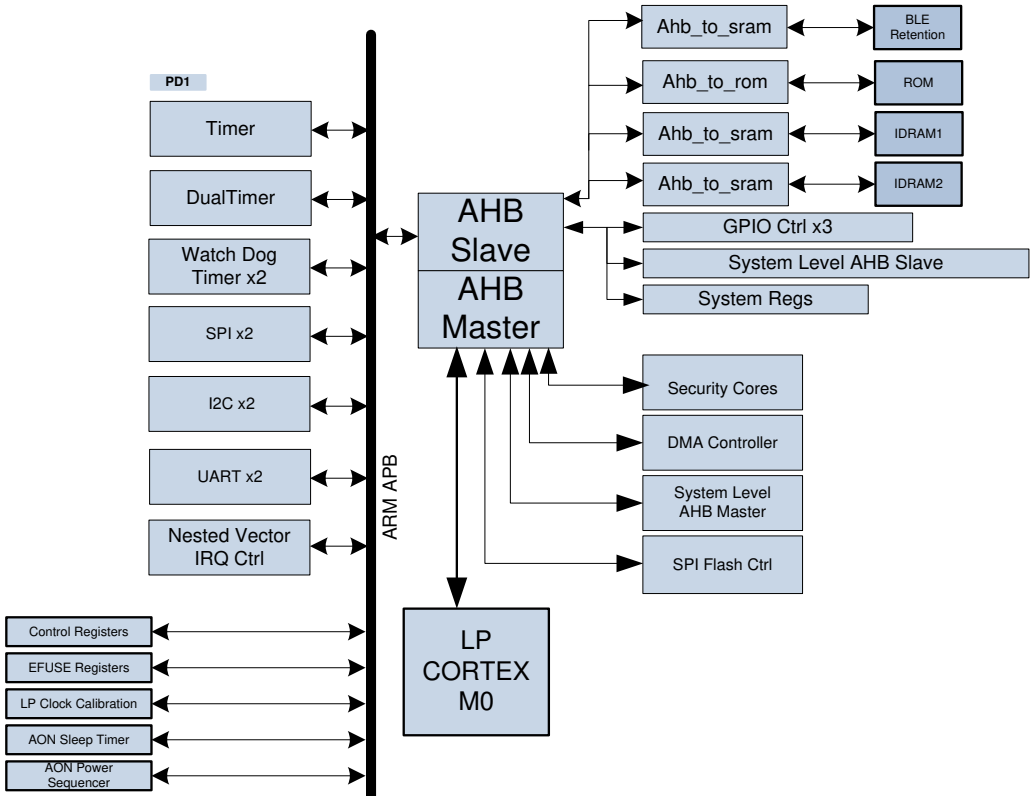
ATBTLC1000 has an ARM Cortex-M0 32-bit processor. It is responsible for controlling the BLE Subsystem and handling all application features.

The Cortex-M0 Microcontroller consists of a full 32-bit processor capable of addressing 4GB of memory. It has a RISC-like load/store instruction set and internal 3-stage Pipeline Von Neumann architecture.

The Cortex-M0 processor provides a single system-level interface using AMBA technology to provide high speed, low latency memory accesses.

The Cortex-M0 processor implements a complete hardware debug solution, with four hardware breakpoint and two watch point options. This provides high system visibility of the processor, memory, and peripherals through a 2-pin Serial Wire Debug (SWD) port that is ideal for microcontrollers and other small package devices.

Figure 8-1. ATBTLC1000 ARM Cortex-M0 Subsystem



8.1.1 Features

The processor features and benefits are:

- Tight integration with the system peripherals to reduce area and development costs
- Thumb instruction set combines high code density with 32-bit performance
- Integrated sleep modes using a Wakeup Interrupt Controller for low power consumption
- Deterministic, high-performance interrupt handling via Nested Vector Interrupt Controller for time-critical applications
- Serial Wire Debug reduces the number of pins required for debugging
- DMA engine for Peripheral-to-Memory, Memory-to-Memory, and Memory-to-Peripheral operation

8.1.2 Module Descriptions

8.1.2.1 Timer

The 32-bit timer block allows the CPU to generate a time tick at a programmed interval. This feature can be used for a wide variety of functions such as counting, interrupt generation, and time tracking.

8.1.2.2 Dual Timer

The APB dual-input timer module is an APB slave module consisting of two programmable 32-bit down-counters that can generate interrupts when they expire. The timer can be used in a Free-running, Periodic, or One-shot mode.

8.1.2.3 Watchdog

The two watchdog blocks allow the CPU to be interrupted if it has not interacted with the watchdog timer before it expires. In addition, this interrupt will be an output of the core so that it can be used to reset the CPU in the event that a direct interrupt to the CPU is not useful. This will allow the CPU to get back to a known state in the event a program is no longer executing as expected. The watchdog module applies a reset to a system in the event of a software failure, providing a way to recover from software crashes.

8.1.2.4 Wake-up Timer

This timer is a 32-bit count-down timer that operates on the 32kHz sleep clock. It can be used as a general purpose timer for the ARM or as a wakeup source for the chip. It has the ability to be a onetime programmable timer, as it will generate an interrupt/wakeup on expiration and stop operation. It also has the ability to be programmed in an auto reload fashion where it will generate an interrupt/wakeup and then proceed to start another count down sequence.

8.1.2.5 SPI Controller

See Section 10.3.

8.1.2.6 I^2C Controller

See Section 10.2.

8.1.2.7 SPI-Flash Controller

The AHB SPI-Flash Controller is used to access an external SPI Flash device to access various instruction/data code needed for storing application code, code patches, and OTA images. Supports several SPI modes including 0, 1, 2, and 3. See Section 10.4.

8.1.2.8 UART

See Section 10.5.

8.1.2.9 DMA Controller

Direct Memory Access (DMA) allows certain hardware subsystems to access main system memory independently of the Cortex-M0 Processor.

The DMA features and benefits are:

- Supports any address alignment
- Supports any buffer size alignment
- Peripheral flow control, including peripheral block transfer
- The following modes are supported:
  - Peripheral to peripheral transfer
  - Memory to memory
  - Memory to peripheral
  - Peripheral to memory