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# Atmel M90E32AS

## Enhanced Poly-Phase High-Performance Wide-Span Energy Metering IC

**DATASHEET**

# FEATURES

## Metering Features

- Metering features fully in compliance with the requirements of IEC62052-11, IEC62053-22 and IEC62053-23, ANSI C12.1 and ANSI C12.20; applicable in poly-phase class 0.2S, 0.5S or class 1 watt-hour meter or class 2 var-hour meter.
- Accuracy of ±0.1% for active energy and ±0.2% for reactive energy over a dynamic range of 6000:1.
- Temperature coefficient is 6 ppm/ ℃ (typ.) for on-chip reference voltage. Automatically temperature compensated.
- Single-point calibration on each phase over the whole dynamic range for active energy; no calibration needed for reactive/ apparent energy.
- ±1 ℃ (typ.) temperature sensor accuracy.
- Flexible piece-wise non-linearity compensation: three current (RMS value)-based segments with two programmable thresholds for each phase. Independent gain and phase angle compensation for each segment.
- Electrical parameters measurement: less than ±0.5% fiducial error for Vrms, Irms, mean active/ reactive/ apparent power, frequency, power factor and phase angle.
- Active (forward/reverse), reactive (forward/reverse), apparent energy with independent energy registers.
- Programmable startup and no-load power thresholds.
- 6 dedicated ADCs for phase A/B/C current and voltage sampling circuits. Current sampled over Current Transformer (CT) or Rogowski coil (di/dt coil); voltage sampled over resistor divider network.
- Programmable power modes: Normal, Idle, Detection and Partial Measurement mode.
- Fundamental (0.2%) and harmonic (1%) active energy with dedicated energy / power registers and independent energy outputs.
- Current and voltage instantaneous signal monitoring.
- Enhanced event detection: sag, over voltage, phase loss, over current, reverse V/I phase sequence, calculated neutral line current $I_{NC}$ over-current and frequency upper and lower threshold.

## Other Features

- 3.3V single power supply. Operating voltage range: 2.8V~3.6V. Metering accuracy guaranteed within 3.0V~3.6V.
- Four-wire SPI interface.
- Programmable voltage sag detection and zero-crossing output.
- Crystal oscillator frequency: 16.384MHz. On-chip two capacitors and no need of external capacitors.
- Lower power consumption. I=13mA (typ.) in Normal mode.
- TQFP48 package.
- Operating temperature: -40 ℃ ~ +85 ℃ .

## APPLICATION

- Poly-phase energy meters of class 0.2S, 0.5S and class 1 which are used in three-phase four-wire (3P4W, Y0) or three-phase three-wire (3P3W, Y or Δ) systems.
- Power monitoring instruments which need to measure voltage, current, mean power, etc.

## GENERAL DESCRIPTION

The M90E32AS is a poly-phase high performance wide-dynamic range metering IC. The M90E32AS incorporates 6 independent 2nd order sigma-delta ADCs, which could be employed in three voltage channels (phase A, B and C) and three current channels (phase A, B, C) in a typical three-phase four-wire system.
The M90E32AS has an embedded DSP which executes calculation of active energy, reactive energy, apparent energy, fundamental and harmonic active energy over ADC signal and on-chip reference voltage. The DSP also calculates measurement parameters such as voltage and current RMS value as well as mean active/reactive/apparent power.
A four-wire SPI interface is provided between the M90E32AS and the external microcontroller.
The M90E32AS is suitable for poly-phase multi-function meters which could measure active/reactive/apparent energy and fundamental/harmonic energy either through four independent energy pulse outputs CF1/CF2/CF3/CF4 or through the corresponding registers.
The ADC and auto-temperature compensation technology for reference voltage ensure the M90E32AS's long-term stability over variations in grid and ambient environment conditions.

## BLOCK DIAGRAM

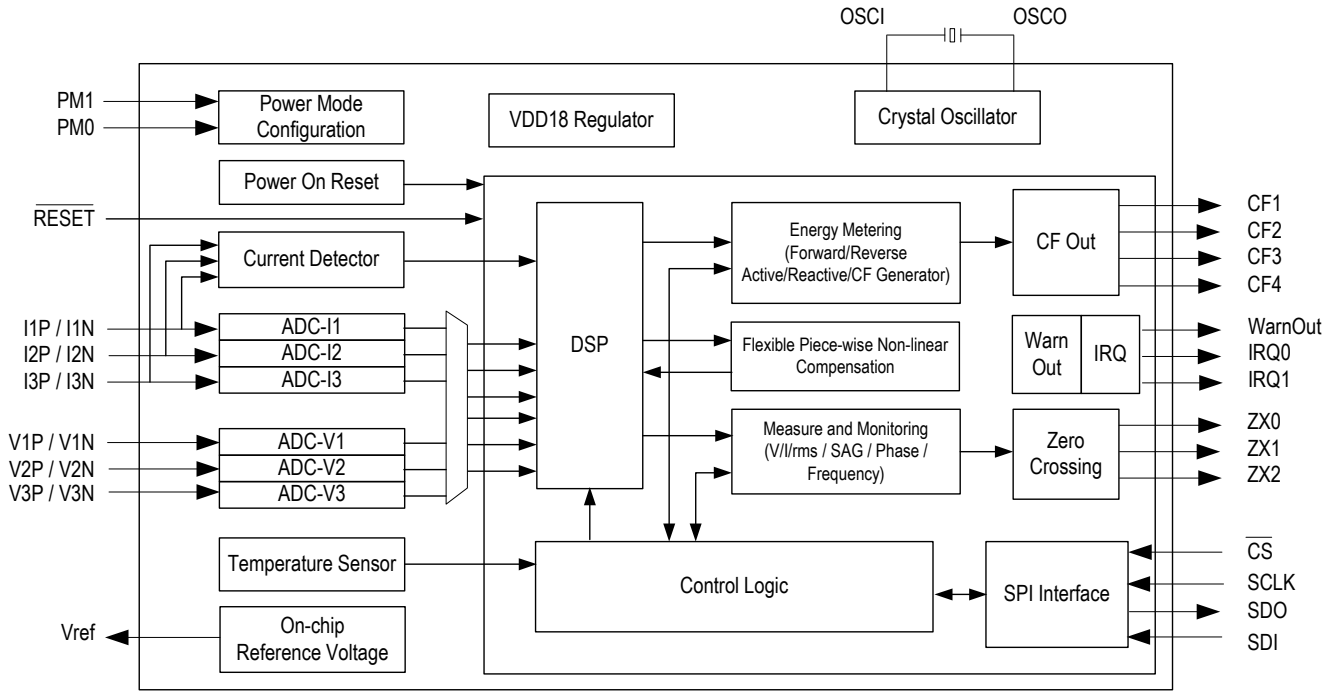


***Figure-1 M90E32AS Block Diagram***

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# 1 PIN ASSIGNMENT

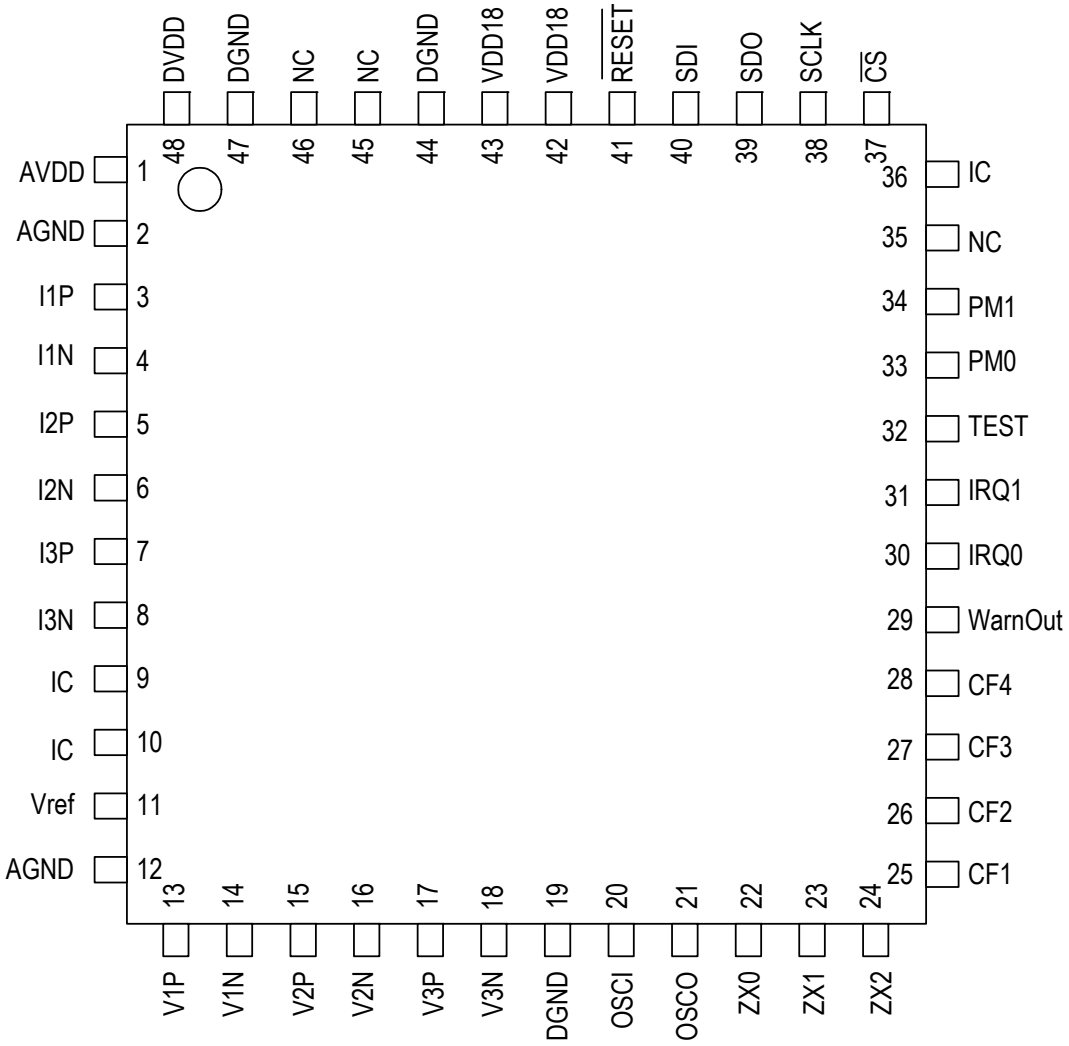


***Figure-2 Pin Assignment (Top View)***

# 2 PIN DESCRIPTION

**Table-1 Pin Description**

| Name | Pin No. | I/O | Type | Description |
|---|---|---|---|---|
| $\overline{\text{Reset}}$ | 41 | I | LVTTL | **$\overline{\text{Reset}}$: Reset Pin (active low)**<br>This pin should connect to ground through a 0.1 μF filter capacitor and a 10kΩ resistor to VDD. In application it can also directly connect to one output pin from microcontroller (MCU). |
| AVDD | 1 | I | Power | **AVDD: Analog Power Supply**<br>This pin provides power supply to the analog part. This pin should connect to DVDD and be decoupled with a 0.1μF capacitor. |
| DVDD | 48 | I | Power | **DVDD: Digital Power Supply**<br>This pin provides power supply to the digital part. It should be decoupled with a 10μF capacitor and a 0.1μF capacitor. |
| VDD18 | 42, 43 | P | Power | **VDD18: Digital Power Supply (1.8 V)**<br>These two pins should be connected together and connected to ground through a 10μF capacitor. |
| DGND | 19, 44, 47 | I | Power | **DGND: Digital Ground** |
| AGND | 2, 12 | I | Power | **AGND: Analog Ground** |
| I1P<br>I1N | 3<br>4 | I | Analog | **I1P: Positive Input for Analog ADC Channel**<br>**I1N: Negative Input for Analog ADC Channel**<br>These pins are differential inputs for analog ADC channel.<br>These 6 analog ADC channels can be flexibly mapped, refer to 3.4 Analog/digital Channel Mapping.[1] |
| I2P<br>I2N | 5<br>6 | I | Analog | **I2P: Positive Input for Analog ADC Channel**<br>**I2N: Negative Input for Analog ADC Channel**<br>These pins are differential inputs for analog ADC channel.<br>These 6 analog ADC channels can be flexibly mapped, refer to 3.4 Analog/digital Channel Mapping.[1] |
| I3P<br>I3N | 7<br>8 | I | Analog | **I3P: Positive Input for Analog ADC Channel**<br>**I3N: Negative Input for Analog ADC Channel**<br>These pins are differential inputs for analog ADC channel.<br>These 6 analog ADC channels can be flexibly mapped, refer to 3.4 Analog/digital Channel Mapping.[1] |
| Vref | 11 | O | Analog | **Vref: Output Pin for Reference Voltage**<br>This pin should be decoupled with a 4.7μF capacitor, it is better to add a 0.1μF ceramic capacitor. |
| V1P<br>V1N | 13<br>14 | I | Analog | **V1P: Positive Input for Analog ADC Channel**<br>**V1N: Negative Input for Analog ADC Channel**<br>These pins are differential inputs for analog ADC channel.<br>These 6 analog ADC channels can be flexibly mapped, refer to 3.4 Analog/digital Channel Mapping.[1] |
| V2P<br>V2N | 15<br>16 | I | Analog | **V2P: Positive Input for Analog ADC Channel**<br>**V2N: Negative Input for Analog ADC Channel**<br>These pins are differential inputs for analog ADC channel.<br>These 6 analog ADC channels can be flexibly mapped, refer to 3.4 Analog/digital Channel Mapping.[1] |
| V3P<br>V3N | 17<br>18 | I | Analog | **V3P: Positive Input for Analog ADC Channel**<br>**V3N: Negative Input for Analog ADC Channel**<br>These pins are differential inputs for analog ADC channel.<br>These 6 analog ADC channels can be flexibly mapped, refer to 3.4 Analog/digital Channel Mapping.[1] |

**Table-1 Pin Description (Continued)**

| Name | Pin No. | I/O | Type | Description |
|---|---|---|---|---|
| OSCI | 20 | I | OSC | **OSCI: External Crystal Input**<br>**OSCO: External Crystal Output**<br>A 16.384 MHz crystal is connected between OSCI and OSCO. There are two on-chip capacitors, therefore no need of external capacitors. |
| OSCO | 21 | O | OSC | |
| ZX0<br>ZX1<br>ZX2 | 22<br>23<br>24 | O | LVTTL | **ZX2/ZX1/ZX0:Zero-Crossing Output**<br>These pins are asserted when voltage or current crosses zero. Zero-crossing mode can be configured by the ZXConfig register (07H). |
| CF1 | 25 | O | LVTTL | **CF1: (all-phase-sum total) Active Energy Pulse Output** |
| CF2 | 26 | O | LVTTL | **CF2: (all-phase-sum total) Reactive/ Apparent Energy Pulse Output**<br>The output of this pin is determined by the CF2varh bit (b7, MMode0). |
| CF3 | 27 | O | LVTTL | **CF3: (all-phase-sum total) Active Fundamental Energy Pulse Output** |
| CF4 | 28 | O | LVTTL | **CF4: (all-phase-sum total) Active Harmonic Energy Pulse Output** |
| WarnOut | 29 | O | LVTTL | **WarnOut: Fatal Error Warning**<br>This pin is asserted high when there is metering related parameter checksum error. Otherwise this pin stays low. Refer to 5.2.2 IRQ and WarnOut Signal Generation. |
| IRQ0 | 30 | O | LVTTL | **IRQ0: Interrupt Output 0**<br>This pin is asserted when one or more events in the EMMIntState0 register (1CCH) occur. It is deasserted when there is no bit set in the EMMIntState0 register (1CCH).<br>In Detection mode, the IRQ0 is used to indicate the output of current detector. The IRQ0 state is cleared when entering or exiting Detection mode. |
| IRQ1 | 31 | O | LVTTL | **IRQ1: Interrupt Output 1**<br>This pin is asserted when one or more events in the EMMIntState1 register (1D0H) occur. It is deasserted when there is no bit set in the EMMIntState1 register (1D0H).<br>In Detection mode, the IRQ1 is used to indicate the output of current detector. The IRQ1 state is cleared when entering or exiting Detection mode. |
| PM0<br>PM1 | 33<br>34 | $I^2$ | LVTTL | **PM1/0: Power Mode Configuration**<br>These two pins define the power mode of M90E32AS. Refer to Table-2. |
| $\overline{CS}$ | 37 | $I^2$ | LVTTL | **$\overline{CS}$: Chip Select (Active Low)**<br>In SPI mode, this pin must be driven from high to low for each read/ write operation, and maintain low for the entire operation. |
| SCLK | 38 | $I^2$ | LVTTL | **SCLK: Serial Clock**<br>This pin is used as the clock for the SPI interface. Refer to 4 SPI Interface. |
| SDO | 39 | O | LVTTL | **SDO: Serial Data Output**<br>This pin is used as the data output for the SPI mode. Refer to 4 SPI Interface. |
| SDI | 40 | $I^2$ | LVTTL | **SDI: Serial Data Input**<br>This pin is used as the data input for the SPI mode. Refer to 4 SPI Interface. |
| TEST | 32 | I | LVTTL | This pin should be always connected to DGND in system application. |
| IC | 9, 10, 36 | | LVTTL | These pins should be always connected to DGND in system application. |
| NC | 35, 45, 46 | | | **NC: These pins should be left open.** |

Note 1: The channel mapping is only valid in Normal mode and Patial Measurement mode.
Note 2: All the digital input pins except OSCI are 5 V compatible.

# 3 FUNCTION DESCRIPTION

## 3.1 POWER SUPPLY

The M90E32AS works with single power rail 3.3V. An on-chip voltage regulator regulates the 1.8V voltage for the digital logic.

The regulated 1.8V power is connected to the VDD18 pin. It needs to be bypassed by an external capacitor.

The M90E32AS has four power modes: Normal (N mode), Partial Measurement (M mode), Detection (D mode) and Idle (I mode). In Idle and Detection modes the 1.8V power regulator is not turned on and the digital logic is not powered. When the logic is not powered, all the configured register values are not kept (all context lost) except for Detection mode related registers (10H~13H) for Detection mode configuration.

The registers in Partial Measurement mode or Normal mode have to be re-configured when transiting from Idle or Detection mode. Refer to 3.8 Power Mode for power mode details.

## 3.2 CLOCK

The M90E32AS has an on-chip oscillator and can directly connect to an external crystal.

The OSCI pin can also be driven with a clock source.

The oscillator will be powered down in Idle and Detection power modes, as described in 3.8 Power Mode.

## 3.3 RESET

There are three reset sources for the M90E32AS:

- $\overline{\text{RESET}}$ pin
- On-chip Power On Reset circuit
- Software Reset generated by the SoftReset register

### 3.3.1 $\overline{\text{RESET}}$ PIN

The $\overline{\text{RESET}}$ pin can be asserted to reset the M90E32AS. The $\overline{\text{RESET}}$ pin has RC filter with typical time constant of 2μs in the I/O, as well as a 2μs (typical) de-glitch filter.

Any reset pulse that is shorter than 2μs can not reset the M90E32AS.

### 3.3.2 POWER ON RESET (POR)

The POR circuit resets the M90E32AS at power up.

POR circuit triggers reset when:

- DVDD power up with crossing the power-up threshold. Refer to Figure-24.
- VDD18 regulator changing from disable to enable, i.e. from Idle or Detection mode to Partial Measurement mode or Normal mode. Refer to Figure-23.

### 3.3.3 SOFTWARE RESET

Chip reset can be triggered by writing to the SoftReset register in Normal mode. The software reset is the same as the reset scope generated from the $\overline{\text{RESET}}$ pin or POR.

These three reset sources have the same reset scope.

All digital logics and registers except for some special registers will be subjected to reset.

- Interface logic: clock dividers
- Digital core/ logic: All registers except for some special registers. Refer to 5.3.1 Detection Mode Registers.

## 3.4 ANALOG/DIGITAL CHANNEL MAPPING

Analog channel to digital channel mapping:

The 6 analog ADC channels can be flexibly mapped to the 6 digital metering/measuring channels (V/I phase A/B/C). Refer to the ChannelMapI and ChannelMapU registers for configuration.

Note that channel mapping is only valid in Normal mode and Patial Measurement mode.

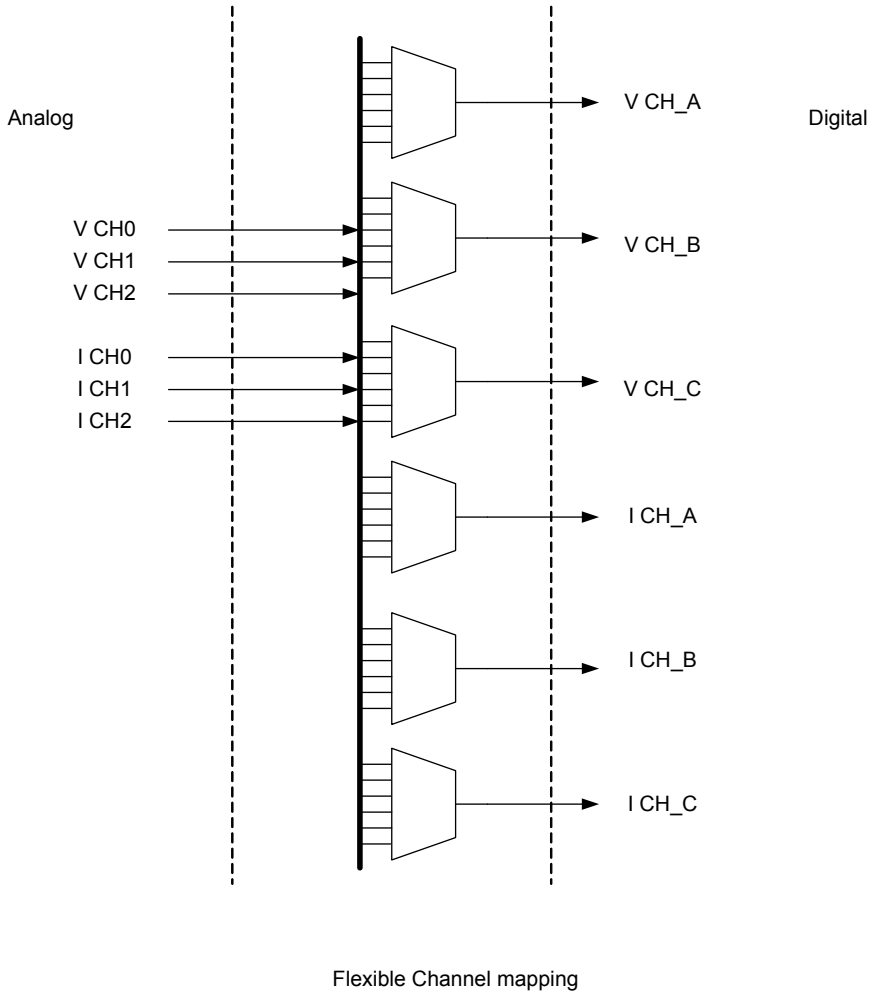


***Figure-3 Channel to Phase Mapping***

## 3.5 METERING FUNCTION

Metering is enabled when any of the MeterEn bits are set.

When metering is not enabled, the CF pulse will not be generated and energy accumulator will not accumulate energy. All energy accumulation related status will be cleared, while startup/noload handling block related status will be still working.

The accumulated energy will be converted to pulse frequency on the CF pins and stored in the corresponding energy registers.

### 3.5.1 THEORY OF ENERGY REGISTERS

The energy accumulation runs at 1 MHz clock rate by accumulating the power value calculated by the DSP processor.

The power accumulation process is equivalent to digitally integrating the instantaneous power with a delta-time of about 1us. The accumulated energy is used to calculate the CF pulses and the corresponding internal energy registers.

The accumulated energy is converted to frequency of the CF pulses. One CF usually corresponds to 1KWh / MC (MC is Meter Constant, e.g. 3200 imp/kWh), and is usually referenced as an energy unit in this datasheet. The internal energy resolution for accumulation and conversion is 0.01 CF.

The 0.01 CF pulse energy constant is referenced as 'PL_constant'.

Within 0.01 CF, forward and reverse energy are counteracted. When energy exceeds 0.01 pulse, the respective forward/reverse energy is increased.

Take the example of active energy. Suppose:

T0: Forward energy register is 12.34 pulses and reverse energy register is 1.23 pulses.

From t0 to t1: 0.005 forward pulses appeared.

From t1 to t2: 0.004 reverse pulses appeared.

From t2 to t3: 0.005 reverse pulses appeared.

From t3 to t4: 0.007 reverse pulses appeared.

The following table illustrates the process of energy accumulation process:

| | t0 | t1 | t2 | t3 | t4 |
|---|---|---|---|---|---|
| **Input energy** | + 0.005 | -0.004 | -0.005 | -0.007 | |
| **Bidirectional energy accumulator** | 0.005 | 0.001 | -0.004 | -0.001 | |
| **Forward 0.01 CF** | 0 | 0 | 0 | 0 | |
| **Reverse 0.01CF** | 0 | 0 | 0 | 1 | |
| **Forward energy register** | 12.34 | 12.34 | 12.34 | 12.34 | 12.34 |
| **Reverse energy register** | 1.23 | 1.23 | 1.23 | 1.23 | 1.24 |

When forward/reverse energy reaches 0.01 pulse, the respective register is updated. When forward or reverse energy reaches 1 pulse, CFx pins output pulse and the CFxRevST bits (b3~0, EMMState0) are updated. Refer to Figure-4.

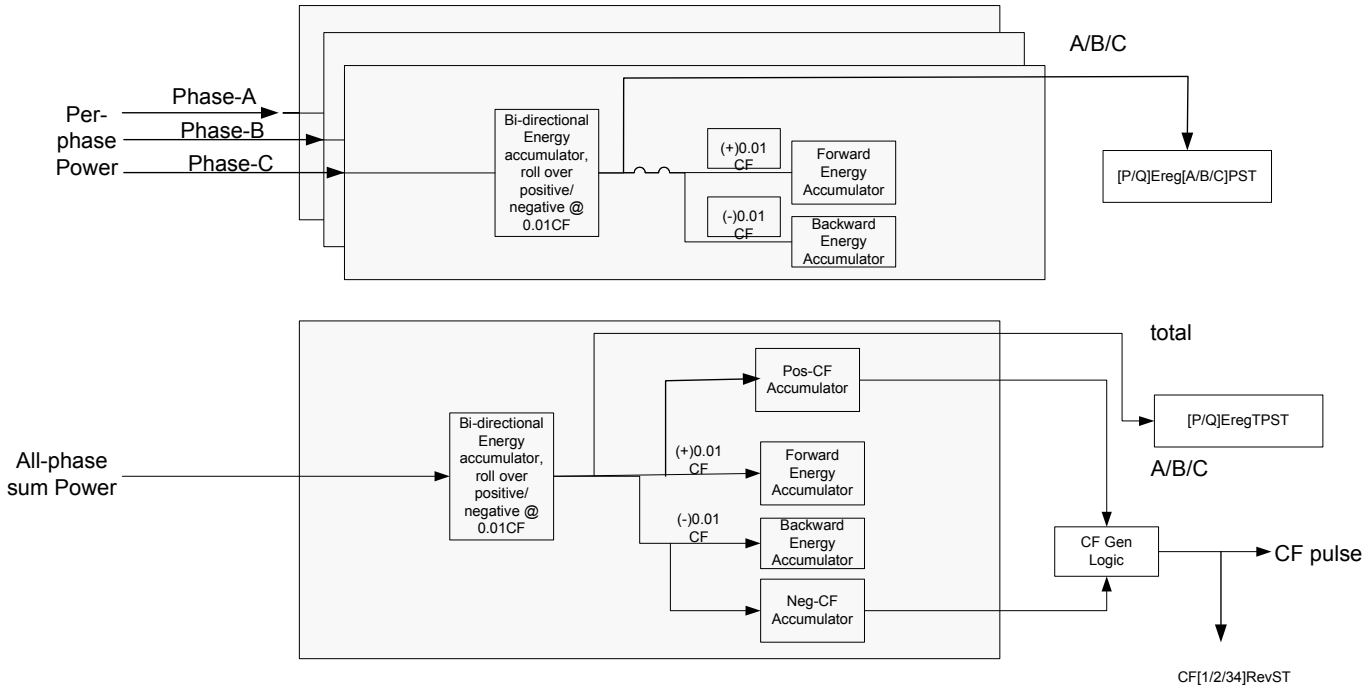


***Figure-4 Energy Accumulation Diagram***

For all-phase-sum total of active, reactive and (arithmetic sum) apparent energy, the associated power is obtained by summing the power of the three phases. The accumulation method of all-phase-sum energy is determined by the EnPC/EnPB/EnPA/ABSEnP/ABSEnQ bits (b0~b4, MMode0).

Note that the direction of all-phase-sum power and single-phase power might be different.

### 3.5.2 ENERGY REGISTERS

The M90E32AS meters non-decomposed total active, reactive and apparent energy, as well as decomposed active fundamental and harmonic energy. The registers are listed as below.

#### 3.5.2.1 Total Energy Registers

Each phase and all-phase-sum has the following registers:

- Active forward/ reverse
- Reactive forward/ reverse
- Apparent energy

Altogether there are 20 energy registers. Those registers are defined in 5.5.1 Regular Energy Registers.

#### 3.5.2.2 Fundamental and Harmonic Energy Registers

The M90E32AS counts decomposed active fundamental and harmonic energy. Reactive energy is not decomposed to fundamental and harmonic.

The fundamental/harmonic energy is accumulated in the same way as active energy accumulation method described above.

Registers:

- Fundamental / harmonic
- all-phase-sum / phase A / phase B / phase C
- Forward / reverse

Altogether there are 16 energy registers. Refer to 5.5.2 Fundamental / Harmonic Energy Register.

### 3.5.3 ENERGY PULSE OUTPUT

CF1 is fixed to be total active energy output (all-phase-sum). Both forward and reverse energy registers can generate the CF pulse (change of forward/ reverse direction can generate an interrupt if enabled).

CF2 is reactive energy output (all-phase-sum) by default. It can also be configured to be arithmetic sum apparent energy output (all-phase-sum).

CF3 is fixed to be active fundamental energy output (all-phase-sum).

CF4 is fixed to be active harmonic energy output (all-phase-sum).

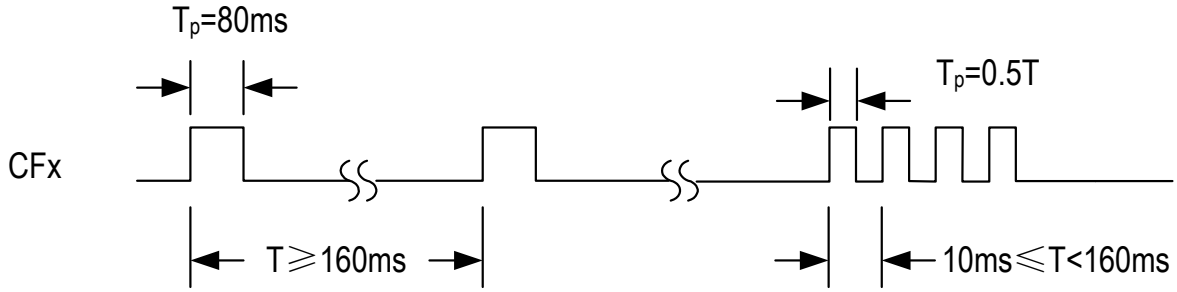


***Figure-5 CFx Pulse Output Regulation***

For CFx pulse width regulation, refer to Figure-5.

Case1 T>=160ms, Tp=80ms

Case 2 10ms<=T<160ms, Tp=T/2

### 3.5.4 STARTUP AND NO-LOAD POWER

There are startup power threshold registers (e.g. PStartTh(35H)). Refer to 5.4 Configuration and Calibration Registers. The power threshold registers are defined for all-phase-sum active, reactive and apparent power. The M90E32AS starts metering when the corresponding all-phase-sum power is greater than the startup threshold. When the power value is lower than the startup threshold, energy is not accumulated and it is assumed as in no-load status. Refer to Figure-6.

There are also no-load Current Threshold registers for Active, Reactive and Apparent energy metering participation for each of the 3 phases. If |P|+|Q| is lower than the corresponding power threshold, that particular phase will not be accumulated. Refer to the PStartTh register and other threshold registers.

There are also no-load status bits (the TPnoload/TQnoload bits (b14~15, Fundamental / Harmonic Energy Register)) defined to reflect the no-load status. The M90E32AS does not output any pulse in no-load status. The power-on state is of no-load status.

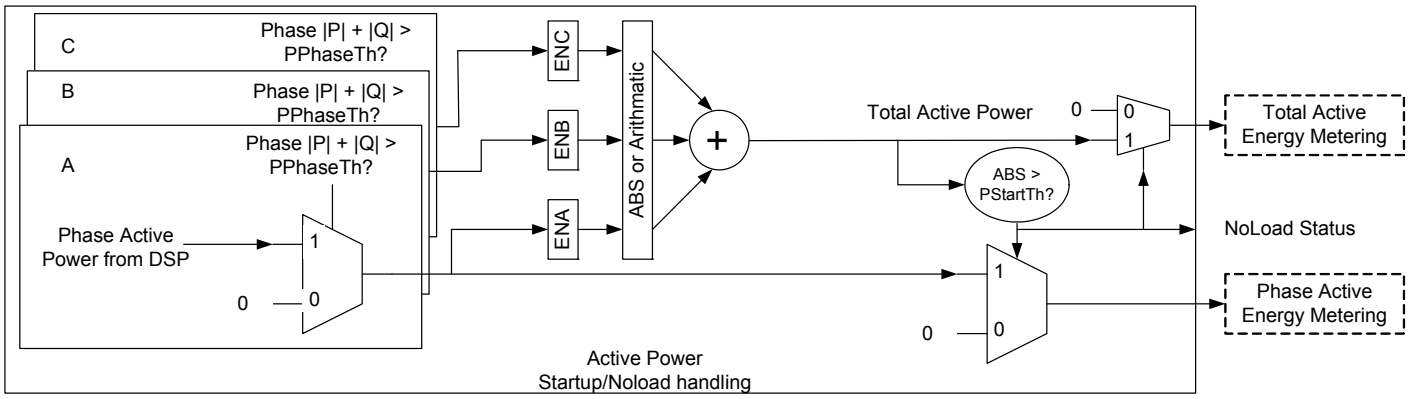


***Figure-6 Active Power Startup/Noload Processing***

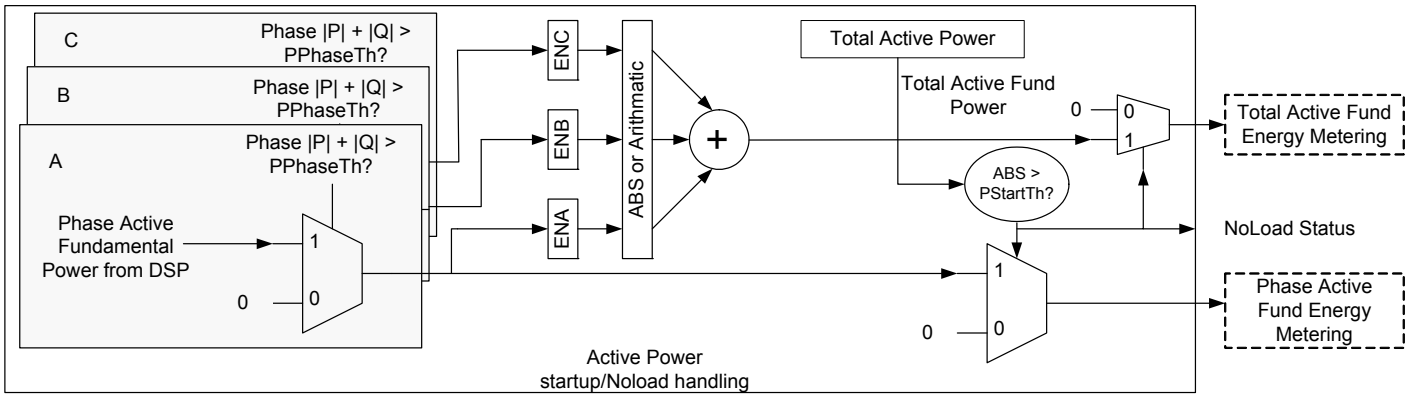


***Figure-7 Fundamental Active Power Startup/Noload Processing***

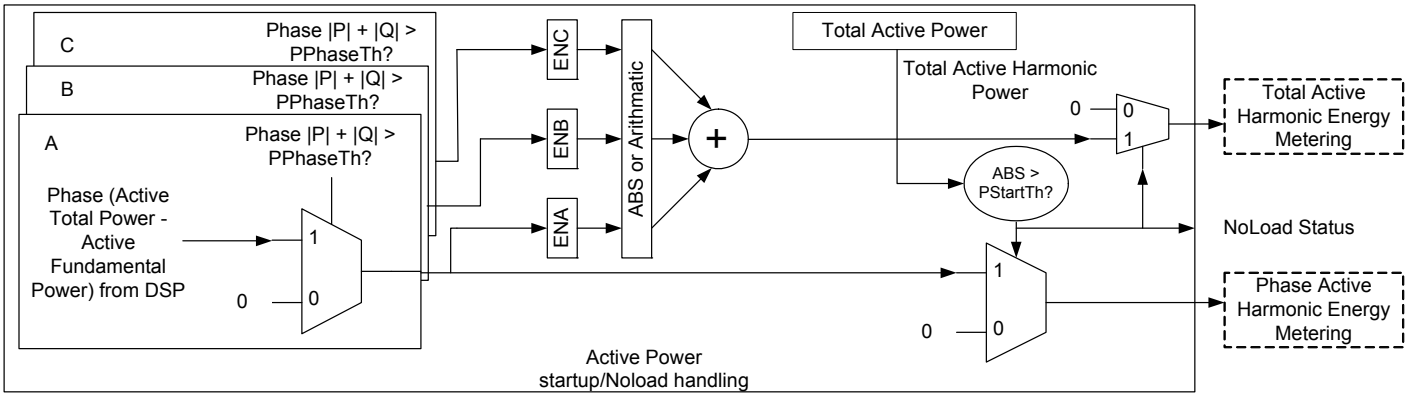


***Figure-8 Harmonic Active Power Startup/Noload Processing***

## 3.6 MEASUREMENT FUNCTION

Measured parameters can be divided to 8 types as follows:

- Active/ Reactive/ Apparent Power
- Fundamental/ Harmonic Power
- RMS for Voltage and Current
- Power Factor
- Phase Angle
- Frequency
- Temperature
- Peak Value

Measured parameters are average values that are averaged among 16 phase-voltage cycles (about 320ms at 50Hz) except for the temperature. The measured parameter update frequency is approximately 3Hz. Refer to Table-17.

### 3.6.1 ACTIVE/ REACTIVE/ APPARENT POWER

Active/ Reactive/ Apparent Power measurement registers can be divided as below:

- active, reactive, apparent power
- all-phase-sum / phase A / phase B / phase C

Altogether there are 12 power registers. Refer to 5.6.1 Power and Power Factor Registers.

Per-phase apparent power is defined as the product of measured Vrms and Irms of that phase.

All-phase-sum power is measured by arithmetically summing the per-phase measured power. The summing of phases can be configured by the MMode0 register.

### 3.6.2 FUNDAMENTAL / HARMONIC ACTIVE POWER

Fundamental / harmonic active power measurement registers can be divided as below:

- fundamental and harmonic power
- all-phase-sum / phase A / phase B / phase C

Altogether there are 8 power registers. Refer to 5.6.2 Fundamental/ Harmonic Power and Voltage/ Current RMS Registers.

### 3.6.3 MEAN POWER FACTOR (PF)

Power Factor is defined for those cases: all-phase-sum / phase A / phase B / phase C.

Altogether there are 4 power factor registers. Refer to 5.6.1 Power and Power Factor Registers.

For all-phase:

$$PF\_all = \frac{All\_phase\_\ sum\ active\_power}{All\_phase\_\ sum\ apparent\_power}$$

For each of the phase::

$$PF\_phase = \frac{active\_power}{apparent\_power}$$

### 3.6.4 VOLTAGE / CURRENT RMS

Voltage/current RMS registers can be divided as follows:

**Per-phase: Phase A / Phase B / Phase C**

Voltage / Current

**Neutral Line Current RMS:**

Neutral line current can be calculated by instantaneous value $i_N = i_A + i_B + i_C$ .

Altogether there are 7 RMS registers.

Refer to 5.6.2 Fundamental/ Harmonic Power and Voltage/ Current RMS Registers.

### 3.6.5 PHASE ANGLE

Phase Angle measurement registers can be divided as below:

- phase A / phase B / phase C
- voltage / current

Altogether there are 6 phase angle registers. Refer to 5.6.3 Peak, Frequency, Angle and Temperature Registers.

Phase Angle is measured by the time-difference between the Voltage and Current channel of the same phase.

### 3.6.6 FREQUENCY

The frequency is measured basing on the zero-crossing point of voltage channels.

The phase A voltage signal zero-crossing will be used to compute the frequency. If phase A is in the SAG condition, phase C will be used. If phase C is also in SAG condition, phase B will be used.

If all the phases are in the SAG condition, Frequency will be measured based on the channels which are not in phaseLoss condition (with the same order). If all phases are lost, the frequency will return zero.

The frequency data is not averaged (updated cycle by cycle).

Refer to 5.6.3 Peak, Frequency, Angle and Temperature Registers.

### 3.6.7 TEMPERATURE

Chip Junction-Temperature is measured roughly every 100 ms by on-chip temperature sensor.

Refer to 5.6.3 Peak, Frequency, Angle and Temperature Registers.

### 3.6.8 PEAK VALUE

Altogether there are 6 peak value registers. Refer to 5.6.3 Peak, Frequency, Angle and Temperature Registers.

Refer to 3.7.1 Instantaneous Signal Monitoring.

## 3.7 POWER QUALITY MONITORING

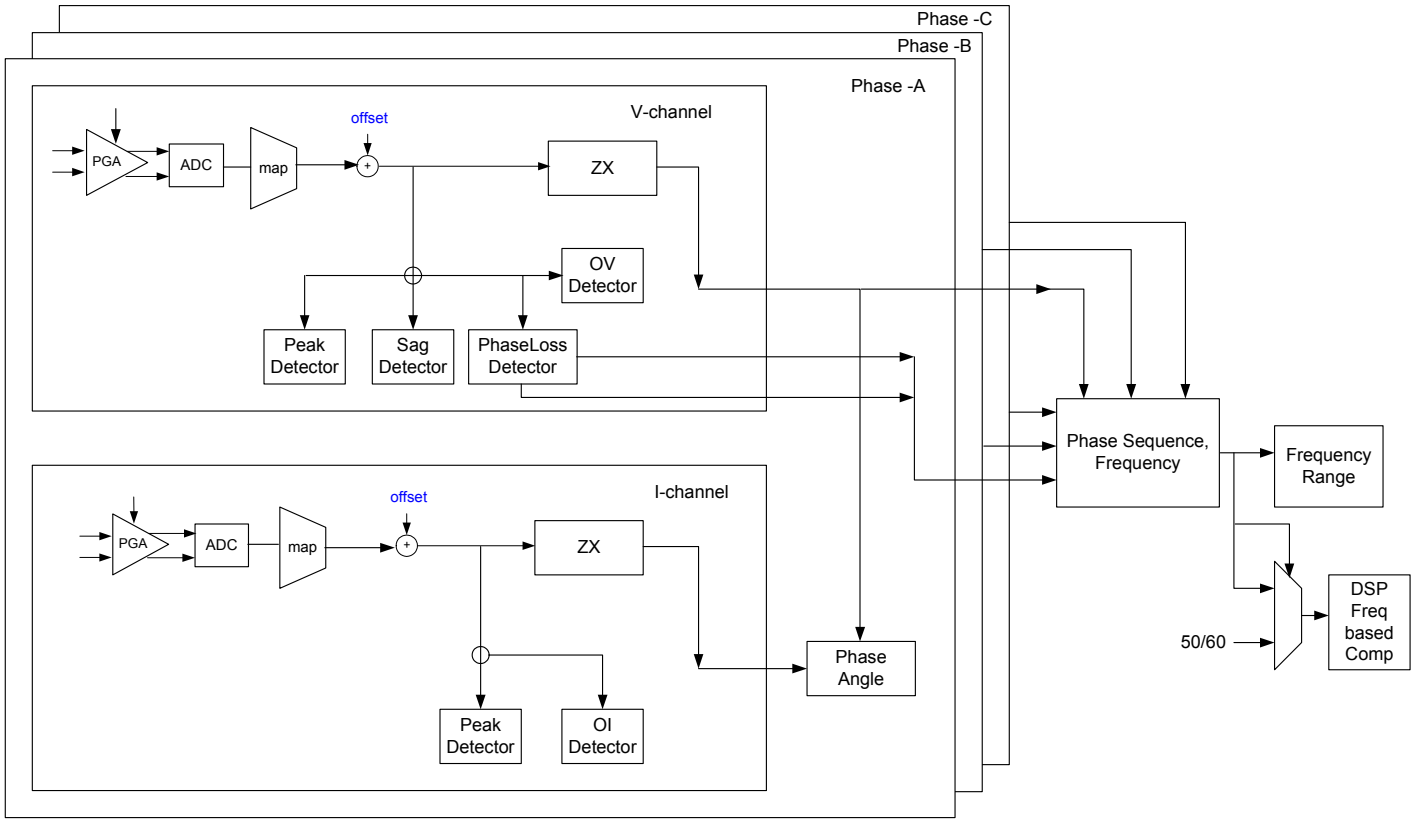


***Figure-9 Power Quality Monitor in Datapath***

### 3.7.1 INSTANTANEOUS SIGNAL MONITORING

Peak detection function:

Peak value for each channel was detected within timing period configured by the PeakDet_period bits (b15~8, SagPeakDetCfg).

The detected peak value is updated on period intersection.

Registers:

The peak value detected can be accessed through register U/I Peak registers. Refer to 5.6.3 Peak, Frequency, Angle and Temperature Registers.

### 3.7.2 INSTANTANEOUS SIGNAL RELATED STATUS AND EVENTS

The registers involved are OVth, OIth, SagTh, PhaseLossTh and SagPeakDetCfg.

The result can be reflected in EMMState0 and EMMState1 registers, as well as EMMIntState0 and EMMIntState1 registers if the corresponding bits in EMMIntEn0/EMMIntEn1 registers are set.

The threshold value has the following relationship with the RMS register (MSB-16bit):

$$xxThRegValue = \frac{RmsRegValue * \sqrt{2}}{VIgain / 2^{14}}$$

Here VIgain is Ugain register value or Igain register value.

#### 3.7.2.1 Sag Detection

Usually in the application the Sag threshold is set to be 78% of the reference voltage. The M90E32AS generates Sag event when there are less than three 8KHz samples (absolute value) greater than the sag threshold in one detecting period. Refer to 6.6 Voltage Sag and Phase Loss Timing. The detecting period length can be configured by the Sag_Period bits (b7~0, SagPeakDetCfg).

Sag status is asserted when there is no voltage instantaneous sample's absolute value goes beyond the Sag threshold in any phase. Sag status is cleared when there are three samples detected with absolute value above the Sag threshold.

For the computation of Sag threshold register value, refer to application note 46103.

The Sag event is captured by the SagPhaseIntST bits (b14-12, EMMIntState1). If the corresponding IRQ enable bits the SagPhaseIntEN bits (b14-12, EMMIntEn1) is set, IRQ can be generated. Refer to Figure-26.

#### 3.7.2.2 Phase Loss Detection

The phase loss detection detects if there is one or more phases' voltage is less than the phase-loss threshold voltage.

The processing and handling is similar to sag detection, only the threshold is different. The threshold computation flow is also similar. The typical threshold setting could be 10% Un or less.

If any phase line is detected as in phase-loss mode, that phase's zero-crossing detection function (both voltage and current) is disabled.

#### 3.7.2.3 Over Voltage (OV) Detection

When any phase's absolute voltage sample instantaneous value goes beyond the over voltage threshold, the Over Voltage status is asserted. The status is de-asserted when the voltage sample instantaneous value go back below the over voltage threshold.

Change of the Over Voltage status can generate interrupt and flagged in the EMMState0 and EMMIntState0 registers.

#### 3.7.2.4 Over Current (OI) Detection

When any phase's absolute current sample instantaneous value go beyond the over current threshold, the Over Current status is asserted. The status is de-asserted when the current sample instantaneous value go back below the over current threshold.

Change of the Over Current status can generate interrupt and flagged in the EMMState0 and EMMIntState0 registers.

### 3.7.3 FREQUENCY MONITORING RELATED STATUS AND EVENTS

The measured frequency is compared with two thresholds configured in the the FreqLoTh register and the FreqHiTh register.

If the measured frequency goes beyond the range defined by the two thresholds, the FreqLoST bit (b11, EMMState1) and FreqHiST bit (b15, EMMState1) will be asserted.

The interrupt status will be updated as well; and if enabled, interrupt signal can be asserted.

### 3.7.4 ZERO-CROSSING DETECTION

Zero-crossing detector detects the zero-crossing point of the fundamental component of voltage and current for each of the 3 phases. Refer to 6.5 Zero-Crossing Timing.

Zero-crossing signal can be independently configured and output. Refer to the definition of the ZXConfig register.

### 3.7.5 NEUTRAL LINE OVERCURRENT DETECTION

The neutral line rms current (calculated) $I_{NC}$ is checked with the threshold defined in the InWarnTh register. If the N Line current is greater than the threshold, the INOv0ST bit (b7, EMMState0) is set. IRQ0 is generated if the INOv0IntEN bit (b7, EMMIntEn0) is set.

### 3.7.6 PHASE SEQUENCE ERROR DETECTION

The phase sequence is detected in two cases: 3P4W and 3P3W, which is defined by the 3P3W bit (b8, MMode0).

3P4W case:

Correct sequence: Voltage/current zero-crossing sequence: phase-A, phase-B and phase-C.

3P3W case:

Correct sequence: Voltage/current zero-crossing between phase-A and phase-C is greater than 180 degree.

If the above mentioned criteria are violated, it is assumed as a phase sequence error, the URevWnST bit (b9, EMMState0) or the IRevWnST bit (b9, EMMState0) will be set.

## 3.8 POWER MODE

The M90E32AS has four power modes. The power mode is solely defined by the PM1 and PM0 pins.

**Table-2 Power Mode Mapping**

| PM1:PM0 Value | Power Mode |
|---|---|
| 11 | Normal (N mode) |
| 10 | Partial Measurement (M mode) |
| 01 | Detection (D mode) |
| 00 | Idle (I mode) |

### 3.8.1 NORMAL MODE (N MODE)

In Normal mode, the default is that all function blocks are active except for current detector block. Refer to Figure-10.

The current detector can be enabled and calibrated in normal mode using control bits in DetectCtrl register.

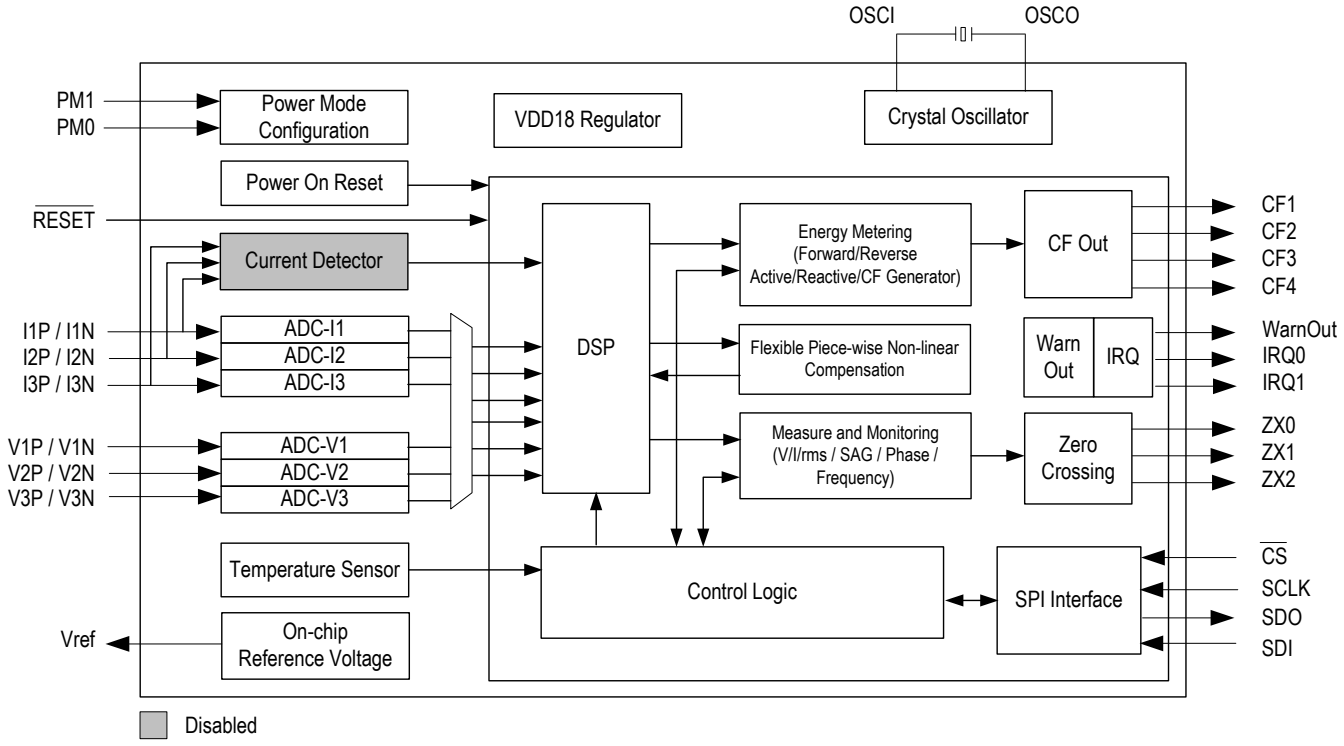


***Figure-10 Block Diagram in Normal Mode***

### 3.8.2 IDLE MODE (I MODE)

In Idle mode, all functions are shut off.

The analog blocks' power supply is powered but circuits are set into power-down mode, i.e, power supply applied but all current paths are shut off. There is very low current since only very low device leakage could exist in this mode.

The digital I/Os' supply is powered.

In I/O and analog interface, the input signals from digital core (which is not powered) will be set to known state as described in Table-3. The PM1 and PM0 pins which are controlled by external MCU are active and can configure the M90E32AS to other modes.

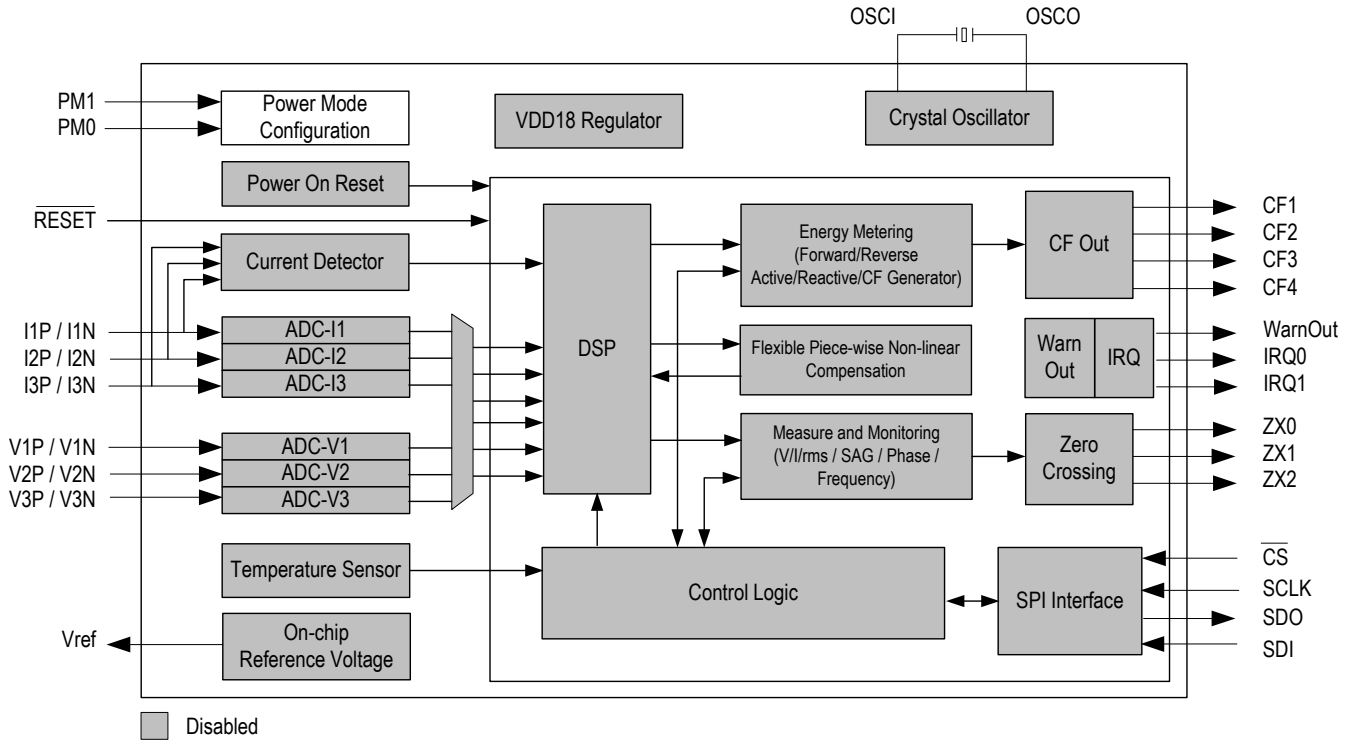


***Figure-11 Block Diagram in Idle Mode***

Please note that since the digital I/O is not shut off, the I/O circuit is active in the Idle mode. The application shall make sure that valid logic levels are applied to the I/O.

Table-3 lists digital I/O and power pins' states in Idle mode. It lists the requirements for inputs and the output level for output.

**Table-3 Digital I/O and Power Pin States in Idle Mode**

| Name | I/O type | Type | Pin State in Idle Mode |
|---|---|---|---|
| $\overline{\text{Reset}}$ | I | LVTTL | Input level shall be VDD33. |
| $\overline{\text{CS}}$ | I | LVTTL | I/O set in input mode.<br>Input level shall be VDD33 or VSS. |
| SCLK | I | LVTTL | I/O set in input mode.<br>Input level shall be VDD33 or VSS. |
| SDO | O | LVTTL | I/O set in input mode.<br>Input level shall be VDD33 or VSS. |
| SDI | I | LVTTL | I/O set in input mode.<br>Input level shall be VDD33 or VSS. |
| PM1<br>PM0 | I | LVTTL | As defined in Table-2. |

**Table-3 Digital I/O and Power Pin States in Idle Mode (Continued)**

| Name | I/O type | Type | Pin State in Idle Mode |
|---|---|---|---|
| OSCI<br>OSCO | I<br>O | OSC | Oscillator powered down.<br>OSCO stays at fixed (low) level. |
| ZX0<br>ZX1<br>ZX2 | O | LVTTL | 0 |
| CF1<br>CF2<br>CF3<br>CF4 | O | LVTTL | 0 |
| WarnOut | O | LVTTL | 0 |
| IRQ0<br>IRQ1 | O | LVTTL | 0 |
| VDD18 | I | Power | Regulated 1.8V: high impedance |
| DVDD | I | Power | Digital Power Supply: powered by system |
| AVDD | I | Power | Analog Power Supply: powered by system |
| Test | I | Input | Always tie to ground in system application |

### 3.8.3 DETECTION MODE (D MODE)

In Detection mode, the current detector is active. The current detector compares whether any phase current exceeds the configured threshold using low-power comparators.

When the current of one phase or multiple phases exceeds the configured threshold, the M90E32AS asserts the IRQ0 pin to high and hold it until power mode change. The IRQ0 state is cleared when entering or exiting Detection mode.

When the current of all three current channels exceed the configured threshold, the M90E32AS asserts the IRQ1 pin to high and hold it until power mode change. The IRQ1 state is cleared when entering or exiting Detection mode.

The threshold registers need to be programmed in Normal mode before entering Detection mode.

The digital I/O state is the same as that in Idle state (except for IRQ0/IRQ1 and PM1/PM0).

The M90E32AS has two comparators for detecting each phase's positive and negative current. Each comparator's threshold can be set individually. The two comparators are both active by default, which called 'double-side detection'. User also can enable one comparator only to save power consumption, which called 'single-side detection'.

Double-side detection has faster response and can detect 'half-wave' current. But it consumes nearly twice as much power as single-side detection.

Comparators can be power-down by configuring the DetectCtrl register. The current detector can be enabled and calibrated in normal mode using control bits in the DetectCtrl register.

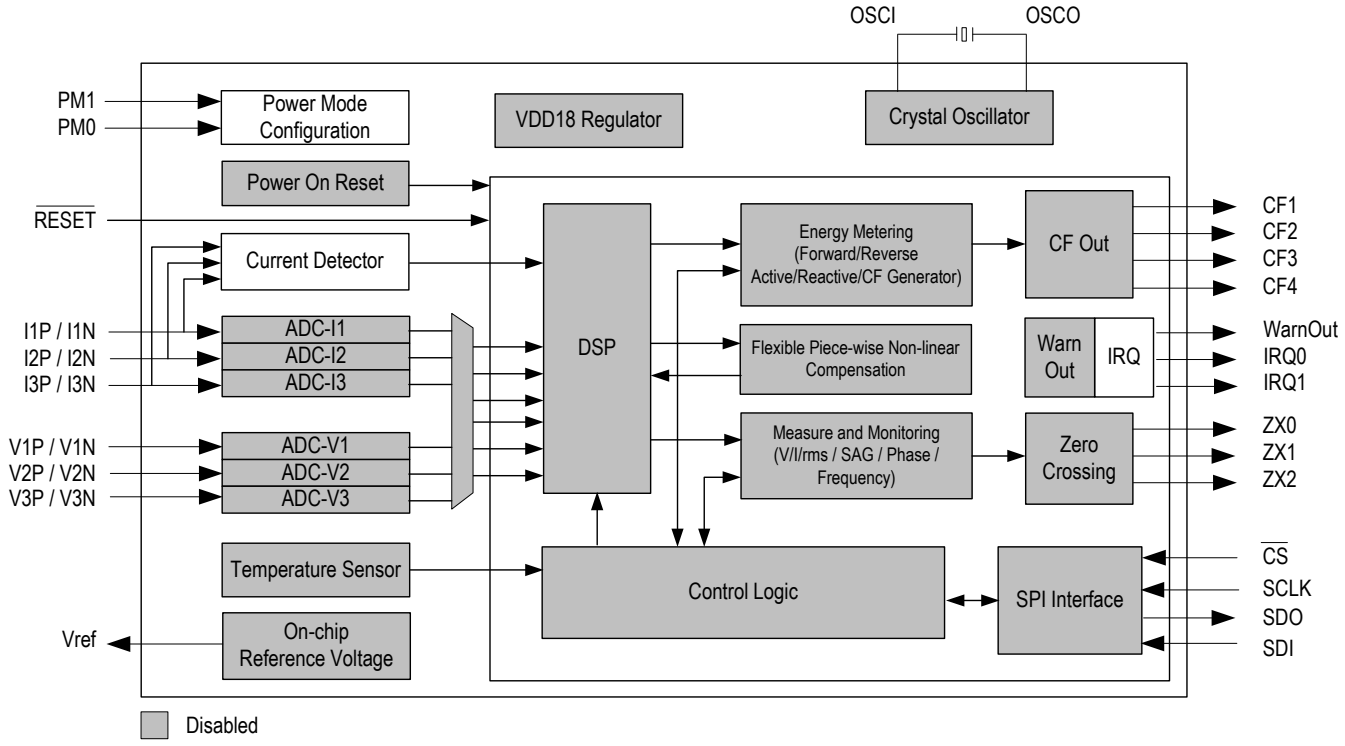


***Figure-12 Block Diagram in Detection Mode***

### 3.8.4 PARTIAL MEASUREMENT MODE (M MODE)

In this mode, all the measurements are through the same hardware that does the measurement in the normal mode. To save power, the energy accumulation block and a portion of the DSP computation code will not be running in this mode.

In this mode, There are configuration bits in the PMPwrCtrl register to get lower power if the application allows:

- Option to turn-off the three analog voltage channel if there is no need to measure voltage and power.
- Option to lower down the digital clock from 16.384Mhz to 8.192MHz

In Partial Measurement mode, CRC checking will be disabled. The interrupts will not be generated.

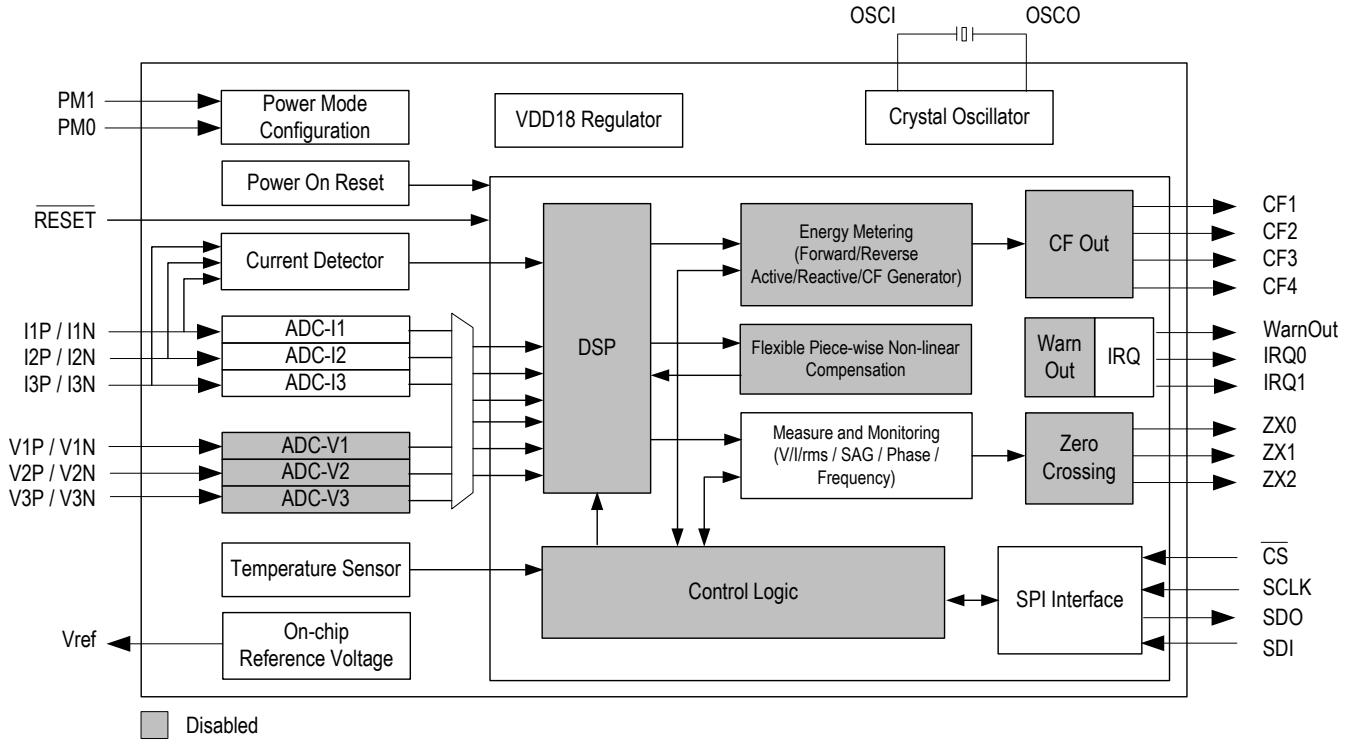


***Figure-13 Block Diagram in Partial Measurement mode***