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8-bit AVR Microcontroller

ATmega48PB/88PB/168PB

DATASHEET COMPLETE

Introduction

Atmel® ATmega48PB/88PB/168PB is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega48PB/88PB/168PB achieves throughputs approaching 1MIPS/MHz, allowing the system designer to optimize power consumption versus processing speed.

Features

- Advanced RISC architecture
  - 131 instructions – most single clock cycle execution
  - 32 x 8 general purpose working registers
  - Fully static operation
  - Up to 20MIPS throughput at 20MHz
  - On-chip 2-cycle Multiplier
- High endurance non-volatile memory segments
  - 4/8/16KBytes of in-system self-programmable Flash program memory
  - 256/512/512Bytes EEPROM
  - 512/1K/1KBytes internal SRAM
  - Write/Erase cycles: 10,000 Flash/100,000 EEPROM
  - Data retention: 20 years at 85°C/100 years at 25°C
  - Optional boot code section with independent lock bits
    - In-system programming by on-chip boot program
    - True Read-While-Write (RWW) operation
  - Programming lock for software security
- Atmel® QTouch® library support
  - Capacitive touch buttons, sliders and wheels
  - QTouch and QMatrix® acquisition
  - Up to 64 sense channels
- Peripheral Features
  - Two 8-bit Timer/Counters (TC) with separate prescaler and compare mode

  - 16-bit Timer/Counter with separate prescaler, compare mode, and capture mode
  - Real Time Counter (RTC) with separate oscillator
  - Six Pulse Width Modulation (PWM) channels
  - 8-channel 10-bit Analog-to-Digital converter (ADC) with temperature measurement
  - Programmable serial USART with start-of-frame detection
  - Master/Slave Serial Interface (SPI)
  - Byte-oriented Two-Wire serial Interface (TWI), Philips I^2C compatible
  - Programmable Watchdog Timer (WDT) with separate on-chip oscillator
  - On-chip Analog Comparator (AC)
  - Interrupt and Wake-up on pin change
    - 256-channel capacitive touch and proximity sensing
- Special microcontroller features
  - Power-On Reset (POR) and programmable brown-out detection (BOD)
  - Internal calibrated oscillator
  - External and internal interrupt sources
  - Six Sleep Modes: Idle, ADC Noise Reduction, Power-Save, Power-Down, Standby, and Extended Standby
  - Unique device ID
- I/O
  - 27 programmable I/O pins
- Packages
  - 32-pin TQFP, VFQFN
- Operating voltage
  - 1.8V – 5.5V
- Temperature range
  - -40°C to 105°C
- Speed grades
  - 0 - 4MHz at 1.8-5.5V
  - 0 - 10MHz at 2.7-5.5.V
  - 0 - 20MHz at 4.5-5.5V
- Power consumption at 1MHz, 1.8V, 25°C
  - Active mode: 0.35mA
  - Power-down mode: 0.23µA
  - Power-save mode: <1.4µA (including 32kHz RTC)

Table of Contents

1. Description

The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega48PB/88PB/168PB provides the following features: 4/8/16Kbytes of In-System Programmable Flash with Read-While-Write capabilities, 256/512/512 bytes EEPROM, 512/1K/1Kbytes SRAM, 27 general purpose I/O lines, 32 general purpose working registers, three flexible Timer/Counters with compare modes, internal and external interrupts, a serial programmable USART, a byte-oriented 2-wire Serial Interface (I²C), an SPI serial port, a 6-channel 10-bit ADC (8 channels in TQFP and VFQFN packages), a programmable Watchdog Timer with internal Oscillator, and six software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, USART, 2-wire Serial Interface, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or hardware reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except asynchronous timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low power consumption.

Atmel® offers the QTouch® library for embedding capacitive touch buttons, sliders and wheels functionality into AVR® microcontrollers. The patented charge-transfer signal acquisition offers robust sensing and includes fully debounced reporting of touch keys and includes Adjacent Key Suppression® (AKS®) technology for unambiguous detection of key events. The easy-to-use QTouch Composer allows you to explore, develop and debug your own touch applications.

The device is manufactured using Atmel's high density non-volatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed In-System through an SPI serial interface, by a conventional non-volatile memory programmer, or by an On-chip Boot program running on the AVR core. The Boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega48PB/88PB/168PB is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATmega48PB/88PB/168PB AVR is supported with a full suite of program and system development tools including: C Compilers, Macro Assemblers, Program Debugger/Simulators, In-Circuit Emulators, and Evaluation kits.

2. Configuration Summary

Table 2-1. Configuration Summary

	ATmega48PB	ATmega88PB	ATmega168PB
Pin count	32	32	32
Flash (KB)	4	8	16
SRAM (Bytes)	512	1024	1024
EEPROM (Bytes)	256	512	512
Max I/O pins	27		
SPI	1		
TWI (I^2C)	1		
USART	1		
ADC	10-bit 15ksps		
ADC channels	8		
AC	1		
8-bit Timer/Counters	2		
16-bit Timer/Counters	1		
PWM channels	6		
Operating voltage	1.8V - 5.5V		
Max operating frequency	20MHz		
Temperature range	-40°C to +105°C		

3. Ordering Information

3.1. ATmega48PB

Speed [MHz](3)	Power Supply [V]	Ordering Code(2)	Package(1)	Operational Range
20	1.8 - 5.5	ATmega48PB-AU ATmega48PB-AUR(4) ATmega48PB-MU ATmega48PB-MUR(4)	32A 32A 32MS1 32MS1	Industrial (-40°C to +85°C)
		ATmega48PB-AN ATmega48PB-ANR(4) ATmega48PB-MN ATmega48PB-MNR(4)	32A 32A 32MS1 32MS1	Industrial (-40°C to +105°C)

Note: 1. This device can also be supplied in wafer form. Contact your local Atmel sales office for detailed ordering information and minimum quantities.

2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

3. See ”Speed Grades” on page 304.

4. Tape & Reel.

Package Type	
32A	32-lead, Thin (1.0mm) Plastic Quad Flat Package (TQFP)
32MS1	32-pad, 5.0x5.0x0.9mm body, Lead Pitch 0.50mm, Very-thin Fine pitch, Quad Flat No Lead Package (VFQFN)

3.2. ATmega88PB

Speed [MHz](3)	Power Supply [V]	Ordering Code(2)	Package(1)	Operational Range
20	1.8 - 5.5	ATmega88PB-AU ATmega88PB-AUR(4) ATmega88PB-MU ATmega88PB-MUR(4)	32A 32A 32MS1 32MS	Industrial (-40°C to +85°C)
		ATmega88PB-AN ATmega88PB-ANR(4) ATmega88PB-MN ATmega88PB-MNR(4)	32A 32A 32MS1 32MS1	Industrial (-40°C to +105°C)

Note: 1. This device can also be supplied in wafer form. Contact your local Atmel sales office for detailed ordering information and minimum quantities.

2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive).Also Halide free and fully Green.

3. See ”Speed Grades” on page 304.

4. Tape & Reel.

Package Type	
32A	32-lead, Thin (1.0mm) Plastic Quad Flat Package (TQFP)
32MS1	32-pad, 5.0x5.0x0.9mm body, Lead Pitch 0.50mm, Very-thin Fine pitch, Quad Flat No Lead Package (VFQFN)

3.3. ATmega168PB

Speed [MHz]	Power Supply [V]	Ordering Code(2)	Package(1)	Operational Range
20	1.8 - 5.5	ATmega168PB-AU ATmega168PB-AUR(3) ATmega168PB-MU ATmega168PB-MUR(3)	32A 32A 32MS1 32MS1	Industrial (-40°C to +85°C)
		ATmega168PB-AN ATmega168PB-ANR(3) ATmega168PB-MN ATmega168PB-MNR(3)	32A 32A 32MS1 32MS1	Industrial (-40°C to +105°C)

Note: 1. This device can also be supplied in wafer form. Contact your local Atmel sales office for detailed ordering information and minimum quantities.

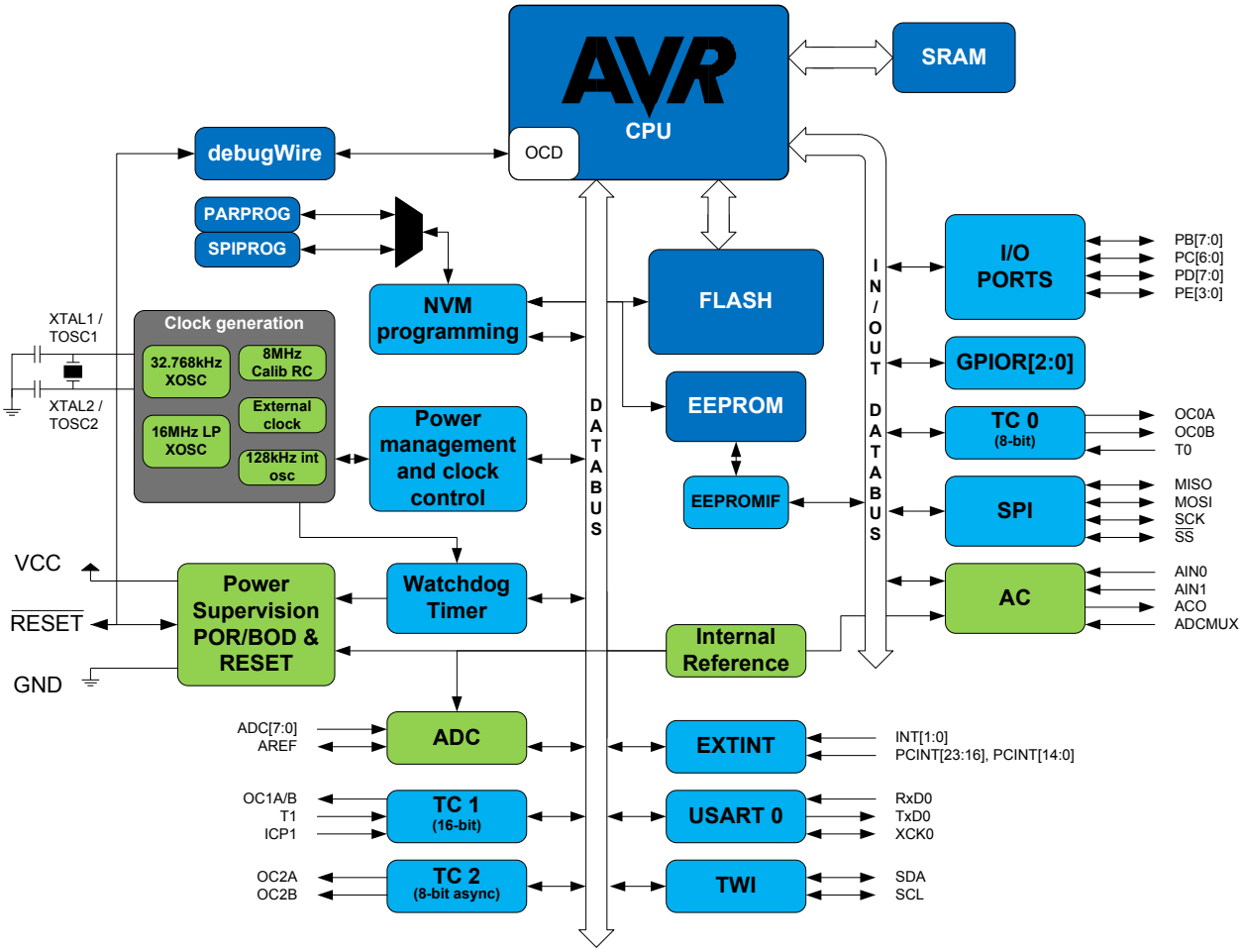
2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive).Also Halide free and fully Green.

3. Tape & Reel.

Package Type	
32A	32-lead, Thin (1.0mm) Plastic Quad Flat Package (TQFP)
32MS1	32-pad, 5.0x5.0x0.9mm body, Lead Pitch 0.50mm, Very-thin Fine pitch, Quad Flat No Lead Package (VFQFN)

4. Block Diagram

Figure 4-1. Block Diagram



5. Pin Configurations

Figure 5-1. 32 TQFP Pinout ATmega48PB/88PB/168PB

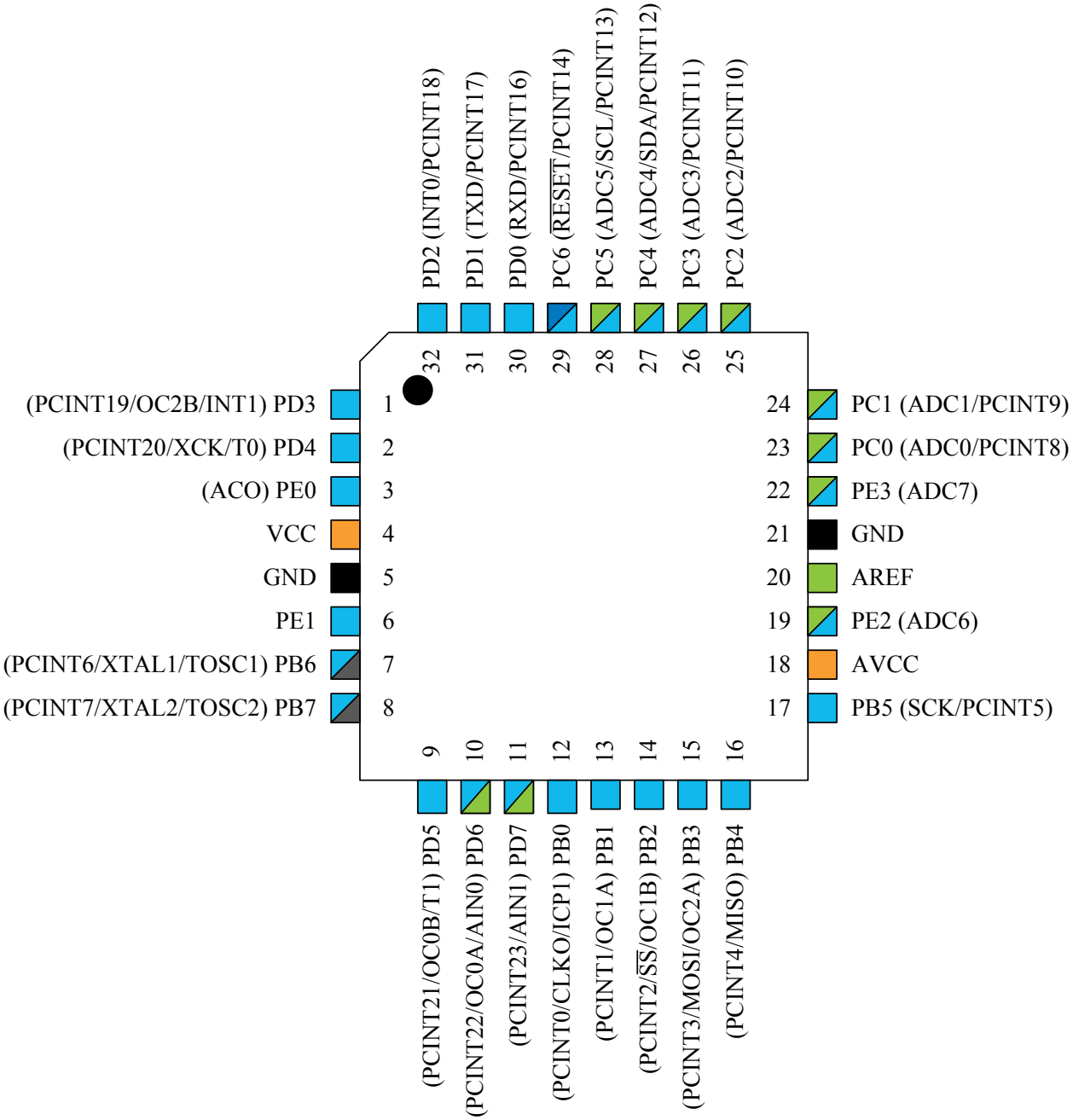
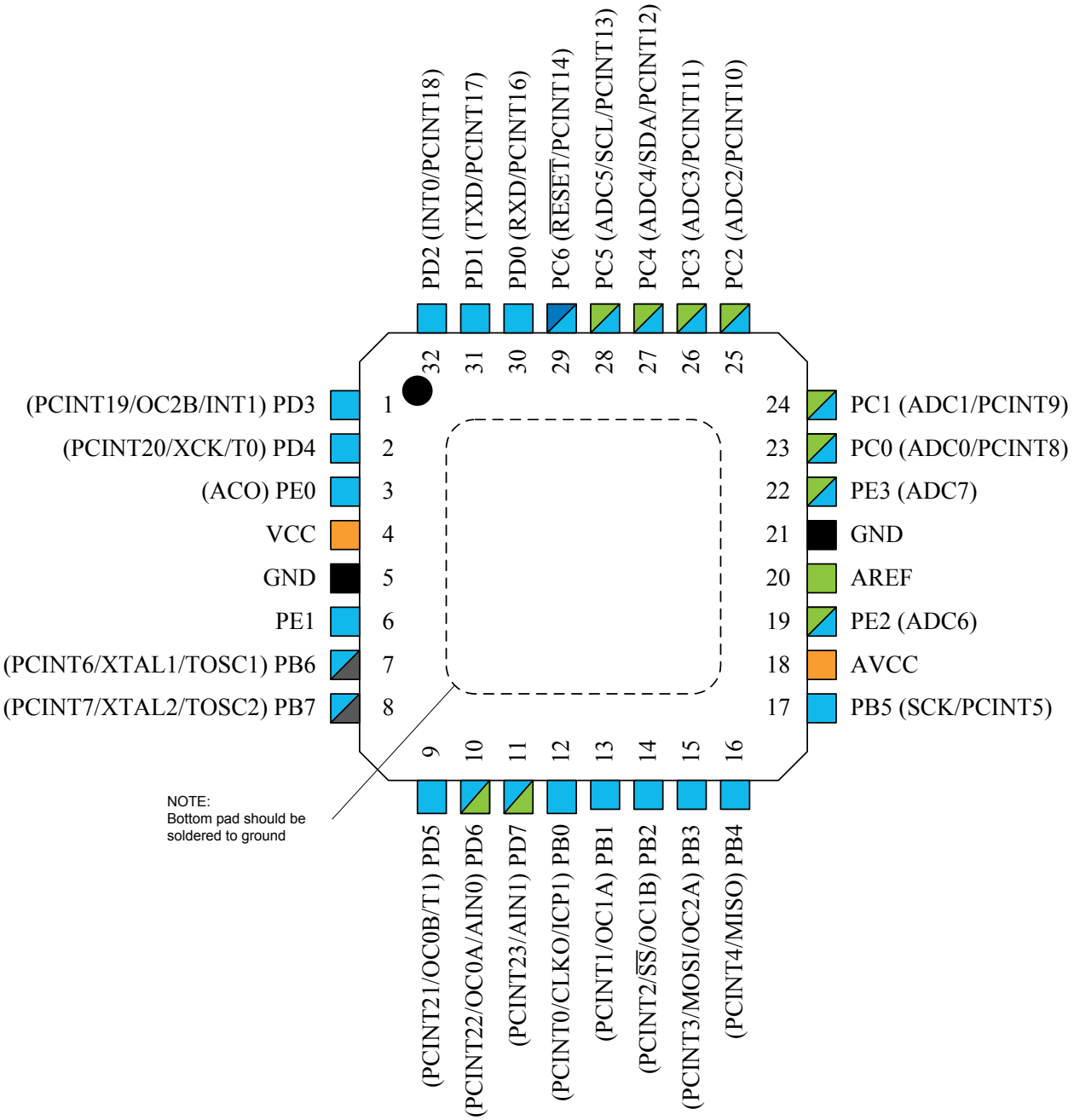


Figure 5-2. 32 VQFN Pinout ATmega48PB/88PB/168PB



5.1. Pin Descriptions

5.1.1. VCC

Digital supply voltage.

5.1.2. GND

Ground.

5.1.3. Port B (PB[7:0]) XTAL1/XTAL2/TOSC1/TOSC2

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Depending on the clock selection fuse settings, PB6 can be used as input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

Depending on the clock selection fuse settings, PB7 can be used as output from the inverting Oscillator amplifier.

If the Internal Calibrated RC Oscillator is used as chip clock source, PB[7:6] is used as TOSC[2:1] input for the Asynchronous Timer/Counter2 if the AS2 bit in ASSR is set.

Related Links

System Clock and Clock Options on page 48
Alternate Port Functions on page 109

5.1.4. Port C (PC[5:0])

Port C is a 7-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The PC[5:0] output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

5.1.5. PC6/RESET

If the RSTDISBL Fuse is programmed, PC6 is used as an I/O pin. Note that the electrical characteristics of PC6 differ from those of the other pins of Port C.

If the RSTDISBL Fuse is unprogrammed, PC6 is used as a Reset input. A low level on this pin for longer than the minimum pulse length will generate a Reset, even if the clock is not running. Shorter pulses are not guaranteed to generate a Reset.

The various special features of Port C are elaborated in Alternate Functions of Port C.

5.1.6. Port D (PD[7:0])

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Related Links

Alternate Port Functions on page 109

5.1.7. Port E (PE[3:0])

Port E is an 4-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port E output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port E pins that are externally pulled low will source current if the pull-up resistors are activated. The Port E pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Related Links

Alternate Port Functions on page 109

5.1.8. AV_{CC}

AV_{CC} is the supply voltage pin for the A/D Converter, PC[3:0], and PE[3:2]. It should be externally connected to V_{CC}, even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter. Note that PC[6:4] use digital supply voltage, V_{CC}.

5.1.9. AREF

AREF is the analog reference pin for the A/D Converter.

5.1.10. ADC[7:6] (TQFP and VFQFN Package Only)

In the TQFP and VFQFN package, ADC[7:6] serve as analog inputs to the A/D converter. These pins are powered from the analog supply and serve as 10-bit ADC channels.

6. I/O Multiplexing

Each pin is by default controlled by the PORT as a general purpose I/O and alternatively it can be assigned to one of the peripheral functions.

The following table describes the peripheral signals multiplexed to the PORT I/O pins.

Table 6-1. PORT Function Multiplexing

No	PAD	EXTINT	PCINT	ADC/AC	OSC	T/C # 0	T/C # 1	USART	I2C	SPI
1	PD[3]	INT1	PCINT19			OC2B				
2	PD[4]		PCINT20			T0		XCK0		
3	PE[0]		PCINT24	ACO			ICP4		SDA1	
4	VCC									
5	GND									
6	PE[1]		PCINT25				TC4		SCL1	
7	PB[6]		PCINT6		XTAL1/TOSC1					
8	PB[7]		PCINT7		XTAL2/TOSC2					
9	PD[5]		PCINT21			OC0B	T1			
10	PD[6]		PCINT22	AIN0		OC0A				
11	PD[7]		PCINT23	AIN1						
12	PB[0]		PCINT0		CLKO	ICP1				
13	PB[1]		PCINT1			OC1A				
14	PB[2]		PCINT2			OC1B				$\overline{SS0}$
15	PB[3]		PCINT3			OC2A		TXD1		MOSI0
16	PB[4]		PCINT4					RXD1		MISO0
17	PB[5]		PCINT5					XCK0		SCK0
18	AVCC									
19	PE[2]		PCINT26	ADC6		ICP3				$\overline{SS1}$
20	AREF									
21	GND									
22	PE[3]		PCINT27	ADC7		T3				MOSI1
23	PC[0]		PCINT8	ADC0						MISO1
24	PC[1]		PCINT9	ADC1						SCK1
25	PC[2]		PCINT10	ADC2						
26	PC[3]		PCINT11	ADC3						
27	PC[4]		PCINT12	ADC4					SDA0	
28	PC[5]		PCINT13	ADC5					SCL0	
29	PC[6]/$\overline{RESET}$		PCINT14							
30	PD[0]		PCINT16			OC3A		RXD0		
31	PD[1]		PCINT17				OC4A	TXD0		
32	PD[2]	INT0	PCINT18			OC3B	OC4B			

7. Comparison Between Processors

The ATmega48PB/88PB/168PB differ only in memory sizes, boot loader support, and interrupt vector sizes. The table below summarizes the different memory and interrupt vector sizes for the devices.

Table 7-1. Memory Size Summary

Device	Flash	EEPROM	RAM	Interrupt Vector Size
ATmega48PB	4KBytes	256Bytes	512Bytes	1 instruction word/vector
ATmega88PB	8KBytes	512Bytes	1KBytes	1 instruction word/vector
ATmega168PB	16KBytes	512Bytes	1KBytes	2 instruction words/vector

ATmega88PB/168PB support a real Read-While-Write Self-Programming Mechanism (SPM). The SPM instruction can only execute from the separate Boot Loader Section. In ATmega48PB there is no Read-While-Write support and no separate Boot Loader Section. The SPM instruction can execute from the entire Flash.

8. Resources

A comprehensive set of development tools, application notes and datasheets are available for download on http://www.atmel.com/avr.

9. Data Retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

10. About Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Confirm with the C compiler documentation for more details.

For I/O Registers located in extended I/O map, “IN”, “OUT”, “SBIS”, “SBIC”, “CBI”, and “SBI” instructions must be replaced with instructions that allow access to extended I/O. Typically “LDS” and “STS” combined with “SBRS”, “SBRC”, “SBR”, and “CBR”.

Related Links

Data Transfer on page 275

USART MSPIM Initialization on page 274

11. Capacitive Touch Sensing

11.1. QTouch Library

The Atmel® QTouch® Library provides a simple to use solution to realize touch sensitive interfaces on most Atmel AVR® microcontrollers. The QTouch Library includes support for the Atmel QTouch and Atmel QMatrix® acquisition methods.

Touch sensing can be added to any application by linking the appropriate Atmel QTouch Library for the AVR Microcontroller. This is done by using a simple set of APIs to define the touch channels and sensors, and then calling the touch sensing API's to retrieve the channel information and determine the touch sensor states.

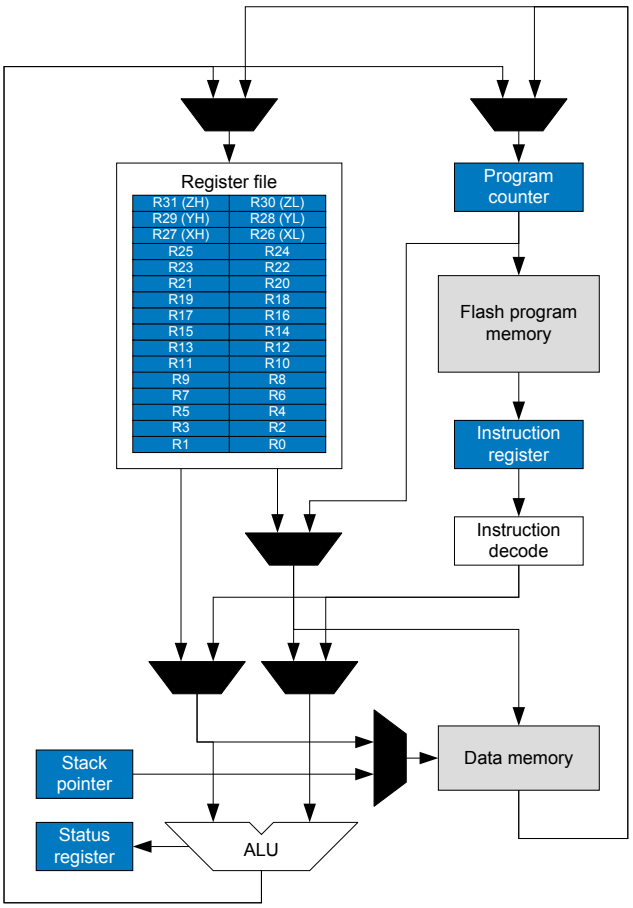
The QTouch Library is FREE and downloadable from the Atmel website at the following location: http://www.atmel.com/technologies/touch/. For implementation details and other information, refer to the Atmel QTouch Library User Guide - also available for download from the Atmel website.

12. AVR CPU Core

12.1. Overview

This section discusses the AVR core architecture in general. The main function of the CPU core is to ensure correct program execution. The CPU must therefore be able to access memories, perform calculations, control peripherals, and handle interrupts.

Figure 12-1. Block Diagram of the AVR Architecture



In order to maximize performance and parallelism, the AVR uses a Harvard architecture – with separate memories and buses for program and data. Instructions in the program memory are executed with a single level pipelining. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This concept enables instructions to be executed in every clock cycle. The program memory is In-System Reprogrammable Flash memory.

The fast-access Register File contains 32 x 8-bit general purpose working registers with a single clock cycle access time. This allows single-cycle Arithmetic Logic Unit (ALU) operation. In a typical ALU operation, two operands are output from the Register File, the operation is executed, and the result is stored back in the Register File – in one clock cycle.

Six of the 32 registers can be used as three 16-bit indirect address register pointers for Data Space addressing – enabling efficient address calculations. One of the these address pointers can also be used as an address pointer for look up tables in Flash program memory. These added function registers are the 16-bit X-, Y-, and Z-register, described later in this section.

The ALU supports arithmetic and logic operations between registers or between a constant and a register. Single register operations can also be executed in the ALU. After an arithmetic operation, the Status Register is updated to reflect information about the result of the operation.

Program flow is provided by conditional and unconditional jump and call instructions, able to directly address the whole address space. Most AVR instructions have a single 16-bit word format. Every program memory address contains a 16- or 32-bit instruction.

Program Flash memory space is divided in two sections, the Boot Program section and the Application Program section. Both sections have dedicated Lock bits for write and read/write protection. The SPM instruction that writes into the Application Flash memory section must reside in the Boot Program section.

During interrupts and subroutine calls, the return address Program Counter (PC) is stored on the Stack. The Stack is effectively allocated in the general data SRAM, and consequently the Stack size is only limited by the total SRAM size and the usage of the SRAM. All user programs must initialize the SP in the Reset routine (before subroutines or interrupts are executed). The Stack Pointer (SP) is read/write accessible in the I/O space. The data SRAM can easily be accessed through the five different addressing modes supported in the AVR architecture.

The memory spaces in the AVR architecture are all linear and regular memory maps.

A flexible interrupt module has its control registers in the I/O space with an additional Global Interrupt Enable bit in the Status Register. All interrupts have a separate Interrupt Vector in the Interrupt Vector table. The interrupts have priority in accordance with their Interrupt Vector position. The lower the Interrupt Vector address, the higher the priority.

The I/O memory space contains 64 addresses for CPU peripheral functions as Control Registers, SPI, and other I/O functions. The I/O Memory can be accessed directly, or as the Data Space locations following those of the Register File, 0x20 - 0x5F. In addition, this device has Extended I/O space from 0x60 - 0xFF in SRAM where only the ST/STS/STD and LD/LDS/LDD instructions can be used.

12.2. ALU – Arithmetic Logic Unit

The high-performance AVR ALU operates in direct connection with all the 32 general purpose working registers. Within a single clock cycle, arithmetic operations between general purpose registers or between a register and an immediate are executed. The ALU operations are divided into three main categories – arithmetic, logical, and bit-functions. Some implementations of the architecture also provide a powerful multiplier supporting both signed/unsigned multiplication and fractional format. See *Instruction Set* section for a detailed description.

12.3. Status Register

The Status Register contains information about the result of the most recently executed arithmetic instruction. This information can be used for altering program flow in order to perform conditional operations. The Status Register is updated after all ALU operations, as specified in the Instruction Set Reference. This will in many cases remove the need for using the dedicated compare instructions, resulting in faster and more compact code.

The Status Register is not automatically stored when entering an interrupt routine and restored when returning from an interrupt. This must be handled by software.