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# ATmega3208/4808 – 32-pin Data Sheet

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## megaAVR® 0-series

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### Introduction

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The ATmega3208/3209/4808/4809 microcontrollers of the megaAVR® 0-series are using the AVR® processor with hardware multiplier, running at up to 20 MHz, with a wide range of Flash sizes up to 48 KB, up to 6 KB of SRAM, and 256 bytes of EEPROM in 28-, 32-, or 48-pin package. The series uses the latest technologies from Microchip with a flexible and low-power architecture including Event System and SleepWalking, accurate analog features and advanced peripherals.

The devices described here offer Flash sizes from 32 KB to 48 KB in a 32-pin package.

### Features

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- AVR® CPU
  - Single-cycle I/O access
  - Two-level interrupt controller
  - Two-cycle hardware multiplier
- Memories
  - Up to 48 KB In-system self-programmable Flash memory
  - 256B EEPROM
  - Up to 6 KB SRAM
  - Write/Erase endurance:
    - Flash 10,000 cycles
    - EEPROM 100,000 cycles
  - Data retention: 20 Years at 85°C
- System
  - Power-on Reset (POR) circuit
  - Brown-out Detection (BOD)
  - Clock options:
    - 20 MHz low power internal oscillator with fuse-protected frequency setting
    - 32.768 kHz Ultra Low Power (ULP) internal oscillator
    - 32.768 kHz external crystal oscillator
    - External clock input
  - Single pin Unified Program Debug Interface (UPDI)
  - Three sleep modes:
    - Idle with all peripherals running and mode for immediate wake-up time
    - Standby
      - Configurable operation of selected peripherals

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- SleepWalking peripherals
    - Power Down with limited wake-up functionality
- Peripherals
  - One 16-bit Timer/Counter type A with dedicated period register, three compare channels (TCA)
  - Three 16-bit Timer/Counter type B with input capture (TCB)
  - One 16-bit Real Time Counter (RTC) running from external crystal or internal RC oscillator
  - Three USART with fractional baud rate generator, autobaud, and start-of-frame detection
  - Master/slave Serial Peripheral Interface (SPI)
  - Dual mode Master/Slave TWI with dual address match
    - Standard mode (Sm, 100 kHz)
    - Fast mode (Fm, 400 kHz)
    - Fast mode plus (Fm+, 1 MHz)
  - Event System for CPU independent and predictable inter-peripheral signaling
  - Configurable Custom Logic (CCL) with up to four programmable Lookup Tables (LUT)
  - One Analog Comparator (AC) with scalable reference input
  - One 10-bit 150 ksps Analog to Digital Converter (ADC)
  - Five selectable internal voltage references: 0.55V, 1.1V, 1.5V, 2.5V, and 4.3V
  - CRC code memory scan hardware
    - Optional automatic scan after reset
  - Watchdog Timer (WDT) with Window Mode, with separate on-chip oscillator
  - External interrupt on all general purpose pins
- I/O and Packages:
  - 27 programmable I/O lines
  - 32-pin VQFN 5x5 and TQFP 7x7
- Temperature Range: -40°C to 125°C
- Speed Grades:
  - 0-5 MHz @ 1.8V – 5.5V
  - 0-10 MHz @ 2.7V – 5.5V
  - 0-20 MHz @ 4.5V – 5.5V, -40°C to 105°C

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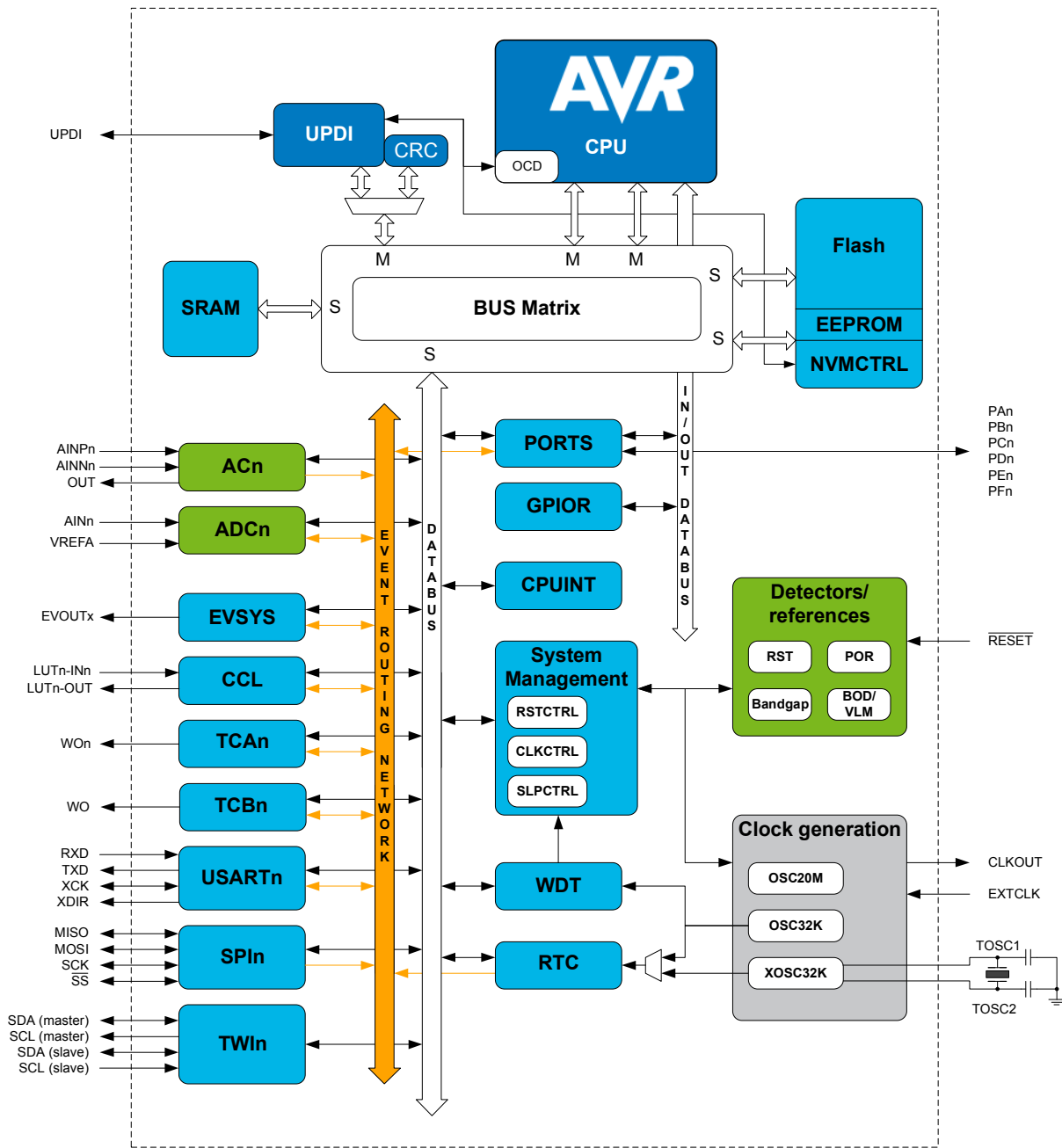
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**1. Ordering Information**

Find available ordering options online at [microchipdirect.com](http://microchipdirect.com), or contact your local sales representative.

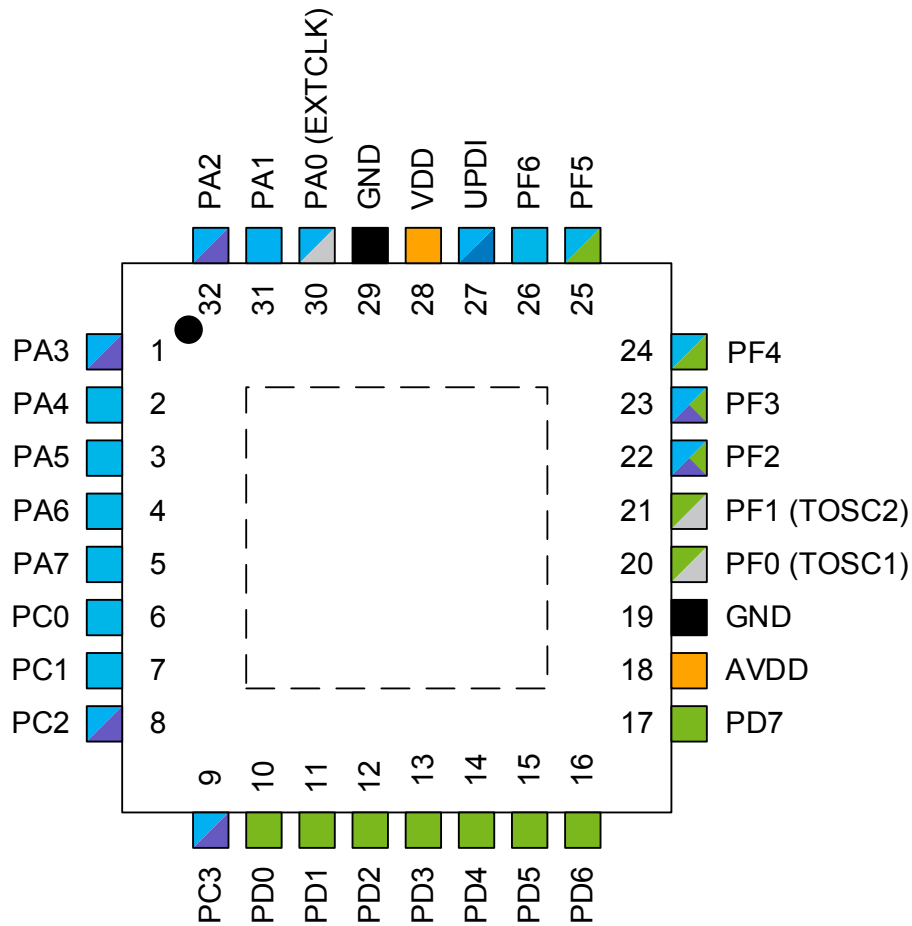
### 2. Block Diagram









### 3. Pinout






#### 3.1 32-pin QFN/TQFP



#### Power

-  Input supply
-  Ground
-  GPIO on VDD power domain
-  GPIO on AVDD power domain

#### Functionality

-  Programming, debug
-  Clock, crystal
-  TWI
-  Digital functions only
-  Analog functions



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## I/O Multiplexing and Considerations

### 4. I/O Multiplexing and Considerations

#### 4.1 Multiplexed Signals

QFN32/ TQFP32	Pin name <sup>(1,2)</sup>	Special	ADC0	AC0	USARTn	SPI0	TWI0	TCA0	TCBn	Other	CCL-LUTn
30	PA0	EXTCLK			0,TxD			0-WO0			0-IN0
31	PA1				0,RxD			0-WO1			0-IN1
32	PA2	TWI			0,XCK		SDA(MS)	0-WO2	0-WO	EVOUTA	0-IN2
1	PA3	TWI			0,XDIR		SCL(MS)	0-WO3	1-WO		0-OUT
2	PA4				0,TxD <sup>(3)</sup>	MOSI		0-WO4			
3	PA5				0,RxD <sup>(3)</sup>	MISO		0-WO5			
4	PA6				0,XCK <sup>(3)</sup>	SCK					0-OUT <sup>(3)</sup>
5	PA7	CLKOUT		OUT	0,XDIR <sup>(3)</sup>	SS				EVOUTA <sup>(3)</sup>	
6	PC0				1,TxD	MOSI <sup>(3)</sup>		0-WO0 <sup>(3)</sup>	2-WO		1-IN0
7	PC1				1,RxD	MISO <sup>(3)</sup>		0-WO1 <sup>(3)</sup>	3-WO <sup>(3)</sup>		1-IN1
8	PC2	TWI			1,XCK	SCK <sup>(3)</sup>	SDA(MS) <sup>(3)</sup>	0-WO2 <sup>(3)</sup>		EVOUTC	1-IN2
9	PC3	TWI			1,XDIR	SS <sup>(3)</sup>	SCL(MS) <sup>(3)</sup>	0-WO3 <sup>(3)</sup>			1-OUT
10	PD0		AIN0					0-WO0 <sup>(3)</sup>			2-IN0
11	PD1		AIN1	P3				0-WO1 <sup>(3)</sup>			2-IN1
12	PD2		AIN2	P0				0-WO2 <sup>(3)</sup>		EVOU_TD	2-IN2
13	PD3		AIN3	N0				0-WO3 <sup>(3)</sup>			2-OUT
14	PD4		AIN4	P1				0-WO4 <sup>(3)</sup>			
15	PD5		AIN5	N1				0-WO5 <sup>(3)</sup>			
16	PD6		AIN6	P2							2-OUT <sup>(3)</sup>
17	PD7	VREFA	AIN7	N2						EVOU_TD <sup>(3)</sup>	
18	AVDD										
19	GND										
20	PF0	TOSC1			2,TxD			0-WO0 <sup>(3)</sup>			3-IN0
21	PF1	TOSC2			2,RxD			0-WO1 <sup>(3)</sup>			3-IN1
22	PF2	TWI	AIN12		2,XCK		SDA(S) <sup>(3)</sup>	0-WO2 <sup>(3)</sup>		EVOU_TF	3-IN2
23	PF3	TWI	AIN13		2,XDIR		SCL(S) <sup>(3)</sup>	0-WO3 <sup>(3)</sup>			3-OUT
24	PF4		AIN14		2,TxD <sup>(3)</sup>			0-WO4 <sup>(3)</sup>	0-WO <sup>(3)</sup>		
25	PF5		AIN15		2,RxD <sup>(3)</sup>			0-WO5 <sup>(3)</sup>	1-WO <sup>(3)</sup>		
26	PF6	RESET			2,XCK <sup>(3)</sup>						3-OUT <sup>(3)</sup>
27	UPDI										
28	VDD										
29	GND										

**Note:**

1. Pin names are of type Pxn, with x being the PORT instance (A,B,C, ...) and n the pin number. Notation for signals is PORTx\_PINn. All pins can be used as event input.
2. All pins can be used for external interrupt, where pins Px2 and Px6 of each port have full asynchronous detection.
3. Alternate pin positions. For selecting the alternate positions, refer to the PORTMUX documentation.

## 5. Electrical Characteristics

### 5.1 Absolute Maximum Ratings

Stresses beyond those listed in this section may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 5-1. Absolute Maximum Ratings**

Symbol	Description	Conditions	Min.	Max.	Unit
V <sub>DD</sub>	Power Supply Voltage		-0.5	6	V
I <sub>VDD</sub>	Current into a V <sub>DD</sub> pin	T <sub>A</sub> =[-40, 85]°C	-	200	mA
		T <sub>A</sub> =[85, 125]°C	-	100	mA
I <sub>GND</sub>	Current out of a GND pin	T <sub>A</sub> =[-40, 85]°C	-	200	mA
		T <sub>A</sub> =[85, 125]°C	-	100	mA
V <sub>PIN</sub>	Pin voltage with respect to GND		-0.5	V <sub>DD</sub> +0.5	V
I <sub>PIN</sub>	I/O pin sink/source current		-40	40	mA
I <sub>C1</sub> <sup>(1)</sup>	I/O pin injection current except for the RESET pin	V <sub>pin</sub> <GND-0.6V or 5.5V<V <sub>pin</sub> ≤6.1V 4.9V<V <sub>DD</sub> ≤5.5V	-1	1	mA
I <sub>C2</sub> <sup>(1)</sup>	I/O pin injection current except for the RESET pin	V <sub>pin</sub> <GND-0.6V or V <sub>pin</sub> ≤5.5V V <sub>DD</sub> ≤4.9V	-15	15	mA
T <sub>storage</sub>	Storage temperature		-65	150	°C

**Note:**

- If V<sub>PIN</sub> is lower than GND-0.6V, then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as  $R = (GND-0.6V - V_{pin})/I_{Cn}$ .
  - If V<sub>PIN</sub> is greater than V<sub>DD</sub>+0.6V, then a current limiting resistor is required. The positive DC injection current limiting resistor is calculated as  $R = (V_{pin}-(V_{DD}+0.6V))/I_{Cn}$ .

### 5.2 General Operating Ratings

The device must operate within the ratings listed in this section in order for all other electrical characteristics and typical characteristics of the device to be valid.

**Table 5-2. General Operating Conditions**

Symbol	Description	Condition	Min.	Max.	Unit
V <sub>DD</sub>	Operating Supply Voltage		1.8 <sup>(1)</sup>	5.5	V
T <sub>A</sub>	Operating temperature range	Standard temperature range	-40	125	°C

**Note:**

- Operation is guaranteed down to 1.8V or VBOD with BODLEVEL=1.8V, whichever is lower.

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## Electrical Characteristics

**Table 5-3. Operating Voltage and Frequency**

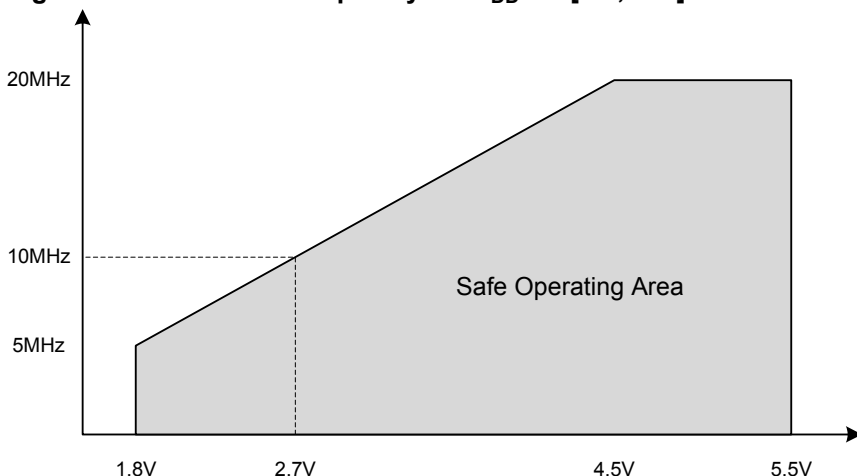
Symbol	Description	Condition	Min.	Max. <sup>(1)</sup>	Unit
f <sub>CLK_CPU</sub>	Nominal operating system clock frequency	V <sub>DD</sub> =[1.8, 5.5]V T <sub>A</sub> =[-40, 105]°C <sup>(2)</sup>	0	5	MHz
		V <sub>DD</sub> =[2.7, 5.5]V T <sub>A</sub> =[-40, 105]°C <sup>(3)</sup>	0	10	
		V <sub>DD</sub> =[4.5, 5.5]V T <sub>A</sub> =[-40, 105]°C <sup>(4)</sup>	0	20	
		V <sub>DD</sub> =[2.7, 5.5]V T <sub>A</sub> =[-40, 125]°C <sup>(3)</sup>	0	8	
		V <sub>DD</sub> =[4.5, 5.5]V T <sub>A</sub> =[-40, 125]°C <sup>(3)</sup>	0	16	

**Note:**

1. Operation is guaranteed 5% above the maximum frequency.
2. Operation is guaranteed down to BOD triggering level, V<sub>BOD</sub> with BODLEVEL=1.8V.
3. Operation is guaranteed down to BOD triggering level, V<sub>BOD</sub> with BODLEVEL=2.7V.
4. Operation is guaranteed down to BOD triggering level, V<sub>BOD</sub> with BODLEVEL=4.3V.

The maximum CPU clock frequency depends on V<sub>DD</sub>. As shown in the following figure, the Maximum Frequency vs. V<sub>DD</sub> is linear between 1.8V < V<sub>DD</sub> < 2.7V and 2.7V < V<sub>DD</sub> < 4.5V

**Figure 5-1. Maximum Frequency vs. V<sub>DD</sub> for [-40, 105]°C**



### 5.3 Power Considerations

The average die junction temperature, T<sub>J</sub> (in °C) is given from the formula

$$T_J = T_A + P_D * R_{\theta JA}$$

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## Electrical Characteristics

where  $P_D$  is the total power dissipation.

The total thermal resistance of a package ( $R_{\theta JA}$ ) can be separated into two components,  $R_{\theta JC}$  and  $R_{\theta CA}$ , representing the barrier to heat flow from the semiconductor junction to the package (case) surface ( $R_{\theta JC}$ ) and from the case to the outside ambient air ( $R_{\theta CA}$ ). These terms are related by the equation:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

$R_{\theta JC}$  is device related and cannot be influenced by the user. However,  $R_{\theta CA}$  is user dependent and can be minimized by thermal management techniques such as heat sinks, ambient air cooling, and thermal convection. Thus, good thermal management on the part of the user can significantly reduce  $R_{\theta CA}$  so that  $R_{\theta JA}$  approximately equals  $R_{\theta JC}$ .

The power dissipation curve is negatively sloped as ambient temperature increase. The maximum power dissipation is therefore at minimum ambient temperature while the highest junction temperature occurs at the maximum ambient temperature.

**Table 5-4. Power Dissipation and Junction Temperature vs Temperature**

Package	$T_A$ Range	$R_{\theta JA}$ ( $^{\circ}C/W$ )	$P_D$ (W) typical	$T_J - T_A$ ( $^{\circ}C$ ) typical
VQFN32	-40 $^{\circ}C$ to 125 $^{\circ}C$		1.0	
TQFP32	-40 $^{\circ}C$ to 125 $^{\circ}C$		1.0	

## 5.4 Power Consumption

The values are measured power consumption under the following conditions, except where noted:

- $V_{DD}=3V$
- $T_A=25^{\circ}C$
- OSC20M used as system clock source, except where otherwise specified
- System power consumption measured with peripherals disabled and without I/O drive.

**Table 5-5. Power Consumption in Active and Idle Mode**

Mode	Description	Condition	$V_{DD}$	Typ.	Max.	Unit
Active	Active power consumption	$f_{CLK\_CPU}=20$ MHz (OSC20M)	$V_{DD}=5V$	8.5	-	mA
		$f_{CLK\_CPU}=10$ MHz (OSC20M div2)	$V_{DD}=5V$	4.3	-	mA
			$V_{DD}=3V$	2.3	-	mA
			$V_{DD}=2V$	0.75	-	mA
		$f_{CLK\_CPU}=5$ MHz (OSC20M div4)	$V_{DD}=5V$	2.15	-	mA
			$V_{DD}=3V$	1.2	-	mA
			$V_{DD}=2V$	0.75	-	mA
		$f_{CLK\_CPU}=32$ KHz (OSCULP32K)	$V_{DD}=5V$	16.4	-	$\mu A$
			$V_{DD}=3V$	9.0	-	$\mu A$
$V_{DD}=2V$	6.0		-	$\mu A$		
Idle	Idle power consumption	$f_{CLK\_CPU}=20$ MHz (OSC20M)	$V_{DD}=5V$	2.8	-	mA
		$f_{CLK\_CPU}=10$ MHz (OSC20M div2)	$V_{DD}=5V$	1.4	-	mA

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## Electrical Characteristics

Mode	Description	Condition	Typ.	Max.	Unit
		$V_{DD}=3V$	0.8	-	mA
		$f_{CLK\_CPU}=5\text{ MHz (OSC20M div4)}$	$V_{DD}=5V$ 0.7	-	mA
			$V_{DD}=3V$ 0.4	-	mA
			$V_{DD}=2V$ 0.25	-	mA
		$f_{CLK\_CPU}=32\text{ KHz (OSCULP32K)}$	$V_{DD}=5V$ 5.6	-	$\mu A$
			$V_{DD}=3V$ 2.8	-	$\mu A$
			$V_{DD}=2V$ 1.8	-	$\mu A$

**Table 5-6. Power Consumption in Power-Down, Standby and Reset Mode**

Mode	Description	Condition	Typ. 25°C	Max. 85°C	Max. 125°C	Unit
Standby	Standby power consumption	RTC running at 1.024 kHz from external XOSC32K (CL=7.5pF)	$V_{DD}=3V$ 0.69	-	-	$\mu A$
		RTC running at 1.024 kHz from internal OSCULP32K	$V_{DD}=3V$ 0.65	TBD	TBD	$\mu A$
Power Down/ Standby	Power down/Standby power consumption are the same when all peripherals are stopped	All peripherals stopped	$V_{DD}=3V$ 0.10	TBD	TBD	$\mu A$
Reset	Reset power consumption	RESET line pulled low	$V_{DD}=3V$ 100	-	-	$\mu A$

## 5.5 Peripherals Power Consumption

The table below can be used to calculate the additional current consumption for the different I/O peripherals in the various operating modes.

Operating conditions:

- $V_{DD}=3V$
- $T=25^{\circ}C$
- OSC20M at 1 MHz used as system clock source, except where otherwise specified.

**Table 5-7. Peripherals Power Consumption**

Peripheral	Conditions	Typ. <sup>(1)</sup>	Unit
BOD	Continuous	19	$\mu A$
	Sampling @ 1 kHz	1.2	
TCA	16-bit count @ 1 MHz	12.6	$\mu A$

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## Electrical Characteristics

Peripheral	Conditions	Typ. <sup>(1)</sup>	Unit
TCB	16-bit count @ 1 MHz	7.4	μA
RTC	16-bit count @ OSCULP32K	1.2	μA
WDT (including OSCULP32K)		0.7	μA
OSC20M		125	μA
AC	Fast Mode <sup>(2)</sup>	92	μA
	Low Power Mode <sup>(2)</sup>	45	μA
ADC	50 ksps	325	μA
	100 ksps	340	μA
XOSC32K	C <sub>L</sub> =7.5 pF	0.5	μA
OSCULP32K		0.4	μA
USART	Enable @ 9600 Baud	13	μA
SPI (Master)	Enable @ 100 kHz	2.1	μA
TWI (Master)	Enable @ 100 kHz	23.9	μA
TWI (Slave)	Enable @ 100 kHz	17.1	μA
Flash programming	Erase Operation	1.5	mA
	Write Operation	3.0	

**Note:**

1. Current consumption of the module only. To calculate the total power consumption of the system, add this value to the base value in section “Power Consumption”.
2. CPU in Standby mode.

## 5.6 BOD and POR Characteristics

**Table 5-8. Power Supply Characteristics**

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
SRON	Power-on Slope		-	-	100	V/ms

**Table 5-9. Power On Reset (POR) Characteristics**

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
V <sub>POR</sub>	POR threshold voltage on V <sub>DD</sub> falling	V <sub>DD</sub> falls/rises at 0.5V/ms or slower	0.8	-	1.6	V
	POR threshold voltage on V <sub>DD</sub> rising		1.4	-	1.8	

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## Electrical Characteristics

**Table 5-10. Brownout Detection (BOD) Characteristics**

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
V <sub>BOD</sub>	BOD detection level (falling)	BODLEVEL=1.8V	1.71	1.78	1.85	V
		BODLEVEL=2.7V	2.45	2.60	2.75	
		BODLEVEL=4.3V	4.05	4.25	4.45	
V <sub>HYS</sub>	Hysteresis	BODLEVEL=1.8V	-	25	-	mV
		BODLEVEL=2.7V	-	40	-	
		BODLEVEL=4.3V	-	80	-	
t <sub>BOD</sub>	Detection time	Continuous	-	7	-	μs
		Sampled, 1 kHz	-	1	-	ms
		Sampled, 125 Hz	-	8	-	
t <sub>startup</sub>	Start-up time	Time from enable to ready	-	40	-	μs
ΔV <sub>LVD</sub>	Interrupt level 0	Percentage above the selected BOD level	-	4	-	%
	Interrupt level 1		-	13	-	
	Interrupt level 2		-	25	-	

## 5.7 External Reset Characteristics

**Table 5-11. External Reset Characteristics**

Mode	Description	Condition	Min.	Typ.	Max.	Unit
V <sub>VIH_RST</sub>	Input Voltage for $\overline{\text{RESET}}$		0.7×V <sub>DD</sub>	-	V <sub>DD</sub> +0.2	V
V <sub>VIL_RST</sub>	Input Low Voltage for $\overline{\text{RESET}}$		-0.2	-	0.3×V <sub>DD</sub>	
t <sub>MIN_RST</sub>	Minimum pulse width on $\overline{\text{RESET}}$ pin		300	-	-	ns
R <sub>p_RST</sub>	$\overline{\text{RESET}}$ pull-up resistor	V <sub>Reset</sub> =0V	20	35	50	kΩ

## 5.8 Oscillators and Clocks

Operating conditions:

- V<sub>DD</sub>=3V, except where specified otherwise.

**Table 5-12. 20 MHz Internal Oscillator (OSC20M) Characteristics**

Symbol	Description	Condition	Min.	Typ.	Max.	Unit	
f <sub>OSC20M</sub>	Factory calibration frequency	FREQSEL=0	T <sub>A</sub> =25°C, 3.0V		16		MHz
		FREQSEL=1			20		
f <sub>CAL</sub>	Frequency calibration range	OSC16M <sup>(2)</sup>		14.5	17.5	MHz	
		OSC20M <sup>(2)</sup>		18.5	21.5	MHz	



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## Electrical Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit	
	Factory calibration accuracy		$T_A=25^{\circ}\text{C}$ , 3.0V	TBD	$\pm 0.75$	TBD	%
$E_{\text{TOTAL}}$	Total error with 16 MHz frequency selection	From target frequency	$T_A=[0, 70]^{\circ}\text{C}$ , $V_{\text{DD}}=[1.8, 3.6]\text{V}$	TBD	$\pm 2$	TBD	%
			Full operation range	TBD	$\pm 3$	TBD	
	Total error with 20 MHz frequency selection	From target frequency	$T_A=[0, 70]^{\circ}\text{C}$ , $V_{\text{DD}}=[1.8, 3.6]\text{V}$	TBD	$\pm 2$	TBD	
			Full operation range	TBD	$\pm 3$	TBD	
$E_{\text{DRIFT}}$	Accuracy with 16 MHz Frequency Selection relative to the factory-stored frequency value	Factory calibrated $V_{\text{DD}}=3\text{V}^{(1)}$	$T_A=[0, 70]^{\circ}\text{C}$ , $V_{\text{DD}}=[1.8, 5.5]\text{V}$	TBD	$\pm 1.5$	TBD	%
	Accuracy with 20 MHz Frequency Selection relative to the factory-stored frequency value	Factory calibrated $V_{\text{DD}}=3\text{V}^{(1)}$	$T_A=[0, 70]^{\circ}\text{C}$ , $V_{\text{DD}}=[1.8, 5.5]\text{V}$	TBD	$\pm 1.5$	TBD	
$\Delta f_{\text{OSC20M}}$	Calibration step size			-	0.75	-	%
$D_{\text{OSC20M}}$	Duty cycle			-	50	-	%
$t_{\text{startup}}$	Start-up time	Within 2% accuracy		-	12	-	$\mu\text{s}$

**Note:**

1. See also the description of OSC20M on calibration.
2. Oscillator Frequencies above speed specification must be divided so that CPU clock always is within specification.

**Table 5-13. 32.768 kHz Internal Oscillator (OSCULP32K) Characteristics**

Symbol	Description	Condition	Condition	Min.	Typ.	Max.	Unit
$f_{\text{OSCULP32K}}$	Factory calibration frequency				32.768		kHz
	Factory calibration accuracy		$T_A=25^{\circ}\text{C}$ , 3.0V	-3	$\pm 2$	3	%
$E_{\text{TOTAL}}$	Total error from target frequency	Factory calibrated	$T_A=[0, 70]^{\circ}\text{C}$ , $V_{\text{DD}}=[1.8, 3.6]\text{V}$	-10	$\pm 5$	+10	%
			Full operation range	-30	$\pm 10$	+30	
$D_{\text{OSCULP32K}}$	Duty cycle				50		%
$t_{\text{startup}}$	Start-up time			-	250	-	$\mu\text{s}$

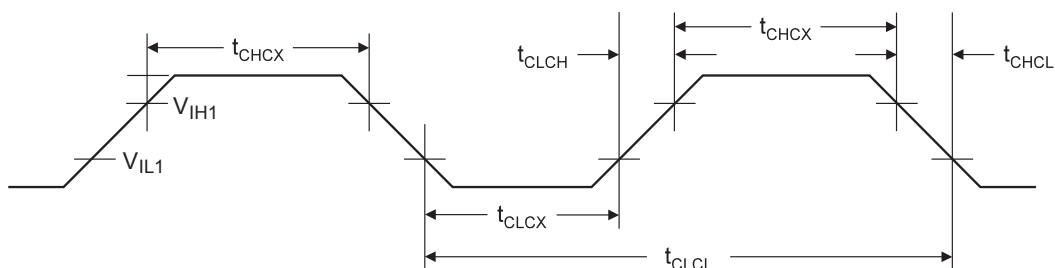
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## Electrical Characteristics

**Table 5-14. 32.768 kHz External Crystal Oscillator (XOSC32K) Characteristics**

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
$f_{out}$	Frequency		-	32.768	-	kHz
$t_{startup}$	Startup time	$C_L=7.5$ pF	-	300	-	ms
		$C_L=12.5$ pF	-	TBD	-	
$C_L$	Crystal load capacitance		7.5	-	12.5	pF
$C_{TOSC1}$	Parasitic capacitor load		-	5.5	-	pF
$C_{TOSC2}$			-	5.5	-	pF
ESR	Equivalent Series Resistance - Safety Factor=3	$C_L=7.5$ pF	-	-	80	k $\Omega$
		$C_L=12.5$ pF	-	-	40	

**Figure 5-2. External Clock Waveform Characteristics**



**Table 5-15. External Clock Characteristics**

Symbol	Description	Condition	$V_{DD}=[1.8, 5.5]V$		$V_{DD}=[2.7, 5.5]V$		$V_{DD}=[4.5, 5.5]V$		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
$f_{CLCL}$	Frequency		0	5.0	0.0	10.0	0.0	20.0	MHz
$t_{CLCL}$	Clock Period		200	-	100	-	50	-	ns
$t_{CHCX}$	High Time		80	-	40	-	20	-	ns
$t_{CLCX}$	Low Time		80	-	40	-	20	-	ns
$t_{CLCH}$	Rise Time (for maximum frequency)		-	40	-	20	-	10	ns
$t_{CHCL}$	Fall Time (for maximum frequency)		-	40	-	20	-	10	ns
$\Delta t_{CLCL}$	Change in period from one clock cycle to the next		-	20	-	20	-	20	%

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## Electrical Characteristics

### 5.9 I/O Pin Characteristics

**Table 5-16. I/O Pin Characteristics ( $T_A=[-40, 85]^{\circ}\text{C}$ ,  $V_{DD}=[1.8, 5.5]\text{V}$  unless otherwise noted)**

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
$V_{IL}$	Input Low Voltage		-0.2	-	$0.3 \times V_{DD}$	V
$V_{IH}$	Input High Voltage		$0.7 \times V_{DD}$	-	$V_{DD} + 0.2\text{V}$	V
$I_{IH} / I_{IL}$	I/O pin Input Leakage Current	$V_{DD}=5.5\text{V}$ , Pin high	-	< 0.05	-	$\mu\text{A}$
		$V_{DD}=5.5\text{V}$ , Pin low	-	< 0.05	-	
$V_{OL}$	I/O pin drive strength	$V_{DD}=1.8\text{V}$ , $I_{OL}=1.5\text{ mA}$	-	-	0.36	V
		$V_{DD}=3.0\text{V}$ , $I_{OL}=7.5\text{ mA}$	-	-	0.6	
		$V_{DD}=5.0\text{V}$ , $I_{OL}=15\text{ mA}$	-	-	1	
$V_{OH}$	I/O pin drive strength	$V_{DD}=1.8\text{V}$ , $I_{OH}=1.5\text{ mA}$	1.44	-	-	V
		$V_{DD}=3.0\text{V}$ , $I_{OH}=7.5\text{ mA}$	2.4	-	-	
		$V_{DD}=5.0\text{V}$ , $I_{OH}=15\text{ mA}$	4	-	-	
$I_{total}$	Maximum combined I/O sink/ source current per pin group <sup>(1)</sup>		-	-	100	mA
	Maximum combined I/O sink/ source current per pin group <sup>(1)</sup>	$T_A=25^{\circ}\text{C}$	-	-	200	
$t_{RISE}$	Rise time	$V_{DD}=3.0\text{V}$ , load=20 pF	-	2.5	-	ns
		$V_{DD}=5.0\text{V}$ , load=20 pF	-	1.5	-	
		$V_{DD}=3.0\text{V}$ , load=20 pF, slew rate enabled	-	19	-	
		$V_{DD}=5.0\text{V}$ , load=20 pF, slew rate enabled	-	9	-	
$t_{FALL}$	Fall time	$V_{DD}=3.0\text{V}$ , load=20 pF	-	2.0	-	ns
		$V_{DD}=5.0\text{V}$ , load=20 pF	-	1.3	-	
		$V_{DD}=3.0\text{V}$ , load=20 pF, slew rate enabled	-	21	-	
		$V_{DD}=5.0\text{V}$ , load=20 pF, slew rate enabled	-	11	-	
$C_{pin}$	I/O pin capacitance except for TOSC, VREFA, and TWI pins		-	3.5	-	pF
$C_{pin}$	I/O pin capacitance on TOSC pins		-	4	-	pF
$C_{pin}$	I/O pin capacitance on TWI pins		-	10	-	pF
$C_{pin}$	I/O pin capacitance on VREFA pin		-	14	-	pF
$R_p$	Pull-up resistor		20	35	50	k $\Omega$

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## Electrical Characteristics

**Note:**

- Pin group A (PA[7:0]), PF[6:2]), pin group B (PB[7:0], PC[7:0]), pin group C (PD:7:0, PE[3:0], PF[1:0]). For 28-pin and 32-pin devices pin group A and B should be seen as a single group. The combined continuous sink/source current for each individual group should not exceed the limits.

### 5.10 VREF

**Table 5-17. Internal Voltage Reference Characteristics**

Symbol	Description	Min.	Typ.	Max.	Unit
$t_{start}$	Start-up time	-	25	-	$\mu s$
$V_{DDINT055V}$	Power supply voltage range for INT055V	1.8	-	5.5	V
$V_{DDINT11V}$	Power supply voltage range for INT11V	1.8	-	5.5	
$V_{DDINT15V}$	Power supply voltage range for INT15V	1.8	-	5.5	
$V_{DDINT25V}$	Power supply voltage range for INT25V	3.0	-	5.5	
$V_{DDINT43V}$	Power supply voltage range for INT43V	4.8	-	5.5	

**Table 5-18. ADC Internal Voltage Reference Characteristics<sup>(1)</sup>**

Symbol <sup>(2)</sup>	Description	Condition	Min.	Typ.	Max.	Unit
INT11V	Internal reference voltage	$V_{DD}=[1.8V, 3.6V]$ $T=[0 - 105]^{\circ}C$	-2.0		2.0	%
INT055V INT15V INT25V	Internal reference voltage	$V_{DD}=[1.8V, 3.6V]$ $T=[0 - 105]^{\circ}C$	-3.0		3.0	
INT055V INT11V INT15V INT25V INT43V	Internal reference voltage	$V_{DD}=[1.8V, 5.5V]$ $T=[-40 - 125]^{\circ}C$	-5.0		5.0	

**Note:**

- These values are based on characterization and not covered by production test limits.
- The symbols INTxxV refer to the respective values of the ADC0REFSEL bit field in the VREF.CTRLA register.

**Table 5-19. AC Internal Voltage Reference Characteristics<sup>(1)</sup>**

Symbol <sup>(2)</sup>	Description	Condition	Min.	Typ.	Max.	Unit
INT055V INT11V	Internal reference voltage	$V_{DD}=[1.8V, 3.6V]$ $T=[0 - 105]^{\circ}C$	-3.0		3.0	%

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## Electrical Characteristics

Symbol <sup>(2)</sup>	Description	Condition	Min.	Typ.	Max.	Unit
INT15V INT25V						
INT055V INT11V INT15V INT25V INT43V	Internal reference voltage	$V_{DD}=[1.8V, 5.5V]$ $T=[-40 - 125]^{\circ}C$	-5.0		5.0	

**Note:**

1. These values are based on characterization and not covered by production test limits.
2. The symbols INTxxV refer to the respective values of the AC0REFSEL bit field in the VREF.CTRLA register.

## 5.11 ADC

### 5.11.1 Internal Reference Characteristics

Operating conditions:

- $V_{DD} = 1.8$  to  $5.5V$
- Temperature =  $-40^{\circ}C$  to  $125^{\circ}C$
- DUTYCYC = 25%
- $CLK_{ADC} = 13 * f_{ADC}$
- SAMPCAP is 10 pF for 0.55V reference, while it is set to 5 pF for  $V_{REF} \geq 1.1V$
- Applies for all allowed combinations of  $V_{REF}$  selections and Sample Rates unless otherwise noted

**Table 5-20. Power Supply, Reference, and Input Range**

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
$V_{DD}$	Supply voltage	$CLK_{ADC} \leq 1.5$ MHz	1.8	-	5.5	V
		$CLK_{ADC} > 1.5$ MHz	2.7	-	5.5	
$V_{REF}$	Reference voltage	REFSEL = Internal reference	0.55	-	$V_{DD}-0.5$	V
		REFSEL = External reference	1.1	-	$V_{DD}$	
		REFSEL = $V_{DD}$	1.8	-	5.5	
$C_{IN}$	Input capacitance	SAMPCAP=5 pF	-	5	-	pF
		SAMPCAP=10 pF	-	10	-	
$V_{IN}$	Input voltage range		0	-	$V_{REF}$	V
$I_{BAND}$	Input bandwidth	$1.1V \leq V_{REF}$	-	-	57.5	kHz

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## Electrical Characteristics

**Table 5-21. Clock and Timing Characteristics**

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
$f_{ADC}$	Sample rate	$1.1V \leq V_{REF}$	15	-	115	ksps
		$1.1V \leq V_{REF}$ (8-bit resolution)	15	-	150	
		$V_{REF} = 0.55V$ (10 bits)	7.5	-	20	
$CLK_{ADC}$	Clock frequency	$V_{REF} = 0.55V$ (10 bits)	100	-	260	kHz
		$1.1V \leq V_{REF}$ (10 bits)	200	-	1500	
		$1.1V \leq V_{REF}$ (8-bit resolution)	200	-	2000	
$T_s$	Sampling time		2	2	33	$CLK_{ADC}$ cycles
$T_{CONV}$	Conversion time (latency)	Sampling time = $2 CLK_{ADC}$	8.7	-	50	$\mu s$
$T_{START}$	Start-up time	Internal $V_{REF}$	-	22	-	$\mu s$

**Table 5-22. Accuracy Characteristics Internal Reference<sup>(2)</sup>**

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit	
Res	Resolution		-	10	-	bit	
INL	Integral Non-linearity	REFSEL = INTERNAL $V_{REF} = 0.55V$	$f_{ADC} = 7.7$ ksps	-	1.0	-	LSB
		REFSEL = INTERNAL or VDD	$f_{ADC} = 15$ ksps	-	1.0	-	
		REFSEL = INTERNAL or VDD $1.1V \leq V_{REF}$	$f_{ADC} = 77$ ksps	-	1.0	-	
			$f_{ADC} = 115$ ksps	-	1.2	-	
DNL <sup>(1)</sup>	Differential Non-linearity	REFSEL = INTERNAL $V_{REF} = 0.55V$	$f_{ADC} = 7.7$ ksps	-	0.6	-	LSB
		REFSEL = INTERNAL $V_{REF} = 1.1V$	$f_{ADC} = 15$ ksps	-	0.4	-	
		REFSEL = INTERNAL or VDD $1.5V \leq V_{REF}$	$f_{ADC} = 15$ ksps	-	0.4	-	
		REFSEL = INTERNAL or VDD $1.1V \leq V_{REF}$	$f_{ADC} = 15$ ksps	-	0.4	-	
			$f_{ADC} = 77$ ksps	-	0.4	-	

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## Electrical Characteristics

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit	
		REFSEL = INTERNAL $1.1V \leq V_{REF}$	$f_{ADC} = 115$ ksps	-	0.5	-	
		REFSEL = VDD $1.8V \leq V_{REF}$	$f_{ADC} = 115$ ksps	-	0.9	-	
EABS	Absolute accuracy	REFSEL = INTERNAL $V_{REF} = 1.1V$	$T = [0-105]^{\circ}C$ $V_{DD} = [1.8V-3.6V]$	-	<10	-	LSB
			$V_{DD} = [1.8V-3.6V]$	-	<15	-	
		REFSEL = VDD		-	2	-	
		REFSEL = INTERNAL		-	<35	-	
EGAIN	Gain error	REFSEL = INTERNAL $V_{REF} = 1.1V$	$T = [0-105]^{\circ}C$ $V_{DD} = [1.8V-3.6V]$	-	$\pm 15$	-	LSB
			$V_{DD} = [1.8V-3.6V]$	-	$\pm 20$	-	
		REFSEL = VDD		-	2	-	
		REFSEL = INTERNAL		-	$\pm 35$	-	
EOFF	Offset error	REFSEL = INTERNAL $V_{REF} = 0.55V$		-	-0.5	-	LSB
		REFSEL = INTERNAL $1.1V \leq V_{REF}$		-	-0.5	-	LSB

**Note:**

1. A DNL error of less than or equal to 1 LSB ensures a monotonic transfer function with no missing codes.
2. These values are based on characterization and not covered by production test limits.
3. Reference setting and  $f_{ADC}$  must fulfill the specification in "Clock and Timing Characteristics" and "Power supply, Reference, and Input Range" tables.

### 5.11.2 External Reference Characteristics

Operating conditions:

- $V_{DD} = 1.8$  to  $5.5V$
- Temperature =  $-40^{\circ}C$  to  $125^{\circ}C$
- DUTYCYC = 25%
- $CLK_{ADC} = 13 * f_{ADC}$
- SAMPCAP is 5 pF



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## Electrical Characteristics

The accuracy characteristics numbers are based on characterization of the following input reference levels and  $V_{DD}$  ranges:

- $V_{ref} = 1.8\text{ V}$ ,  $V_{DD} = 1.8\text{ to }5.5\text{ V}$
- $V_{ref} = 2.6\text{ V}$ ,  $V_{DD} = 2.7\text{ to }5.5\text{ V}$
- $V_{ref} = 4.096\text{ V}$ ,  $V_{DD} = 4.5\text{ to }5.5\text{ V}$
- $V_{ref} = 4.3\text{ V}$ ,  $V_{DD} = 4.5\text{ to }5.5\text{ V}$

**Table 5-23. Accuracy Characteristics External Reference<sup>(2)</sup>**

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
Res	Resolution		-	10	-	bit
INL	Integral Non-linearity	$f_{ADC}=15\text{ ksps}$	-	0.9	-	LSB
		$f_{ADC}=77\text{ ksps}$	-	0.9	-	
		$f_{ADC}=115\text{ ksps}$	-	1.2	-	
DNL <sup>(1)</sup>	Differential Non-linearity	$f_{ADC}=15\text{ ksps}$	-	0.2	-	LSB
		$f_{ADC}=77\text{ ksps}$	-	0.4	-	
		$f_{ADC}=115\text{ ksps}$	-	0.8	-	
EABS	Absolute accuracy	$f_{ADC}=15\text{ ksps}$	-	2	-	LSB
		$f_{ADC}=77\text{ ksps}$	-	2	-	
		$f_{ADC}=115\text{ ksps}$	-	2	-	
EGAIN	Gain error	$f_{ADC}=15\text{ ksps}$	-	2	-	LSB
		$f_{ADC}=77\text{ ksps}$	-	2	-	
		$f_{ADC}=115\text{ ksps}$	-	2	-	
E0FF	Offset error		-	-0.5	-	LSB

**Note:**

1. A DNL error of less than or equal to 1 LSB ensures a monotonic transfer function with no missing codes.
2. These values are based on characterization and not covered by production test limits.

## 5.12 AC

**Table 5-24. Analog Comparator Characteristics**

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
$V_{IN}$	Input Voltage	Low Power Mode	-0.2	-	$V_{DD}$	V
		High speed mode	-0.2	-	$V_{DD}$	
$C_{IN}$	Input Pin Capacitance	PD1 to PD6	-	3.5	-	pF
		PD7	-	14	-	

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## Electrical Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
V <sub>OFF</sub>	Input Offset Voltage, Low Power Mode	0.7V < V <sub>IN</sub> < (V <sub>DD</sub> - 0.7V)	TBD	±10	TBD	mV
		V <sub>IN</sub> = [0V, V <sub>DD</sub> ]	-	±30	-	
	Input Offset Voltage, High-speed Mode	0.7V < V <sub>IN</sub> < (V <sub>DD</sub> - 0.7V)	TBD	±5	TBD	
		V <sub>IN</sub> = [-0.2V, V <sub>DD</sub> ]	-	±20	-	
I <sub>L</sub>	Input Leakage Current		-	5	-	nA
T <sub>START</sub>	Start-up Time		-	1.3	-	µs
V <sub>HYS</sub>	Hysteresis, High-speed mode	HYSMODE=0x0	-	0	-	mV
		HYSMODE=0x1	-	10	-	
		HYSMODE=0x2	-	25	-	
		HYSMODE=0x3	-	50	-	
t <sub>PD</sub>	Propagation Delay	25 mV Overdrive, V <sub>DD</sub> ≥ 2.7V, High speed mode	-	50	-	ns
		25 mV Overdrive, V <sub>DD</sub> ≥ 2.7V, Low Power Mode	-	150	-	

### 5.13 UPDI Timing

#### UPDI Enable Sequence

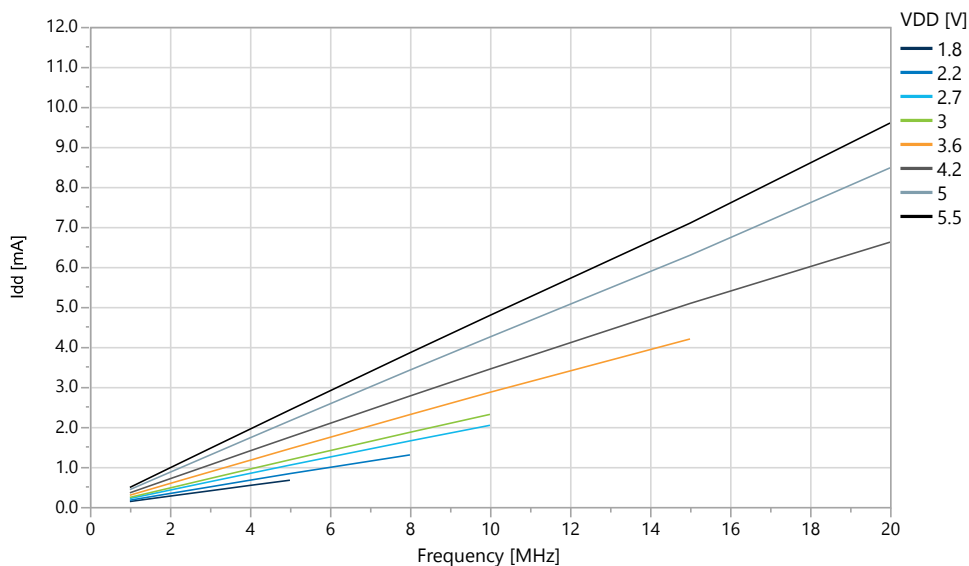
Symbol	Description	Min.	Max.	Unit
T <sub>RES</sub>	Duration of Handshake/Break on RESET	10	200	µs
T <sub>UPDI</sub>	Duration of UPDI.txd=0	10	200	µs
T <sub>Deb0</sub>	Duration of Debugger.txd=0	0.2	1	µs
T <sub>DebZ</sub>	Duration of Debugger.txd=z	200	14000	µs

## 6. Typical Characteristics

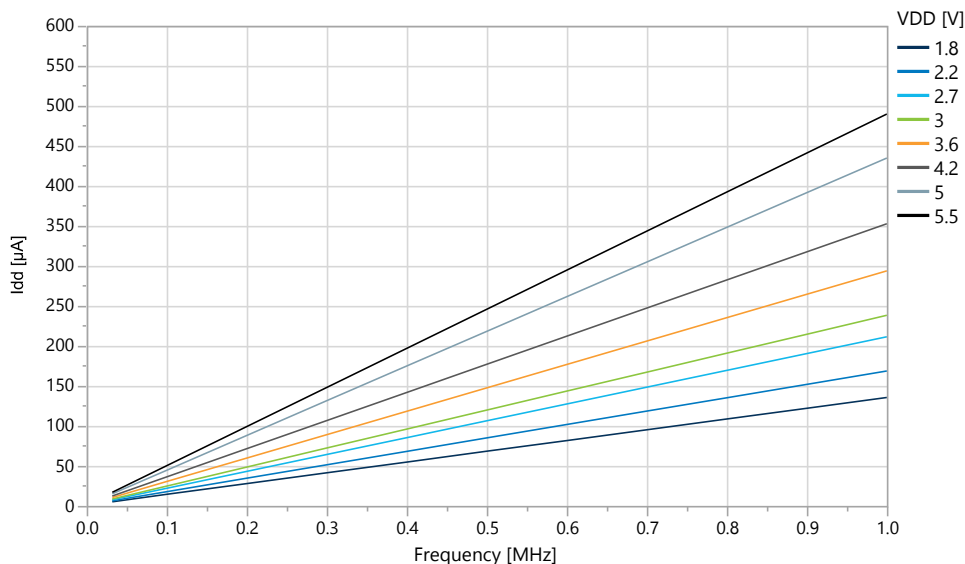
### 6.1 Power Consumption

#### 6.1.1 Supply Currents in Active Mode

**Figure 6-1. Active Supply Current vs. Frequency (1-20 MHz) at T=25°C**



**Figure 6-2. Active Supply Current vs. Frequency [0.1, 1.0] MHz at T=25°C**



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## Typical Characteristics

Figure 6-3. Active Supply Current vs. Temperature (f=20 MHz OSC20M)

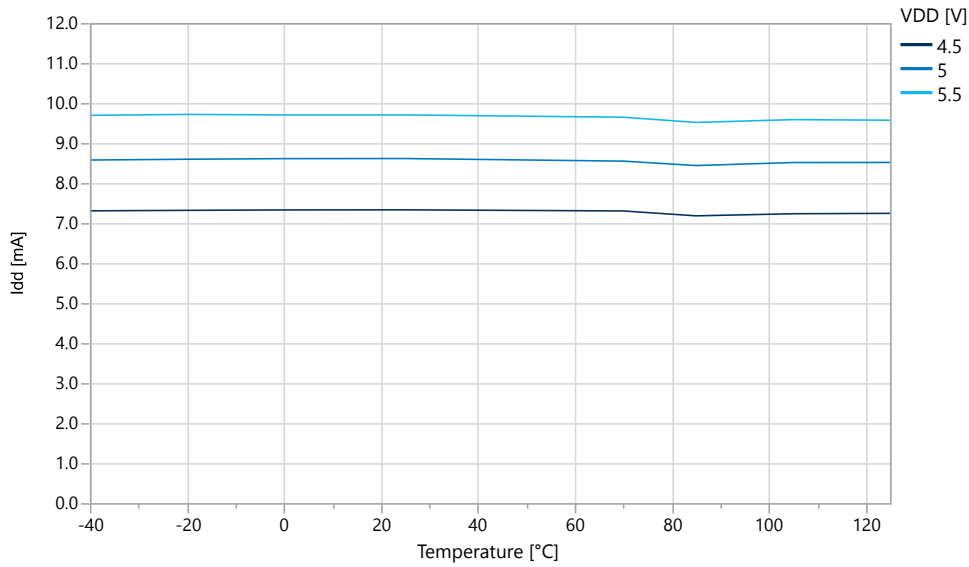


Figure 6-4. Active Supply Current vs.  $V_{DD}$  (f=[1.25, 20] MHz OSC20M) at T=25°C

