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8-bit AVR Microcontroller

ATmega324PB

DATASHEET SUMMARY

Introduction

The Atmel® picoPower® ATmega324PB is a low-power CMOS 8-bit microcontroller based on the AVR® enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega324PB achieves throughputs close to 1MIPS per MHz. This empowers system designer to optimize the device for power consumption versus processing speed.

Feature

High Performance, Low Power Atmel®AVR® 8-Bit Microcontroller Family

- Advanced RISC Architecture
  - 131 Powerful Instructions
  - Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 20 MIPS Throughput at 20MHz
  - On-Chip 2-cycle Multiplier
- High Endurance Non-Volatile Memory Segments
  - 32KBytes of In-System Self-Programmable Flash Program Memory
  - 1KBytes EEPROM
  - 2KBytes Internal SRAM
  - Write/Erase Cycles: 10,000 Flash/100,000 EEPROM
  - Data Retention: 20 Years at 85°C
  - Optional Boot Code Section with Independent Lock Bits
    - In-System Programming by On-chip Boot Program
    - True Read-While-Write Operation
  - Programming Lock for Software Security
- Atmel QTouch® Library Support
  - Capacitive Touch Buttons, Sliders and Wheels
  - QTouch and QMatrix Acquisition
- JTAG (IEEE std. 1149.1 Compliant) Interface

This is a summary document. A complete document is available on our Web site at www.atmel.com

  - Boundary-Scan Capabilities According to the JTAG Standard
  - Extensive On-chip Debug Support
  - Programming of Flash, EEPROM, Fuses, and Lock Bits Through the JTAG Interface
- Peripheral Features
  - Peripheral Touch Controller (PTC)
    - Capacitive Touch buttons, Sliders and Wheels
    - 32 Self-Sap Channels and 256 Mutual Cap Channels
  - Two 8-bit Timer/Counters with Separate Prescaler and Compare Mode
  - Three 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Ten PWM Channels
  - 8-Channel 10-Bit ADC
    - Differential Mode with Selectable Gain at 1×, 10× or 200×
  - Three Programmable Serial USART
  - Two Master/Slave SPI Serial Interface
  - Two Byte-oriented 2-wire Serial Interface (Philips I^2C Compatible)
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
  - Interrupt and Wake-up on Pin Change
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated Oscillator
  - External and Internal Interrupt Sources
  - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby, and Extended Standby
  - Clock Failure Detection Mechanism and Switch to 1MHz Internal RC Clock in case of Failure
  - Individual Serial Number to Represent a Unique ID
- I/O and Packages
  - 39 Programmable I/O Lines
  - 44-Pin TQFP and 44-Pin QFN/MLF
- Operating Voltage:
  - 1.8 - 5.5V
- Temperature Range:
  - -40°C to 105°C
- Speed Grade:
  - 0 - 4MHz @ 1.8 - 5.5V
  - 0 - 10MHz @ 2.7 - 5.5.V
  - 0 - 20MHz @ 4.5 - 5.5V
- Power Consumption at 1MHz, 1.8V, 25°C
  - Active Mode: 0.24mA
  - Power-Down Mode: 0.2µA
  - Power-Save Mode: 1.3µA (Including 32kHz RTC)

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1. Description

The Atmel® ATmega324PB is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega324PB achieves throughputs close to 1MIPS per MHz. This empowers system designer to optimize the device for power consumption versus processing speed.

The Atmel AVR® core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in a single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega324PB provides the following features: 32K bytes of In-System Programmable Flash with Read-While-Write capabilities, 1Kbytes EEPROM, 2Kbytes SRAM, 39 general purpose I/O lines, 32 general purpose working registers, *five* flexible Timer/Counters with compare modes, internal and external interrupts, three serial programmable USART, two byte-oriented 2-wire Serial Interface (I2C), two SPI serial port, a 8-channel 10-bit ADC with optional differential input stage with programmable gain, a programmable Watchdog Timer with internal Oscillator, IEEE std. 1149.1 compliant JTAG test interface, also used for accessing the On-chip Debug system and programming, Clock failure detection mechanism and six software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, USART, 2-wire Serial Interface, SPI port, and interrupt system to continue functioning. PTC with enabling up to 32 self-cap and 256 mutual-cap sensors. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or hardware reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. Also ability to run PTC in power-save mode/ wake-up on touch and Dynamic on/off of PTC analog and digital portion. The ADC Noise Reduction mode stops the CPU and all I/O modules except asynchronous timer, PTC, and ADC to minimize switching noise during ADC conversions. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low power consumption.

Atmel offers the QTouch® library for embedding capacitive touch buttons, sliders and wheels functionality into AVR microcontrollers. The patented charge-transfer signal acquisition offers robust sensing and includes fully debounced reporting of touch keys and includes Adjacent Key Suppression® (AKS®) technology for unambiguous detection of key events. The easy-to-use QTouch Composer allows you to explore, develop and debug your own touch applications.

The device is manufactured using Atmel's high density non-volatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed In-System through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program running on the AVR core. The Boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega324PB is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATmega324PB is supported with a full suite of program and system development tools including: C Compilers, Macro Assemblers, Program Debugger/Simulators, In-Circuit Emulators, and Evaluation kits.

2. Configuration Summary

Features	ATmega324PB
Pin count	44
Flash (KB)	32
SRAM (KB)	2
EEPROM (KB)	1
General Purpose I/O lines	39
SPI	2
TWI (I^2C)	2
USART	3
ADC	10-bit 15ksps
Differential ADC mode	Available
ADC channels	8
AC	1
8-bit Timer/Counters	2
16-bit Timer/Counters	3
PWM channels	10
PTC	Available
Peripheral Touch Controller (PTC) channels (X- x Y-Lines) for mutual capacitance	256 (16 x 16)
Peripheral Touch Controller (PTC) channels for self capacitance (Y-Lines only)	32
Clock Failure Detector (CFD)	Available
Output Compare Modulator (OCM1C2)	Available

3. Ordering Information

Speed [MHz]	Power Supply [V]	Ordering Code[2]	Package[1]	Operational Range
20	1.8 - 5.5	ATmega324PB-AU ATmega324PB-AUR[3] ATmega324PB-MU ATmega324PB-MUR[3]	44A 44A 44M1 44M1	Industrial (-40°C to 85°C)
		ATmega324PB-AN ATmega324PB-ANR[3] ATmega324PB-MN ATmega324PB-MNR[3]	44A 44A 44M1 44M1	Industrial (-40°C to 105°C)

Note: 1. This device can also be supplied in wafer form. Contact your local Atmel sales office for detailed ordering information and minimum quantities.

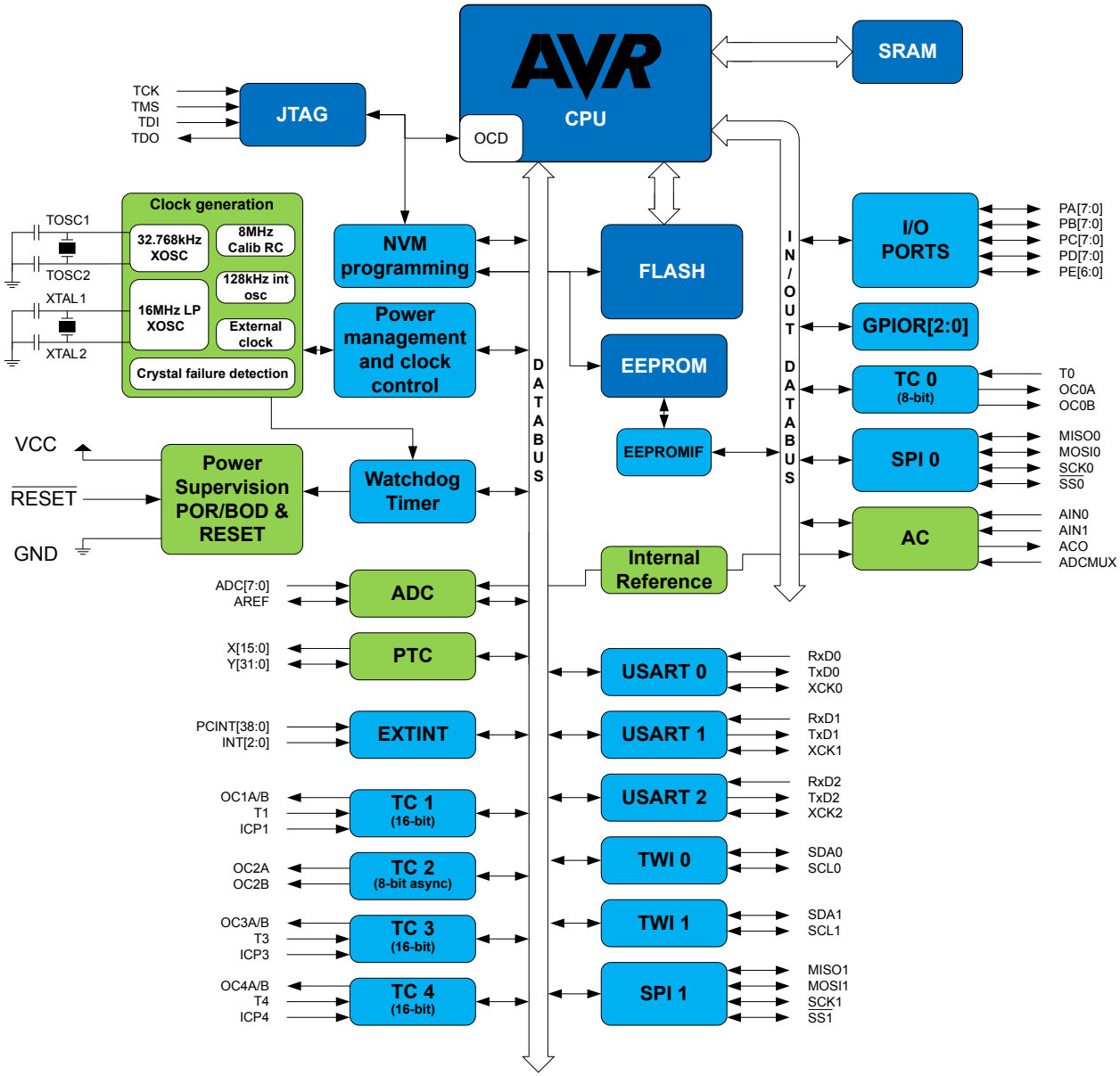
2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

3. Tape & Reel.

Package Type	
44A	44-lead, Thin (1.0mm) Plastic Quad Flat Package (TQFP)
44M1	44-pad, 7 x 7 x 0.9mm body, Lead Pitch 0.50mm, Very-thin Fine pitch, Quad Flat No Lead Package/Quad Flat No-Lead/Micro Lead Frame Package (VQFN/QFN/MLF)

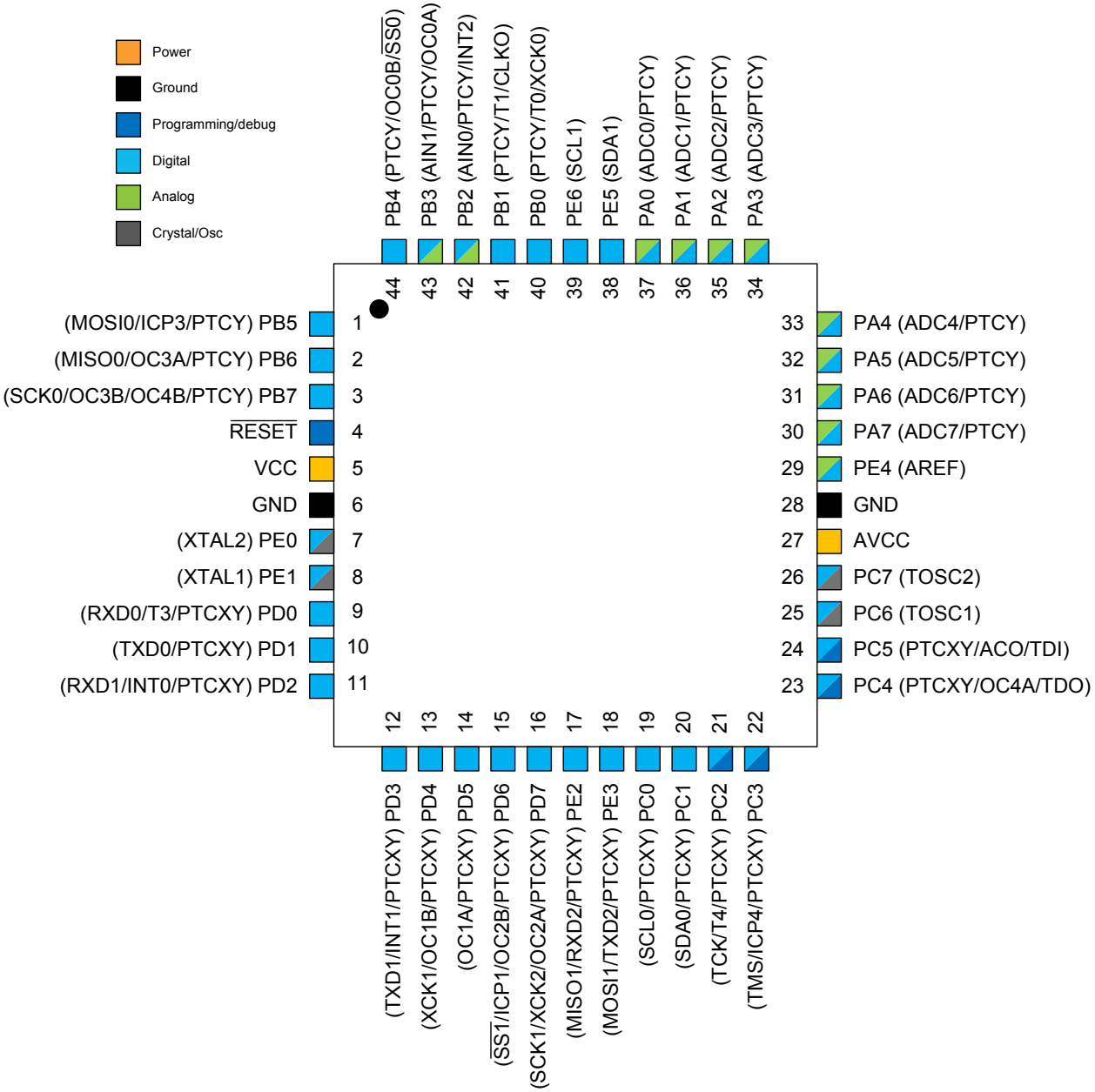
4. Block Diagram

Figure 4-1. Block Diagram



5. Pin Configurations

Figure 5-1. Pinout ATmega324PB



5.1. Pin Descriptions

5.1.1. VCC

Digital supply voltage.

5.1.2. GND

Ground.

5.1.3. Port A (PA[7:0])

This port serves as analog inputs to the Analog-to-digital Converter.

This is an 8-bit, bi-directional I/O port with internal pull-up resistors, individually selectable for each bit. The output buffers have symmetrical drive characteristics, with both high sink and source capability. As inputs, the port pins that are externally pulled low will source current if pull-up resistors are activated. Port pins are tri-stated when a reset condition becomes active, even if the clock is not running.

5.1.4. Port B (PB[7:0])

This is an 8-bit, bi-directional I/O port with internal pull-up resistors, individually selectable for each bit. The output buffers have symmetrical drive characteristics, with both high sink and source capability. As inputs, the port pins that are externally pulled low will source current if pull-up resistors are activated. Port pins are tri-stated when a reset condition becomes active, even if the clock is not running.

This port also serves the functions of various special features.

5.1.5. Port C (PC[7:0])

This is an 8-bit, bi-directional I/O port with internal pull-up resistors, individually selectable for each bit. The output buffers have symmetrical drive characteristics, with both high sink and source capability. As inputs, the port pins that are externally pulled low will source current if pull-up resistors are activated. Port pins are tri-stated when a reset condition becomes active, even if the clock is not running.

This port also serves the functions of the JTAG interface, along with special features.

5.1.6. Port D (PD[7:0])

This is an 8-bit, bi-directional I/O port with internal pull-up resistors, individually selectable for each bit. The output buffers have symmetrical drive characteristics, with both high sink and source capability. As inputs, the port pins that are externally pulled low will source current if pull-up resistors are activated. Port pins are tri-stated when a reset condition becomes active, even if the clock is not running.

This port also serves the functions of various special features.

5.1.7. Port E (PE6:0) XTAL1/XTAL2/AREF

This is a 7-bit bi-directional GPIO port with internal pull-up resistors (selected for each bit). The Port E output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port E pins that are externally pulled low will source current if the pull-up resistors are activated. The Port E pins are tri-stated when a reset condition becomes active, even if the clock is not running. PE0 and PE1 are multiplexed with XTAL1 and XTAL2 input. PE4 is multiplexed with AREF for the A/D Converter.

5.1.8. $\overline{\text{RESET}}$

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. Shorter pulses are not guaranteed to generate a reset.

5.1.9. AVCC

AVCC is the supply voltage pin for Port A, PE4 (AREF) and the Analog-to-digital Converter. It should be externally connected to V_{CC}, even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter.

6. I/O Multiplexing

Each pin is by default controlled by the PORT as a general purpose I/O and alternatively it can be assigned to one of the peripheral functions.

The following table describes the peripheral signals multiplexed to the PORT I/O pins.

Table 6-1. PORT Function Multiplexing

No.	PAD	EXTINT	PCINT	ADC/AC	PTC X	PTC Y	OSC	T/C # 0	T/C # 1	USART	I2C	SPI	JTAG
1	PB[5]		PCINT13			Y29		ICP3				MOSI0	
2	PB[6]		PCINT14			Y30		OC3A				MISO0	
3	PB[7]		PCINT15			Y31		OC3B	OC4B			SCK0	
4	$\overline{\text{RESET}}$												
5	VCC												
6	GND												
7	PE[0]		PCINT32				XTAL2						
8	PE[1]		PCINT33				XTAL1						
9	PD[0]		PCINT24		X0	Y8		T3		RxD0			
10	PD[1]		PCINT25		X1	Y9				TxD0			
11	PD[2]	INT0	PCINT26		X2	Y10				RxD1			
12	PD[3]	INT1	PCINT27		X3	Y11				TXD1			
13	PD[4]		PCINT28		X4	Y12			OC1B	XCK1			
14	PD[5]		PCINT29		X5	Y13			OC1A				
15	PD[6]		PCINT30		X6	Y14		OC2B	ICP1			$\overline{\text{SS1}}$	
16	PD[7]		PCINT31		X7	Y15		OC2A		XCK2		SCK1	
17	PE[2]				X8	Y16				RxD2		MISO1	
18	PE[3]				X9	Y17				TxD2		MOSI1	
19	PC[0]		PCINT16		X10	Y18					SCL0		
20	PC[1]		PCINT17		X11	Y19					SDA0		
21	PC[2]		PCINT18		X12	Y20			T4				TCK
22	PC[3]		PCINT19		X13	Y21			ICP4				TMS
23	PC[4]		PCINT20		X14	Y22			OC4A				TDO
24	PC[5]		PCINT21	ACO	X15	Y23							TDI
25	PC[6]		PCINT22				TOSC1						
26	PC[7]		PCINT23				TOSC2						
27	AVCC												
28	GND												
29	PE[4]			AREF									
30	PA[7]		PCINT7	ADC7		Y7							
31	PA[6]		PCINT6	ADC6		Y6							
32	PA[5]		PCINT5	ADC5		Y5							
33	PA[4]		PCINT4	ADC4		Y4							
34	PA[3]		PCINT3	ADC3		Y3							

No.	PAD	EXTINT	PCINT	ADC/AC	PTC X	PTC Y	OSC	T/C # 0	T/C # 1	USART	I2C	SPI	JTAG
35	PA[2]		PCINT2	ADC2		Y2							
36	PA[1]		PCINT1	ADC1		Y1							
37	PA[0]		PCINT0	ADC0		Y0							
38	PE[5]										SDA1		
39	PE[6]										SCL1		
40	PB[0]		PCINT8			Y24		T0		XCK0			
41	PB[1]		PCINT9			Y25	CLKO		T1				
42	PB[2]	INT2	PCINT10	AIN0		Y26							
43	PB[3]		PCINT11	AIN1		Y27		OC0A					
44	PB[4]		PCINT12			Y28		OC0B				$\overline{SS0}$	

7. General Information

7.1. Resources

A comprehensive set of development tools, application notes, and datasheets are available for download on http://www.atmel.com/avr.

7.2. Data Retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C.

7.3. About Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Confirm with the C compiler documentation for more details.

For I/O Registers located in extended I/O map, “IN”, “OUT”, “SBIS”, “SBIC”, “CBI”, and “SBI” instructions must be replaced with instructions that allow access to extended I/O. Typically “LDS” and “STS” combined with “SBRS”, “SBRC”, “SBR”, and “CBR”.

7.4. Capacitive Touch Sensing

7.4.1. QTouch Library

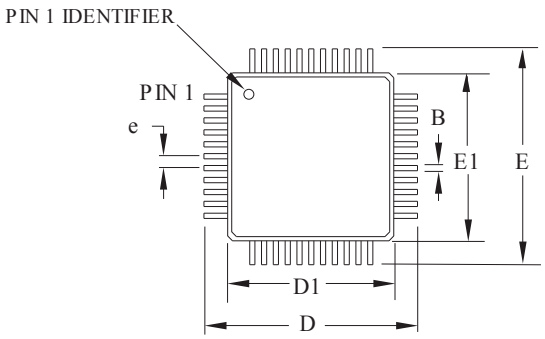
The Atmel® QTouch® Library provides a simple to use solution to realize touch sensitive interfaces on most Atmel AVR® microcontrollers. The QTouch Library includes support for the Atmel QTouch and Atmel QMatrix® acquisition methods.

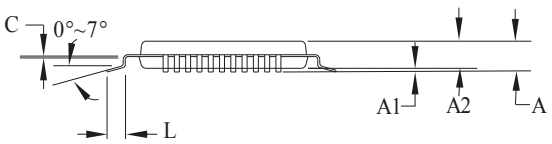
Touch sensing can be added to any application by linking the appropriate Atmel QTouch Library for the AVR Microcontroller. This is done by using a simple set of APIs to define the touch channels and sensors, and then calling the touch sensing API’s to retrieve the channel information and determine the touch sensor states.

The QTouch Library is FREE and downloadable from the Atmel website at the following location: http://www.atmel.com/technologies/touch/. For implementation details and other information, refer to the Atmel QTouch Library User Guide - also available for download from the Atmel website.

8. Packaging Information

8.1. 44-pin TQFP





COMMON DIMENSIONS
(Unit of Measure = mm)

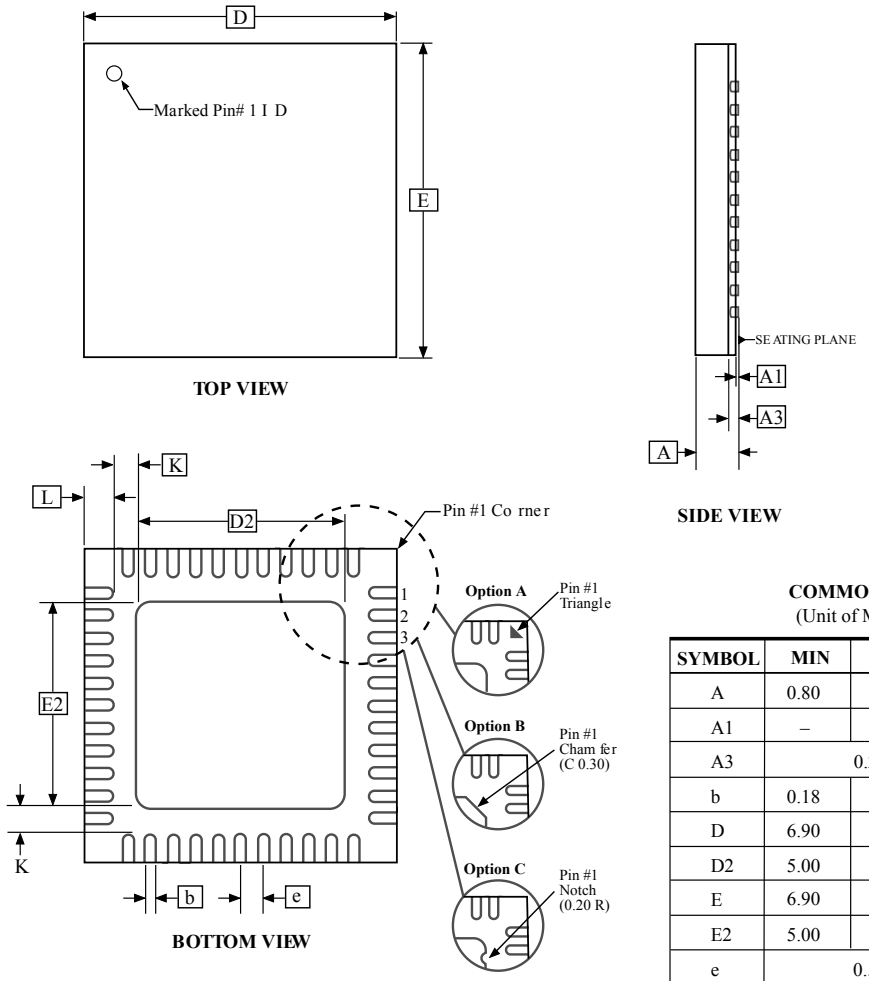
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	0.37	0.45	
C	0.09	(0.17)	0.20	
L	0.45	0.60	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

06/02/2014

	TITLE	DRAWING NO.	REV.
Atmel Package Drawing Contact: packagedrawings@atmel.com	**44A,** 44-lead, 10 x 10mm body size, 1.0mm body thickness, 0.8 mm lead pitch, thin profile plastic quad flat package (TQFP)	44A	C

8.2. 44-pin VQFN



Note : JEDEC Standard MO-220, Fig . 1 (S AW Singulation) VKKD-3 .

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	–	0.02	0.05	
A3		0.20 REF		
b	0.18	0.23	0.30	
D	6.90	7.00	7.10	
D2	5.00	5.20	5.40	
E	6.90	7.00	7.10	
E2	5.00	5.20	5.40	
e		0.50 BSC		
L	0.59	0.64	0.69	
K	0.20	0.26	0.41	

9/26/08

Package Drawing Contact: avr@atmel.com	TITLE	GPC	DRAWING NO.	REV.
	44M1, 44-pad, 7 x 7 x 1.0mm body, lead pitch 0.50mm, 5.20mm exposed pad, thermally enhanced plastic very thin quad flat no lead package (VQFN)	ZWS	44M1	H

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Atmel Corporation 1600 Technology Drive, San Jose, CA 95110 USA **T:** (+1)(408) 441.0311 **F:** (+1)(408) 436.4200 | **www.atmel.com**

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