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Atmel ATPL00B

FSK Power Line Communications SoC

DATASHEET

Features

- Core
  - ADD8051C3A enhanced 8051 core
  - Speedups up to x5 vs. standard 8051 microcontroller
- 128Kbytes internal SRAM
- In-circuit serial flash programming
- Auto boot-loading program from serial flash
- Media Access Control
  - Convolutional and block (FEC) channel coding, Viterbi decoding
  - Hardware CRC error detection and FEC error correction
  - By-pass mode to support earlier no-MAC FSK modem software
- Modem
  - Power Line Carrier Modem for 50 and 60 Hz mains
  - Carrier Frequency: 132.5KHz
  - Baud rate Selectable: 600 to 4800 bps
  - Half Duplex communication
  - Receiver Sensitivity: Up to 44dBµVrms
- Peripherals
  - Three 2-wire UARTs
  - Two SPI. SPI to serial flash and External RTC. Buffered SPI to external metering IC
  - Programmable Watchdog
  - Quad dimmer in/out
  - Up to 20 I/O lines
- Package
  - 144-lead LQFP, 16 x 16 mm, pitch 0.4 mm
  - Pb-free and RoHS compliant
- Typical Applications
  - Automated Meter Reading (AMR) & Advanced Meter Management (AMM)
  - Street lighting
  - Home Automation

Description

The ATPL00B is a Power Line Communications System on Chip that implements a full PLC node using FSK modulations and includes a hardwired Medium Access Controller (ADD1210). It has been developed to reduce the CPU computational load in PLC systems. Thus, the microcontroller is free to be used in the applications tasks.

MAC functional capabilities of ATPL00B (performed in ADD1210 Medium Access Controller) involve the construction of message packets, adding convolutional or FEC (Forward Error Correction) codes to bytes and FCS (Frame Check Sequence) to packets. In reception, the MAC provides frame detection and Viterbi decoding or FCS and FEC correction.

ATPL00B MAC design is versatile and allows users to create a wide range of datagram structures. The MAC shall be set in a bypass mode allowing direct connection between the microcontroller and the modem to support old FSK software that doesn't include the MAC.

ATPL00B PLC modem (ADD1310) is based on a Frequency-shift keying (FSK) Modulation Scheme supporting Minimum Shift Frequency (MSK) in the C-Band with carrier frequency of 132,5KHz. It shall work using a single power supply of 3.3V and a few external components, supporting several Analog Front End (AFE) configurations suitable for Home Automation purposes. It shall replace the traditional analog PLC modem and can use the same software libraries or a simplified version if the hardwired MAC is used. The PLC modem fits CENELEC C-band and EN50065-1 access rules, and has receiver sensitivity up to 44dBµVrms (158 µVrms).

ATPL00B core (ADD8051C3A) includes all features of the standard 8051, with an average speed up to x5 and some additional features.

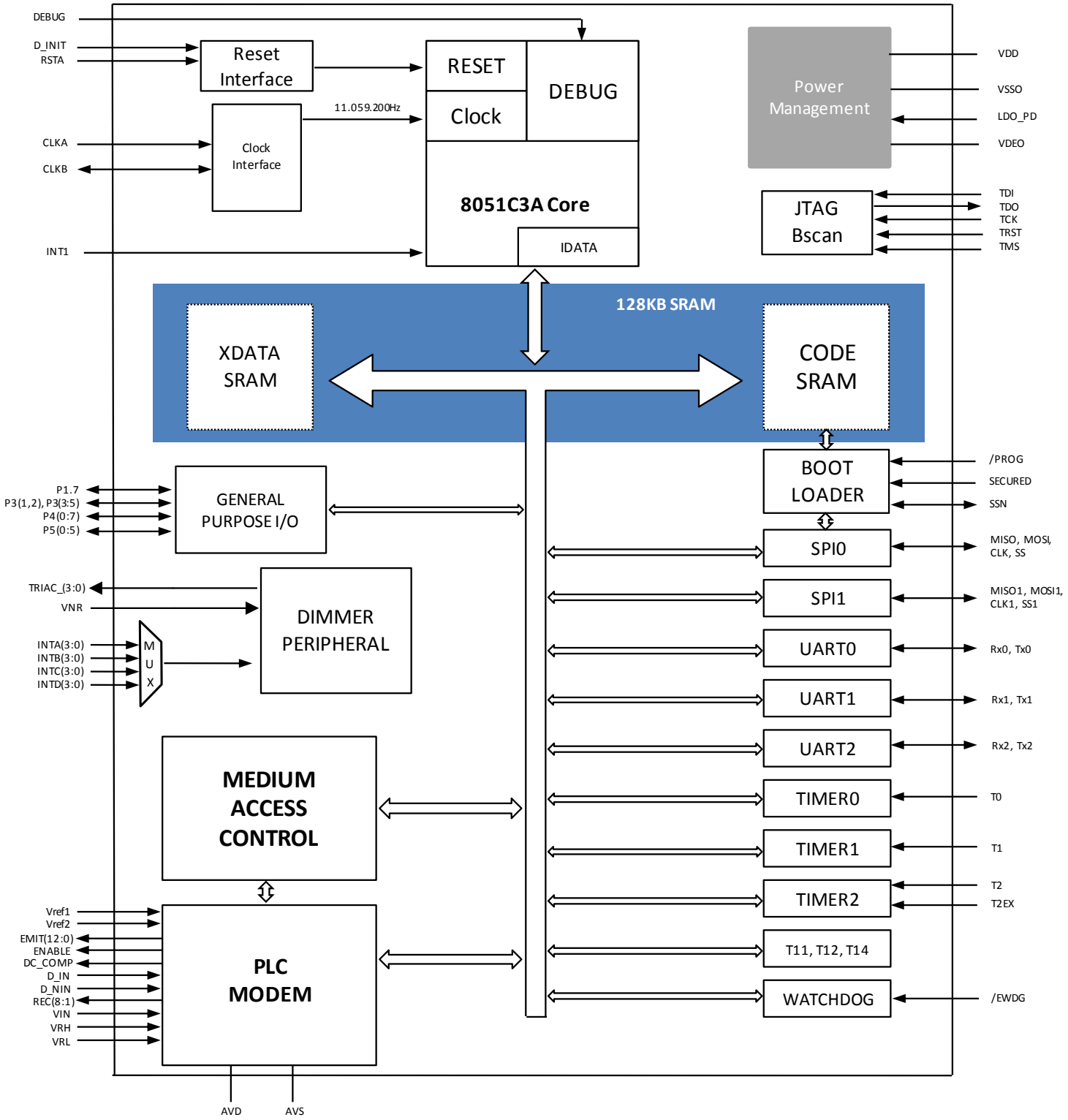
The microcontroller includes some specific peripherals as 4 input / 4 output dimmers for power regulation (phase angle control), and also capable of generating Pulse-Width Modulation (PWM) control.

A flash program loader allows downloading the microcontroller program in a standard SPI serial flash memory and executing it from internal SRAM. In the start-up process, the program is uploaded from serial flash to the internal 128Kbytes of SRAM before starting the execution. After that, the free space in the serial flash shall be used to store application data. ATPL00B includes an encryption engine for code protection. Using a larger flash, several programs may be stored at the same time and the microcontroller shall switch from one program to another. This feature could be used to reprogram the SoC using PLC downloading.

Table of Contents

1. Block Diagram

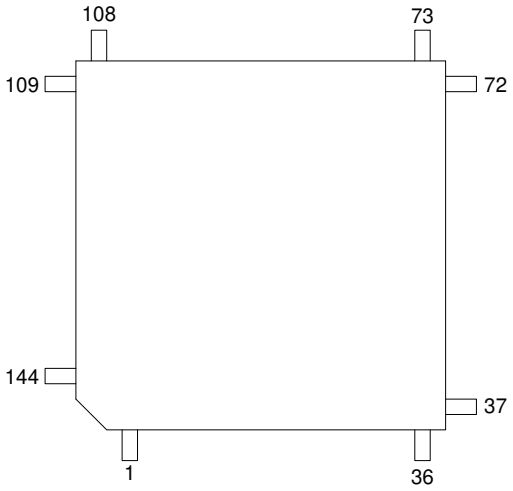
Figure 1-1. ATPL00B 144-pin Block Diagram



2. Package and Pinout

2.1 144-Lead LQFP Package Outline

Figure 2-1. Orientation of the 144-Lead Package



2.2 144-Lead LQFP Pinout

Table 2-1. **ATPL00B 144-Lead LQFP pinout**

PinNo	Pin Name	I/O	I(mA)	Res	HY
1	P3_3/INT1	I/O	±5	PU	-
2	VCC	P	-	-	-
3	GND	P	-	-	-
4	GND	P	-	-	-
5	GND	P	-	-	-
6	TDI	I	±5	PU	-
7	TDO	O	±5	-	-
8	TCK	I	±5	-	-
9	TMS	I	±5	PU	-
10	TRST	I	±5	PU	-
11	D_INIT	I	±5	PD	Y
12	RSTA	I	±5	PD	Y
13	/PROG	I	±5	PU	Y
14	SECURED	I	±5	PD	Y
15	/EWDG	I	±5	PD	Y
16	DEBUG	I	±5	PD	Y
17	VCC	P	-	-	-
18	CLKEB	I/O	-	-	-
19	GND	P	-	-	-
20	CLKEA	I	-	-	-
21	VCC	P	-	-	-
22	GND	P	-	-	-
23	GND	P	-	-	-
24	VDE0	P	-	-	-
25	VDE0	P	-	-	-
26	VSS0	P	-	-	-
27	LDO_PD	I			
28	VDD	P	-	-	-
29	GND	P	-	-	-
30	VCC	P	-	-	-
31	Vref1	I	-	-	-
32	Vref2	I	-	-	-
33	VNR	I	±5	-	Y
34	TRIAC_3	O	±5	-	-
35	TRIAC_2	O	±5	-	-
36	TRIAC_1	O	±5	-	-
37	TRIAC_0	O	±5	-	-
38	P5_5/TXD1/INTA1	I/O	±5	PU	-
39	P5_4/RXD1/INTA0	I/O	±5	PU	-
40	P4_7/T2EX/INTA3	I/O	±5	PU	-
41	P4_6/T2/INTA2	I/O	±5	PU	-
42	P1_7/SSN	I/O	±5	PU	-
43	VCC	P	-	-	-
44	GND	P	-	-	-
45	EMIT_0	O	±X	-	-
46	EMIT_1	O	±X	-	-
47	EMIT_2	O	±X	-	-
48	VCC	P	-	-	-
49	GND	P	-	-	-
50	EMIT_3	O	±X	-	-
51	EMIT_4	O	±X	-	-
52	EMIT_5	O	±X	-	-
53	EMIT_6	O	±X	-	-
54	VCC	P	-	-	-
55	GND	P	-	-	-
56	EMIT_7	O	±X	-	-
57	EMIT_8	O	±X	-	-
58	EMIT_9	O	±X	-	-
59	EMIT_10	O	±X	-	-
60	VCC	P	-	-	-
61	GND	P	-	-	-
62	EMIT_11	O	±X	-	-
63	EMIT_12	O	±X	-	-
64	VCC	P	-	-	-
65	GND	P	-	-	-
66	P3_1/TXD0	I/O	±5	PU	-
67	P3_0/RXD0	I/O	±5	PU	-
68	P4_5/MISO1/INTB3	I/O	±5	PU	-
69	P4_4/MOSI1/INTB2	I/O	±5	PU	-
70	P4_3/SPICLK1/INTB1	I/O	±5	PU	-
71	P4_2/SS1/INTB0	I/O	±5	PU	-
72	P4_1/TXD2	I/O	±5	PU	-
73	P4_0/RXD2	I/O	±5	PU	-
74	VCC	P	-	-	-
75	GND	P	-	-	-
76	INTC3	I	±5	-	-

Table 2-1. **ATPL00B 144-Lead LQFP pinout (Continued)**

PinNo	Pin Name	I/O	I(mA)	Res	HY
77	INTC2	I	±5	-	-
78	INTC1	I	±5	-	-
79	INTC0	I	±5	-	-
80	NC	-	-	-	-
81	NC	-	-	-	-
82	NC	-	-	-	-
83	NC	-	-	-	-
84	NC	-	-	-	-
85	NC	-	-	-	-
86	NC	-	-	-	-
87	NC	-	-	-	-
88	NC	-	-	-	-
89	VDD	P	-	-	-
90	VCC	P	-	-	-
91	GND	P	-	-	-
92	NC	-	-	-	-
93	NC	-	-	-	-
94	NC	-	-	-	-
95	NC	-	-	-	-
96	NC	-	-	-	-
97	NC	-	-	-	-
98	NC	-	-	-	-
99	NC	-	-	-	-
100	NC	-	-	-	-
101	NC	-	-	-	-
102	NC	-	-	-	-
103	VCC	P	-	-	-
104	GND	P	-	-	-
105	INTD3	I	±5	-	-
106	INTD2	I	±5	-	-
107	INTD1	I	±5	-	-
108	INTD0	I	±5	-	-
109	NC	-	-	-	-
110	NC	-	-	-	-
111	NC	-	-	-	-
112	NC	-	-	-	-
113	GND	P	-	-	-
114	DC_COMP	O	±10	-	-
115	VCC	P	-	-	-
116	ENABLE	O	±10	-	-
117	GND	P	-	-	-
118	DNIN	I	±5	-	-
119	DIN	I	±5	-	-
120	REC_1	O	±5	-	-
121	REC_2	O	±5	-	-
122	REC_3	O	±5	-	-
123	REC_4	O	±5	-	-
124	REC_5	O	±5	-	-
125	REC_6	O	±5	-	-
126	REC_7	O	±5	-	-
127	REC_8	O	±5	-	-
128	VCC	P	-	-	-
129	GND	P	-	-	-
130	VRL	I	(**)	-	-
131	VIN	I	(**)	-	-
132	VRH	I	(**)	-	-
133	AVD1	P	-	-	-
134	AVS1	P	-	-	-
135	AVD2	P	-	-	-
136	AVS2	P	-	-	-
137	VCC	P	-	-	-
138	GND	P	-	-	-
139	P5_3/MISO0	I/O	±5	PU	-
140	P5_2/MOSI0	I/O	±5	PU	-
141	P5_1/SPICLK0	I/O	±5	PU	-
142	P5_0/SS0	I/O	±5	PU	-
143	P3_5/T1	I/O	±5	PU	-
144	P3_4/T0	I/O	±5	PU	-

Notes: 1. Mandatory to be tied down

I/O=pin direction: **I**=input, **O**=Output, **P**=Power

I(mA)=nominal current: **+**=source, **-**=sink, **X**=fixed by external resistor

RES=pin pullup/pulldown resistor: **PU**=pullup, **PD**=pulldown ; **HY**=Input Hysteresis

3. Pin Description

Table 3-1. **Pin Description List**

Pin Number	Pin Name	Type	Comments
1	P3.3/INT1	I/O	Microcontroller port 3.3 / External Interrupt 1 • When configured as P3.3, this pin is a pseudo-bidirectional microcontroller I/O port • When configured as INT1, this pin is the 8051C3A microcontroller external interrupt 1 • Internal configuration: 33kΩ typ. pull-up resistor
2, 17, 21, 30, 43, 48, 54, 60, 64, 74, 90, 103, 115, 128, 137	VCC	Power	3.3v digital supply. Digital power supply must be decoupled by external capacitors
3, 4, 5, 19, 22, 23, 29, 44, 49, 55, 61, 65, 75, 91, 104, 113, 117, 129, 138	GND	Power	Digital ground
6	TDI(1)	Input	Test Data In • Internal configuration: 33kΩ typ. pull-up resistor
7	TDO(1)	Output	Test Data out
8	TCK(1)	Input	Test Clock
9	TMS(1)	Input	Test Mode Select • Internal configuration: 33kΩ typ. pull-up resistor
10	TRST(1)	Input	Test Reset • Internal configuration: 33kΩ typ. pull-up resistor
11	D_INIT	Input	Initialization Signal • During power-on, D_INIT should be released before asynchronous reset signal RSTA, in order to ensure proper system start up. Not minimum time is required between both releases, $\Delta t>0$ • D_INIT is active high • Internal configuration: 33kΩ typ. pull-down resistor
12	RSTA	Input	Asynchronous reset • RSTA is a digital input pin used to perform a hardware reset of the ASIC • RSTA is active high • Internal configuration: 33kΩ typ. pull-down resistor

13	/PROG	Input	SPI Flash programming pin
			• /PROG digital input is read during power up and sets the system into “execution” mode or “serial flash programming” mode
			  ◦ ‘0’: Serial flash programming mode
			  ◦ ‘1’: Execution mode (normal mode)
			Internal configuration: 33kΩ typ. pull-up resistor

Table 3-1. **Pin Description List (Continued)**

Pin Number	Pin Name	Type	Comments

14	SECURED	Input	Encryption enable
			• SECURED digital input enables encrypted firmware storage and execution when the board configuration supports it
			  • '0': Encrypted storage/execution disabled
			  • '1': Encrypted storage/execution enabled
			• Internal configuration: 33kΩ typ. pull-down resistor

15	/EWDG	Input	Watchdog enable
			• /EWDG digital input enables watchdog timer. This pin is internally connected to the /EW signal of the ADD8051C3A microcontroller
			  • '0': Watchdog timer enabled
			  • '1': Watchdog timer disabled
			• Internal configuration: 33kΩ typ. pull-down resistor

16	DEBUG	Input	Debug mode enable
			• DEBUG digital input is internally connected to DBG signal of the ADD8051C3A microcontroller, and it is intended to implement software debugging tools
			  • '0': Debug mode disabled
			  • '1': Debug mode enabled
			• Internal configuration: 33kΩ typ. pull-down resistor

18	CLKEB[2]	I/O	External clock reference • CLKEB must be connected to one terminal of a crystal (when a crystal is being used) or to one terminal of a compatible oscillator (when a compatible oscillator is being used)
20	CLKEA[2]	Input	External clock reference • CLKEA must be connected to one terminal of a crystal (when a crystal is being used) or tied to ground if a compatible oscillator is being used
24, 25	VDEO	Power	LDO 3.3v power supply
26	VSSO	Power	LDO ground
27	LDO_PD	Power	LDO Power-down. This digital input is used to put the internal linear regulator into power down mode • '0': Power down mode disabled '1': Power down mode enabled
28,89	VDD	Power	LDO Power output A capacitor in the range 0.1µF - 10µF must be connected to each pin
31	Vref1	Input	Voltage reference 1. Tie to Vcc with a Rpu = 4.7kΩ
32	Vref2	Input	Voltage reference 2. Tie to GND with a Rpd = 4.7kΩ
33	VNR	Input	Zero-crossing detection signal • This input detects the zero-crossing of the mains voltage, needed to properly determine switching times • Depending on whether an isolated or a non-isolated power supply is being used, isolation of this pin should be taken into account in the circuitry design

Table 3-1. **Pin Description List (Continued)**

Pin Number	Pin Name	Type	Comments
34, 35, 36, 37	TRIAC(3:0)	Output	TRIAC outputs • These four pins are outputs to control home automation devices by the ATPL00B dimmer peripheral. TRIAC outputs can be configured to work as phase angle controllers or as PWM controllers
38	P5.5/TxD1/INTA1	I/O	Microcontroller port 5.5 / Standard Serial Port 1 Tx / Dimmer switch 1 • When configured as P5.5, this pin is a pseudo-bidirectional microcontroller I/O port • When configured as TxD1, this pin is the digital output of the asynchronous standard serial port 1 • When configured as INTA1, this pin is the input to dimmer peripheral signal INTERR(1) • Internal configuration: 33kΩ typ. pull-up resistor
39	P5.4/RxD1/INTA0	I/O	Microcontroller port 5.4 / Standard Serial Port 1 Rx / Dimmer switch 0 • When configured as P5.4, this pin is a pseudo-bidirectional microcontroller I/O port • When configured as RxD1, this pin is the digital input of the asynchronous standard serial port 1 • When configured as INTA0, this pin is the input to dimmer peripheral signal INTERR(0) • Internal configuration: 33kΩ typ. pull-up resistor
40	P4.7/T2EX/INTA3	I/O	Microcontroller port 4.7 / T2EX / Dimmer switch 3 • When configured as P4.7, this pin is a pseudo-bidirectional microcontroller I/O port • When configured as T2EX, this pin is the Timer/Counter 2 capture/reload trigger described in Timer2 section • When configured as INTA3, this pin is the input to dimmer peripheral signal INTERR(3) • Internal configuration: 33kΩ typ. pull-up resistor
41	P4.6/T2/INTA2	I/O	Microcontroller port 4.6 / T2 / Dimmer switch 2 • When configured as P4.6, this pin is a pseudo-bidirectional microcontroller I/O port • When configured as T2, this pin works as the external T2 pin described in Timer2 section • When configured as INTA2, this pin is the input to dimmer peripheral signal INTERR(2) • Internal configuration: 33kΩ typ. pull-up resistor
42	P1.7/SSN	I/O	Microcontroller port 1.7 / Silicon Serial Number • When configured as P1.7, this pin is a pseudo-bidirectional microcontroller I/O port • This pin is the digital input used to read a Serial number if a valid SSN device is being used. This Serial Number is used for encryption purposes. Precaution should be taken if used as generic control port since it searches for a Silicon Serial Number device at start-up and could put out undesirable transient values • Internal configuration: 33kΩ typ. pull-up resistor

Table 3-1. **Pin Description List (Continued)**

Pin Number	Pin Name	Type	Comments
45	EMIT.0	Output	Tx/Rx control output pin • This output pin is used by the system to adapt the external Analog-Front-end either in transmission or in reception, thus improving the electrical behavior
46, 47, 50, 51, 52, 53, 56, 57, 58, 59, 62, 63	EMIT(1:12)	Output	PLC transmission ports[3]
66	P3.1/TxD0	I/O	Microcontroller port 3.1 / Standard Serial Port 0 Tx • When configured as P3.1, this pin is a pseudo-bidirectional microcontroller I/O port • When configured as TxD0, this pin is the digital output of the asynchronous standard serial port 0 • Internal configuration: 33kΩ typ. pull-up resistor
67	P3.0/RxD0	I/O	Microcontroller port 3.0 / Standard Serial Port 0 Rx • When configured as P3.0, this pin is a pseudo-bidirectional microcontroller I/O port • When configured as RxD0, this pin is the digital input of the asynchronous standard serial port 0 • Internal configuration: 33kΩ typ. pull-up resistor
68	P4.5/MISO1/INTB3	I/O	Microcontroller port 4.5 / SPI1 Master In Slave Out / Dimmer switch 3 • When configured as P4.5, this pin is a pseudo-bidirectional microcontroller I/O port • When configured as MISO1, this pin is the SPI1 Master In Slave Out • When configured as INTB3, this pin is the input to dimmer peripheral signal INTERR(3) • Internal configuration: 33kΩ typ. pull-up resistor
69	P4.4/MOSI1/INTB2	I/O	Microcontroller port 4.4 / SPI1 Master Out Slave In / Dimmer switch 2 • When configured as P4.2, this pin is a pseudo-bidirectional microcontroller I/O port • When configured as MOSI1, this pin is the SPI1 Master Out Slave In • When configured as INTB2, this pin is the input to dimmer peripheral signal INTERR(2) • Internal configuration: 33kΩ typ. pull-up resistor
70	P4.3/SPICLK1/INTB1	I/O	Microcontroller port 4.3 / SPI1 Clock / Dimmer switch1 • When configured as P4.3, this pin is a pseudo-bidirectional microcontroller I/O port • When configured as SPICLK1, this pin is the SPI1 clock signal • When configured as INTB1, this pin is the input to dimmer peripheral signal INTERR(1) • Internal configuration: 33kΩ typ. pull-up resistor

Table 3-1. **Pin Description List (Continued)**

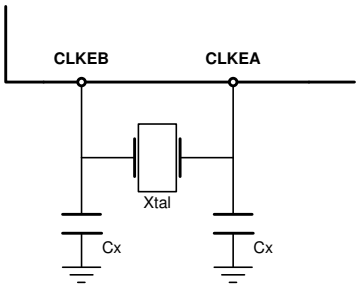
Pin Number	Pin Name	Type	Comments
71	P4.2/SS1/INTB0	I/O	Microcontroller port 4.2 / SPI1 Slave Select / Dimmer switch 0 • When configured as P4.2, this pin is a pseudo-bidirectional microcontroller I/O port • When configured as SS1, this pin is the SPI1 Slave Select. Active low • When configured as INTB0, this pin is the input to dimmer peripheral signal INTERR(0) • Internal configuration: 33kΩ typ. pull-up resistor
73	P4.0/RxD2	I/O	Microcontroller port 4.0 / Standard Serial Port 2 Rx • When configured as P4.0, this pin is a pseudo-bidirectional microcontroller I/O port • When configured as RxD2, this pin is the digital input of the asynchronous standard serial port 2 • Internal configuration: 33kΩ typ. pull-up resistor
76, 77, 78, 79	INTC(3:0)	I/O	Dimmer switches • • These pins can be configured as inputs to dimmer peripheral signals INTERR(3:0)
80, 81, 82, 83, 84, 85, 86, 87, 88, 92, 93, 94, 95, 96, 97, 98, 99, 100, 101, 102, 109, 110, 111, 112	NC	-	No Connect
105, 106, 107, 108	INTD(3:0)	I/O	Dimmer switches • • These pins can be configured as inputs to dimmer peripheral signals INTERR(3:0)
114	DC_COMP	Output	External comparator DC compensation • This output controls the direct current compensation of the external comparator. This pin is connected only if an external comparator is being used. Otherwise, this pin must be left unconnected
116	ENABLE	Output	External comparator enable • Output pin to enable external comparator. This pin is connected only if an external comparator is being used. Otherwise, this pin must be left unconnected
118	DNIN	Input	External comparator inverted output signal • This pin is the input for the external comparator inverted output signal. This pin is connected only if an external comparator is being used. Otherwise, this pin must be tied to ground
119	DIN	Input	External comparator output signal • This pin is the input for the external comparator output signal. This pin is connected only if an external comparator is being used. Otherwise, this pin must be tied to ground

Table 3-1. **Pin Description List (Continued)**

Pin Number	Pin Name	Type	Comments
120, 121, 122, 123, 124, 125, 126, 127	REC(1:8)	Output	External comparator threshold loop • These outputs are used to set the voltage threshold in the external comparator. These pins are connected only if an external comparator is being used. Otherwise, these pins must be left unconnected
130	VRL	Input	Analog input low voltage reference
131	VIN	Input	Direct-analog input voltage
132	VRH	Input	Analog input high voltage reference
133, 135	AVD1, AVD2	Power	3.3v analog power
134, 136	AVS1, AVS2	Power	Analog ground
139	P5.3/MISO0	I/O	Microcontroller port 5.3 / SPI0 Master In Slave Out • When configured as P5.3, this pin is a pseudo-bidirectional microcontroller I/O port • When configured as MISO0, this pin is the SPI0 Master In Slave Out • Internal configuration: 33kΩ typ. pull-up resistor
140	P5.2/MOSI0	I/O	Microcontroller port 5.2 / SPI0 Master Out Slave In • When configured as P5.2, this pin is a pseudo-bidirectional microcontroller I/O port • When configured as MOSI0, this pin is the SPI0 Master Out Slave In • Internal configuration: 33kΩ typ. pull-up resistor
141	P5.1/SPICLK0	I/O	Microcontroller port 5.1 / SPI0 Clock • When configured as 54.1, this pin is a pseudo-bidirectional microcontroller I/O port • When configured as SPICLK0, this pin is the SPI0 clock signal • Internal configuration: 33kΩ typ. pull-up resistor
142	P5.0/SS0	I/O	Microcontroller port 5.0 / SPI0 Slave Select • When configured as P5.0, this pin is a pseudo-bidirectional microcontroller I/O port • When configured as SS0, this pin is the SPI0 Slave Select. Active low • Internal configuration: 33kΩ typ. pull-up resistor
143	P3.5/T1	I/O	Microcontroller port 3.5 / Timer 1 interrupt signal • When configured as P3.5, this pin is a pseudo-bidirectional microcontroller I/O port • When configured as T1, this pin works as the external T1 pin described in Timer1 section • Internal configuration: 33kΩ typ. pull-up resistor
144	P3.4/T0	I/O	Microcontroller port 3.4 / Timer 0 interrupt signal • When configured as P3.4, this pin is a pseudo-bidirectional microcontroller I/O port • When configured as T0, this pin works as the external T0 pin described in Timer0 section • Internal configuration: 33kΩ typ. pull-up resistor

Notes: 1. This pin is part of the JTAG Boundary Scan interface and is only used for boundary scan purposes

2. The crystal should be located as close as possible to CLKEA and CLKEB pins. Recommended value for Cx is 18pF. This value may depend on the specific crystal characteristics



Different configurations allowed depending on external topology and net behavior

4. Processor and Architecture

4.1 ADD8051C3A Microcontroller Description

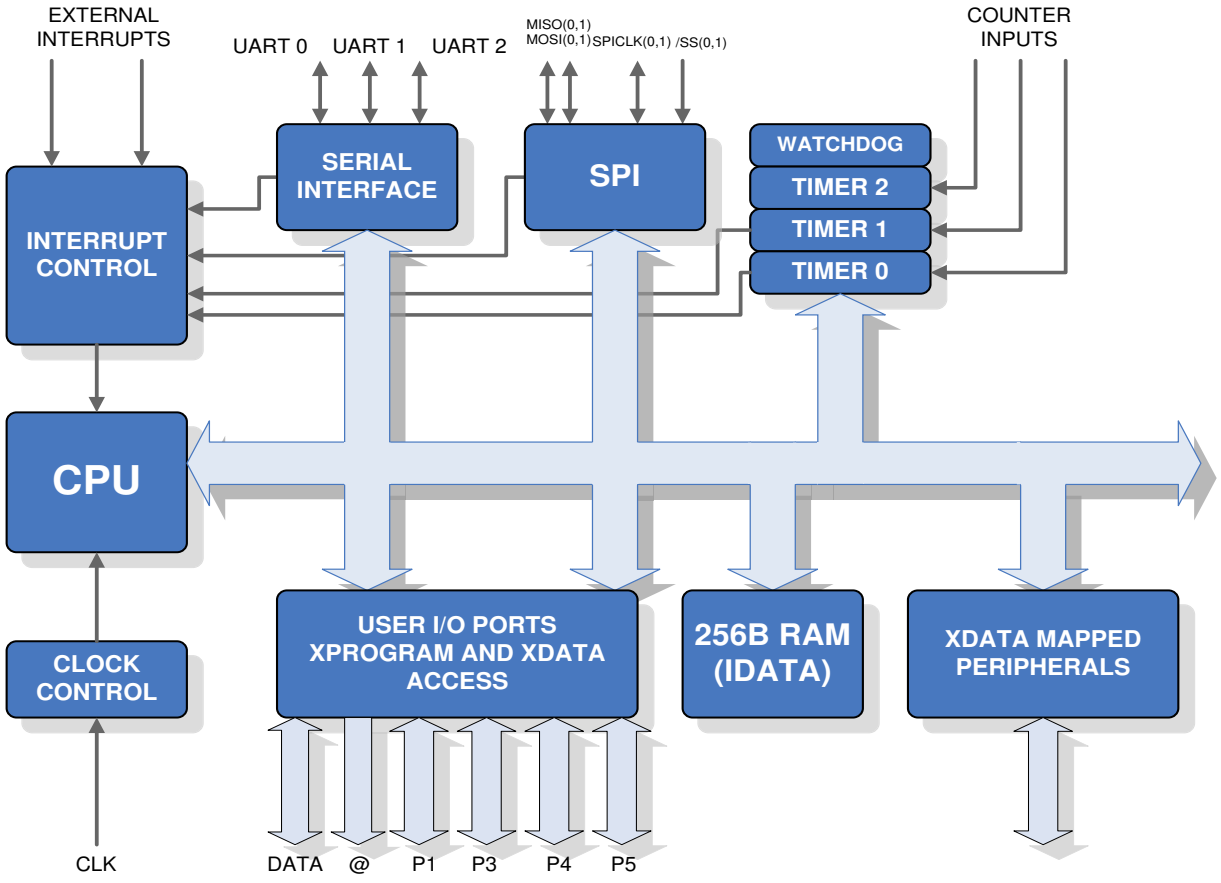
The following document provides a detailed description of the ADD8051C3A architecture and its hardware. ADD8051C3A is fully compatible with any 8051 legacy microcontroller, however there are some hardware differences that deserve to be taken into account.

CPU speed has been improved. The machine cycle has been reduced from 12 to 3 clock cycles, and all the instructions are executed in 1 or 2 machine cycles. Programs are executed a minimum of four times faster than in a standard-8051-architecture device, achieving x5 speedup for most programs.

A 128KBytes SRAM is embedded on chip. Program memory and External Data (XDATA) memory share this 128Kbytes SRAM. The lower 64Kbytes are always dedicated to store program memory, while upper 64Kbytes are configurable to allocate different program and XDATA memory size configurations, depending on bank switching page size (See 4.3).

This document includes a detailed description of registers and peripherals. Some of these items are upgraded versions of the original 8051 microcontroller circuitry, while others are a simplified version.

Figure 4-1. ADD8051C3A microcontroller block diagram



Note: This chapter describes the architecture from the microcontroller point of view. Thus, “on-chip SRAM” is referred to as “external memory” since “external” instructions like MOVX are necessary to access this memory device

4.2 Core Pinout Description

Figure 4-2. ADD8051C3A core pinout diagram

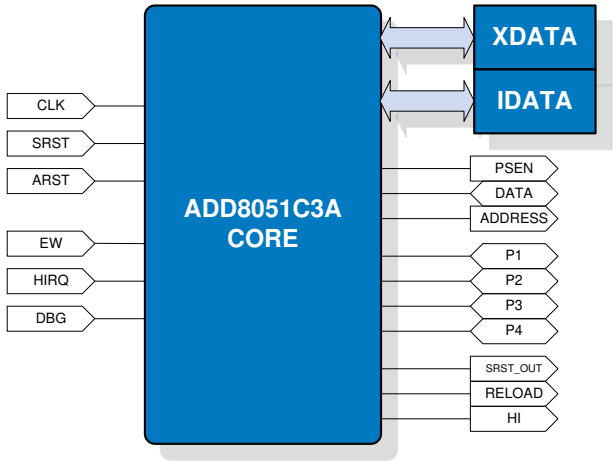


Table 4-1. **Core pinout description**

Pin	I/O	Description
CLK	I	Clock input.
ARST	I	Asynchronous reset.
SRST	I	SRST Must be held active one clock cycle to ensure proper power-on. External signal D_INIT is connected to this core input.
/EW	I	Watchdog enable Low level active. External signal/EWDG is connected to this core input.
HIRQ	I	Hard idle request High level active. When asserted, the microcontroller finishes the instruction in execution and goes to a special hard idle state. In hard idle state the CPU is stopped while peripheral circuits still run, CPU restarts only after HIRQ deassertion.
DBG	I	Debug mode enable High level active.
PSEN	O	Program Store Enable Read strobe to program memory.
DATA	I/O	Data bus 16-bit bidirectional port to access program and/or data memories.
ADDRESS	O	Address bus Output port to access program memory and XDATA.
SRST_OUT	O	Watchdog timer reset signal.
RELOAD	O	Program reload control signal Software or watchdog activated. Force program reload from a serial storage device to a parallel SRAM.
HI	O	Hard idle flag, This flag is set to ‘1’ when the CPU is in hard idle state.

PORTS: P1, P3, P4, P5 (*)	I/O	I/O Ports. 8-bit pseudo bidirectional I/O ports with pull-up resistors. These ports are by default in **pseudo-bidirectional** configuration. Configured in this way, port pins that have 1s written to them are pulled high by the internal pull-ups, and in that state can be used as inputs. When a bit in a Port register has a 0 to 1 transition the related pin is driven high using transistor during 1 clock cycle, then the transistor is switched off and the pull-up resistor keeps the logic level. Ports P3, P4 and P5 can be also configured as **push-pull** mode ports. In push-pull mode the pin is always in output mode and logic 1 is always high driven (see 4.7.1). Some pins of P3, P4 and P5 also serve the functions of various special features of the microcontroller: P3.0 → RxD (serial port 0 input) P3.1 → TxD (serial port 0 output) P3.2 → INT0 (external interrupt 0) P3.3 → INT1 (external interrupt 1) P3.4 → T0 (timer 0 external input) P3.5 → T1 (timer 1 external input) P3.6 → WR(external data memory write strobe) P3.7 → RD (external data memory read strobe) P4.0 → RxD (serial port 2 input) P4.1 → TxD (serial port 2 output) P4.2 → SS1 (slave select input) P4.3 → SPICLK1 (SPI1 clock input/output) P4.4 → MOSI1 (master out / slave in data) P4.5 → MISO1 (master in / slave out data P4.6 → T2 (timer 2 input/output) P4.7 → T2EX (timer 2 external input) P5.0 → SS0 (slave select input) P5.1 → SPICLK0 (SPI0 clock input/output) P5.2 → MOSI0 (master out / slave in data) P5.3 → MISO0 (master in / slave out data) P5.4 → RxD (serial port 1 input) P5.5 → TxD (serial port 1 output) (*) each bit of ports 1, 3, 4 and 5 is composed of three lines: data output, data input and output enable (low level active)

4.3 Memory Organization

ADD8051C3A has separate logical address spaces for program and data memory, as shown in Figure 4-3. The logical separation of program and data memory allows the data memory to be accessed by 8-bit addresses, which can be quickly stored and manipulated by an 8-bit CPU. Nevertheless, 16-bit data memory addresses can also be generated through the DPTR (Data Pointer Registers).

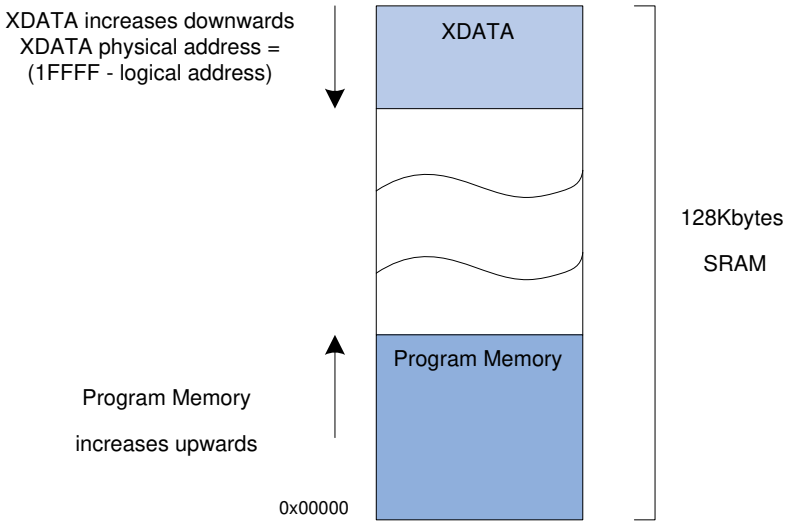
Program Memory and XDATA Memory are combined in a single 128Kbytes SRAM and accessed by the same bus using internal RD and PSEN signals functions.

- Program memory must only be read. Writing in Program Memory could lead to unexpected results and must be avoided. There is a block of 64kbytes of base program memory, which can be increased by extended program pages.

- XDATA occupies a separate address space from Program Memory. Up to 64kbytes of XDATA can be addressed in the Data Memory space. The CPU generates the internal “read” and “write” signals, RD and WR, needed during XDATA Memory accesses.

Additionally to these 128 Kbytes of SRAM, there are 384 bytes of internal data memory (IDATA) in the ADD8051C3A core. This is explained in more detail in 4.3.3 section.

Figure 4-3. 128KB SRAM, XDATA and Program Memory



The program must be uploaded to the SRAM after power up. The source of program must be a non volatile storage unit (i.e. serial flash). A specific module (boot loader peripheral) has been designed to control the booting of the system after power up. The boot loader module can also be used to program the non volatile storage unit (serial flash) using a serial link. The non volatile storage unit must be connected to P5 port pins used for the SPI0 link (see Table 4-1). The serial link to the boot loader shares pins with the microcontroller Serial Port 0. For more information see boot loader section in 8

4.3.1 Program Memory

After reset, the CPU begins execution from location 0000H and stack pointer (SP) value is set to 07H.

Interrupt Handling

A fixed location in Program Memory is assigned to each interrupt. The interrupt causes the CPU to jump to that location, where it begins executing the service routine.

Example: External Interrupt 0, is assigned to location 0003H. If External Interrupt 0 is going to be used, its service routine must begin at location 0003H. If the interrupt is not going to be used, its service location is available as general purpose Program Memory.

The interrupt service locations are spaced at 8-byte intervals beginning at 0x0003 (i.e.0x0003 for External Interrupt0, 0x000B for Timer0, etc.).

If an interrupt service routine is short enough, it can reside entirely within that 8-byte interval. Longer service routines can use a jump instruction to skip over subsequent interrupt locations, if other interrupts are in use.

Program Memory addresses are always 17 bits wide, even though the actual amount of Program Memory used may be less than 64kbytes.

P0 and P2 ports are no longer used to access external memories, but Special Function Registers (SFR) P0 and P2 are still functional.

- P2 register is used to generate the high order address byte when executing MOVX A,@Ri or MOVX @Ri,A.
- P0 register is the program address control register and it is used to specify the size of extended program pages and to control bank switching.

4.3.2 Extended Addressing

ATPL00B combines program code and data in a single 128KB SRAM.

ADDRESS to access program is generated as a function of P0(7:6), P0(5:0) and PC(15:0).

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
P0	SX1	SX0	P05	P04	P03	P02	P01	P00

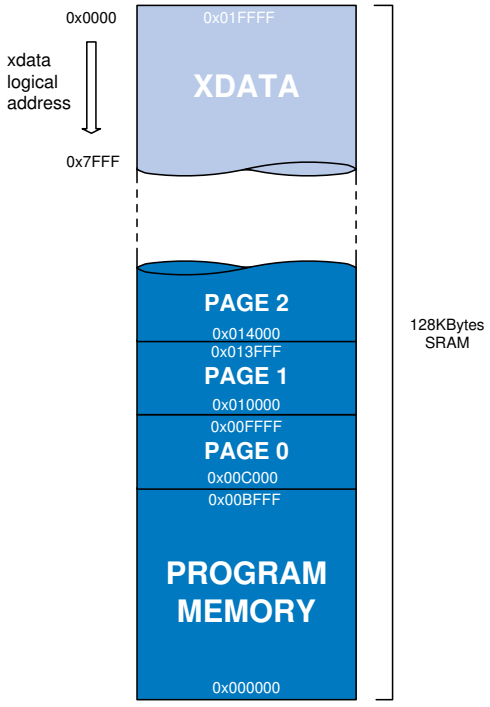
- SX(1:0): Size of extended program pages and common program space

SX(1:0)	Extended	Common
“11”	0KB	64KB
“10”	8KB	56KB
“01”	16KB	48KB
“00”	32KB	32KB

- P0(5:0): Extended program page number

Allowing different configurations as the one shown in Figure 4-4

Figure 4-4. SRAM Extended Addressing. 48KB common memory + 3x16KB extended program pages



Common and extended memory sizes vary depending on the value in P0(7:6), as shown above. According to these size values, the core knows when the PC is pointing to an address located in common memory and when it is pointing to an address located in extended memory. When PC is pointing to an address in extended memory, then P0(5:0) indicates the extended page number and the physical address is automatically calculated. Some examples are shown below.

Example: SX(1:0)=”00” (common memory size = 32KB)

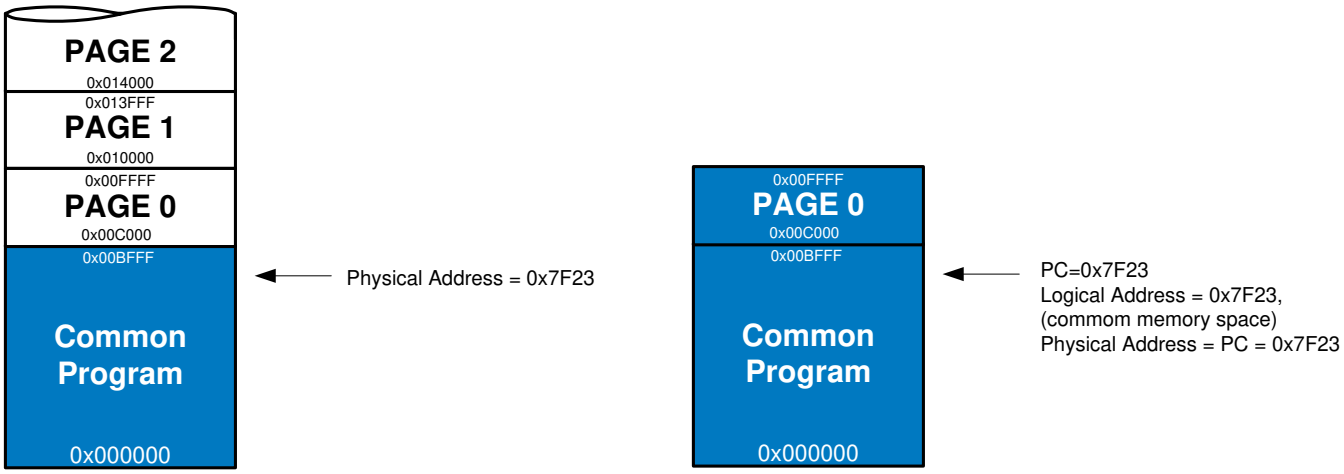
PC=0x7F23 (PC pointing to an address in common memory space)

P0(5:0)= don’t care

LOGIC ADDRESS=0x7F23, common memory space

PHYSICAL ADDRESS=0x7F23 (common memory space → P0(5:0) is ignored)

Figure 4-5. Extended Addressing example 1



Example: SX(1:0)=”00” (common memory size = 32KB)

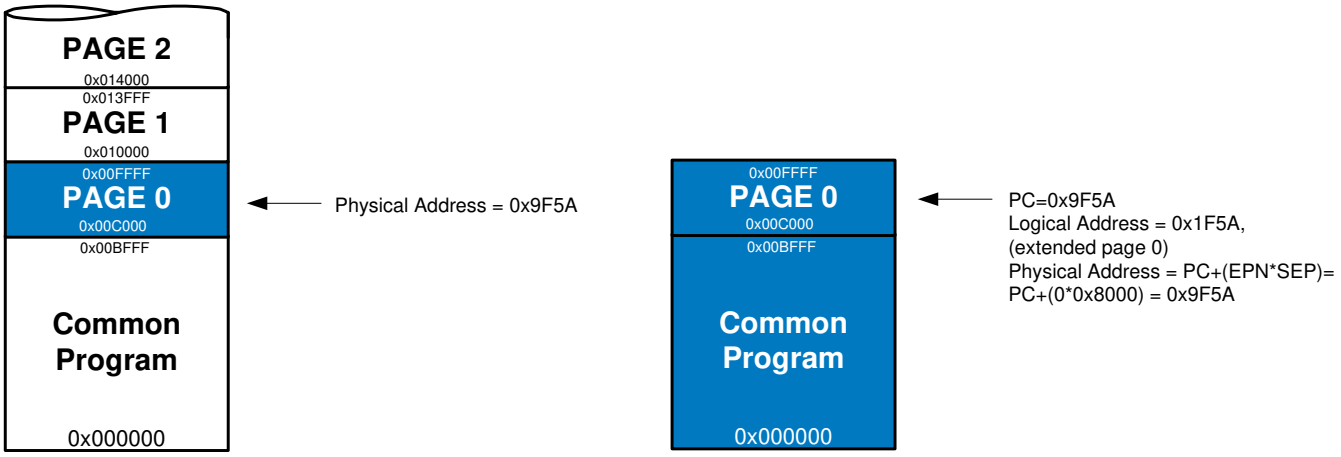
PC=0x9F5A (PC pointing to an address in extended memory)

P0(5:0)= 0x00 (extended page 0)

LOGIC ADDRESS=0x1F5A, extended page 0

PHYSICAL ADDRESS=0x9F5A

Figure 4-6. Extended Addressing example 2



Example: SX(1:0)=”00” (common memory size = 32KB)

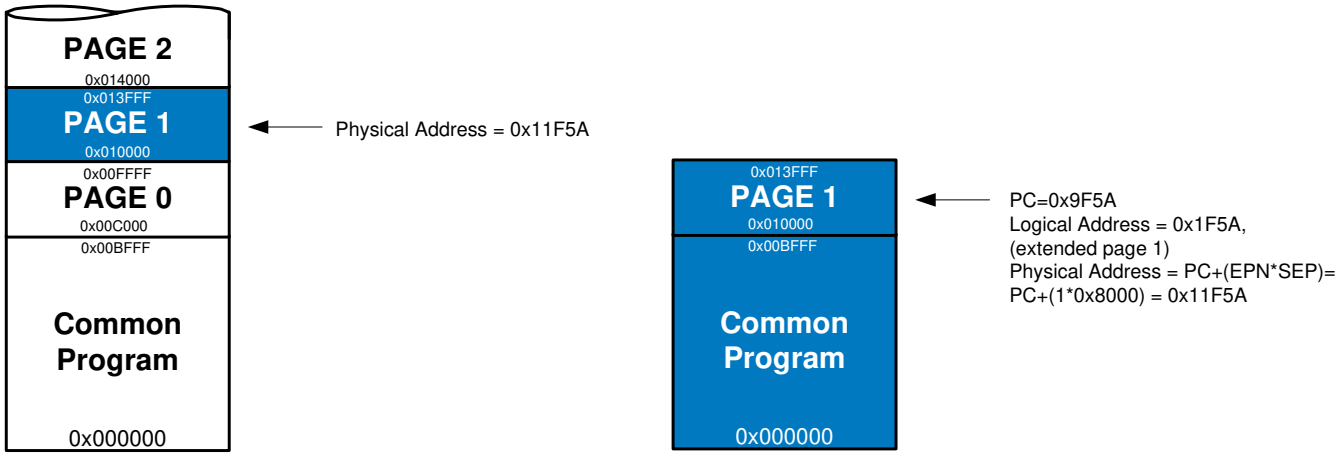
PC=0x9F5A (PC pointing to an address in extended memory)

P0(5:0)= 0x01 (extended page 1)

LOGIC ADDRESS=0x1F5A, extended page 1

PHYSICAL ADDRESS=0x11F5A

Figure 4-7. Extended Addressing example 3



Thus if PC < SCS then Physical Address = PC

else Physical Address = PC+(EPN*SEP)

where SCS= Size of Common Space;

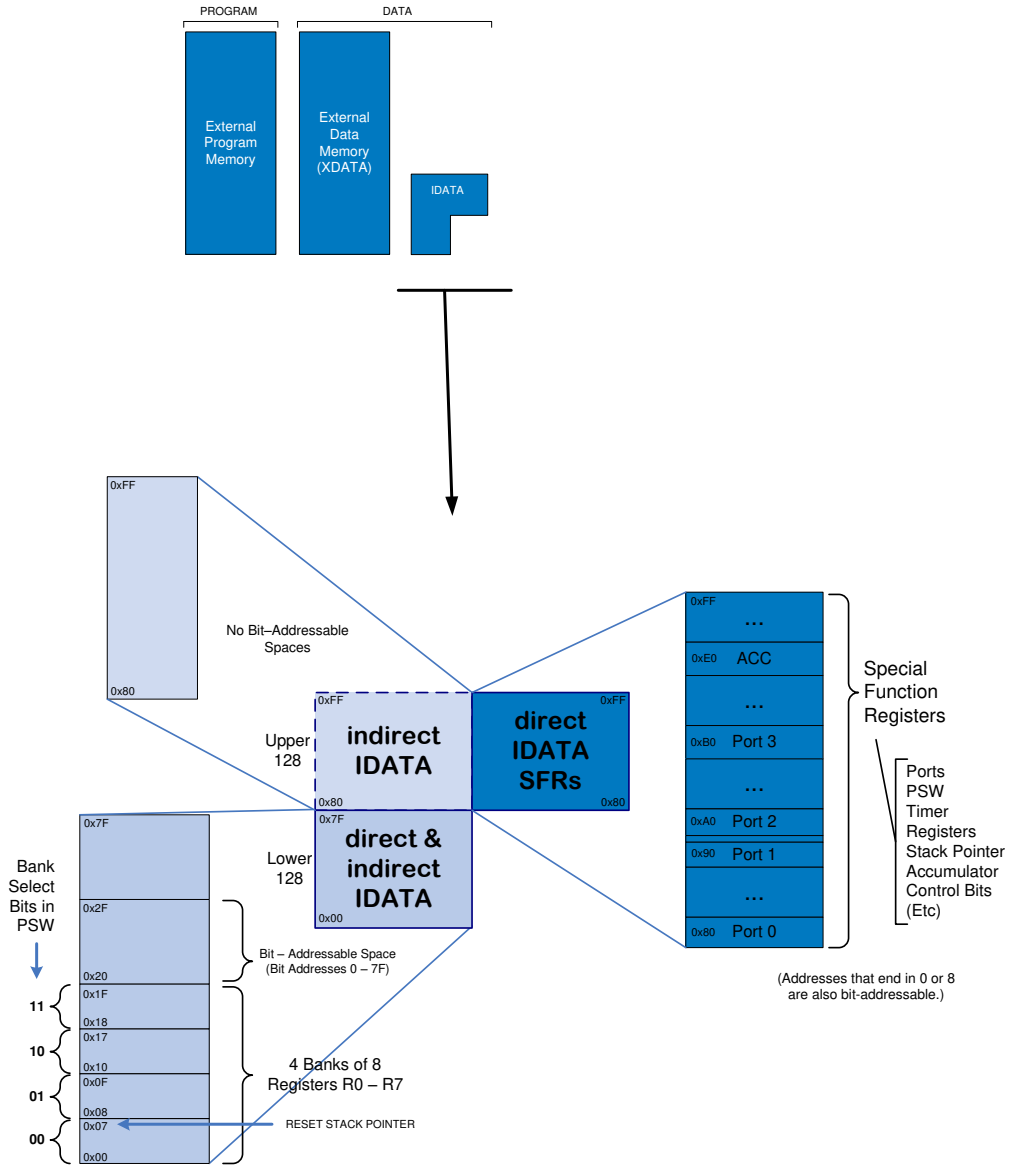
EPN=Extended Page Number;

SEP= Size of Extended Pages(defined by SX(1:0) value).

4.3.3 Data Memory

Figure 4-8 shows the internal and external Logical Data Memory spaces available to the microcontroller user.

Figure 4-8. Data Memory Space



Logical addressing of the Internal Data Memory is mapped as shown in Figure 4-8. The internal IDATA memory space has a total size of 384 bytes and is divided into three blocks, which are generally referred to as the Lower 128 bytes, the Upper 128 bytes and SFR space (128 bytes size).

Internal Data Memory addresses are always one byte wide, which implies an address space of only 256 bytes. A simple trick is used to accommodate the 384 bytes of IDATA using 8 bit addresses: direct addresses higher than 7FH access SFR memory space, whereas indirect addresses higher than 7FH access the Upper 128 bytes of IDATA. Thus, Figure 4-8 shows the Upper 128 bytes and SFR space occupying the same block of addresses, 80H through FFH, although they are physically separate entities.