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Features

- **Supply Voltage: 8.5V**
- **RF Frequency Range: 1400 MHz to 1550 MHz**
- **IF Frequency Range: 150 MHz to 250 MHz**
- **Enhanced IM3 Rejection**
- **Overall Gain Control Range: 30 dB Typically**
- **DSB Noise Figure: 10 dB**
- **Gain-controlled Amplifier and L-band Mixer**
- **Power-down Function for the Analog Part**
- **On-chip Gain-control Circuitry**
- **On-chip VCO, Typical Frequency 1261.568 MHz**
- **Internal VCO Can Be Overdriven by an External LO**
- **On-chip Frequency Synthesizer**
  - **Fixed LO Divider Factor: 2464**
  - **Nine Selectable Reference Divider Factors: 32, 33, 35, 36, 48, 49, 63, 64, 65**
  - **A Reference Oscillator (Can Be Overdriven by an External Reference Signal)**
  - **Tri-state Phase Detector with Programmable Charge Pump**
  - **Programmable Deactivation of Tuning Output**
  - **Lock-status Indication**
  - **Test Interface**

L-band Down-converter for DAB Receivers

ATR2730

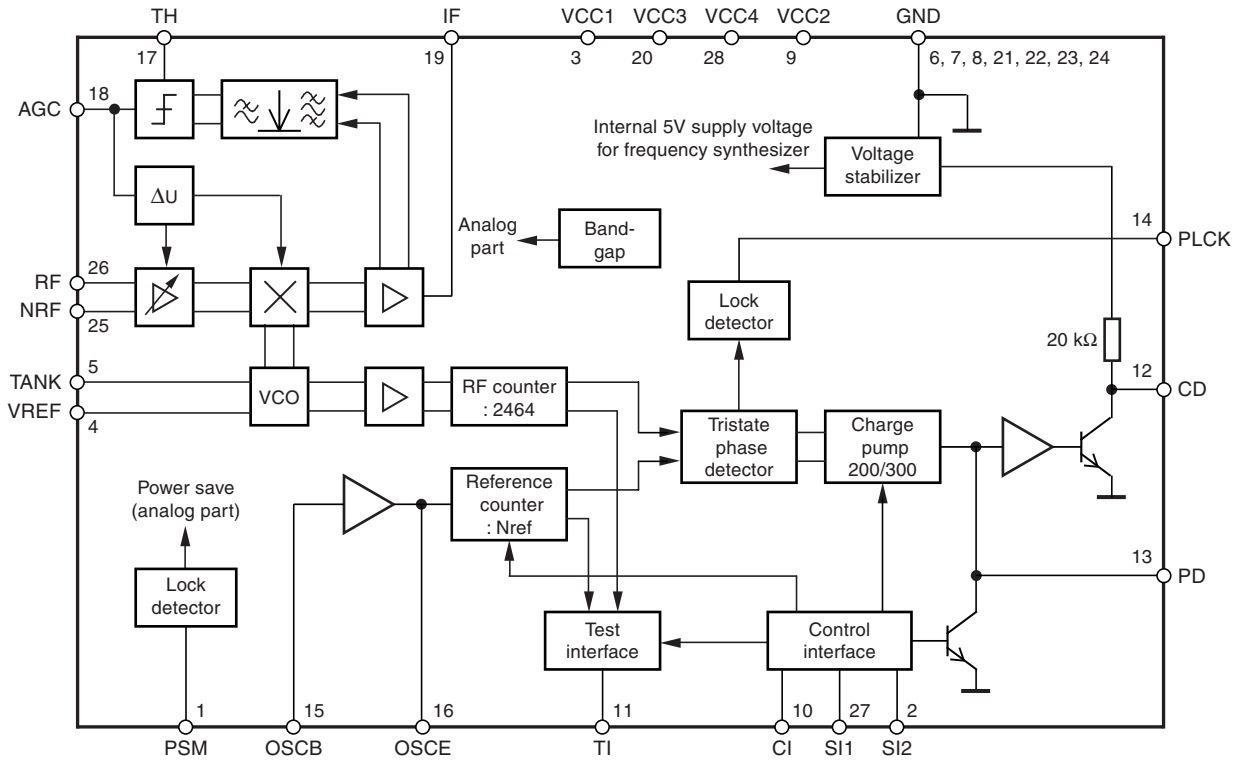
Preliminary

1. Description

The ATR2730 is a monolithically integrated L-band down-converter circuit fabricated with Atmel®'s advanced UHF5S technology. This IC covers all functions of an L-band down-converter in a DAB receiver. The device includes a gain-controlled amplifier, a gain-controlled mixer, an output buffer, a gain control block, a power-save function for the analog part, an L-band oscillator, and a complete frequency synthesizer unit. The frequency synthesizer block consists of a reference oscillator/buffer, a reference divider, an RF divider, a tri-state phase detector, a loop filter amplifier, a lock detector, a programmable charge pump, a test interface, and a control interface.

4903C–DAB–03/07

Figure 1-1. Block Diagram



2. Pin Configuration

Figure 2-1. Pinning SSO28

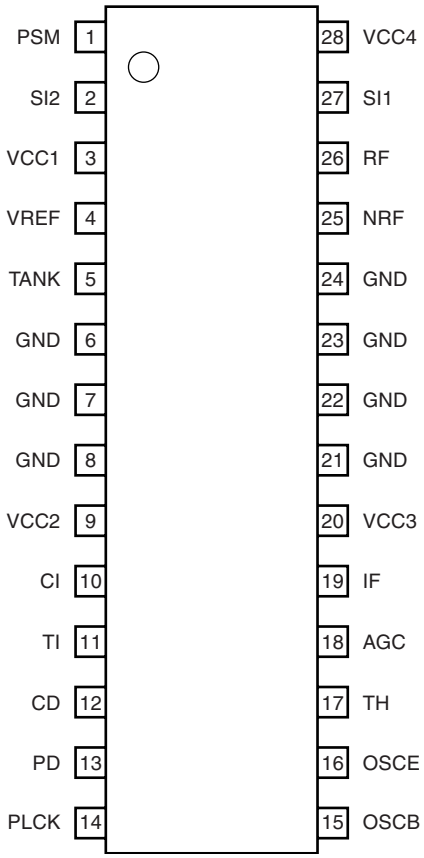


Table 2-1. Pin Description

Pin	Symbol	Function
1	PSM	Power save mode
2	SI2	Control input
3	VCC1	Supply voltage VCO
4	VREF	Reference pin of VCO
5	TANK	Tank pin of VCO
6, 7, 8, 21, 22, 23, 24	GND	Ground
9	VCC2	Supply voltage PLL
10	CI	Control input
11	TI	Test interface
12	CD	Active filter output
13	PD	Tri-state charge pump output
14	PLCK	Lock-indication output (open collector)
15	OSCB	Input of internal oscillator/buffer
16	OSCE	Output of internal oscillator/buffer
17	TH	Threshold voltage of comparator
18	AGC	Charge-pump output of comparator, AGC input for amplifier and mixer
19	IF	Intermediate frequency output
20	VCC3	Supply voltage
25	NRF	RF input (inverted)
26	RF	RF input
27	SI1	Control input
28	VCC4	Supply voltage

3. Functional Description

The ATR2730 is an L-band down-converter circuit covering a gain-controlled amplifier, a gain-controlled mixer, an output buffer, a gain control circuitry, an L-band oscillator, and a frequency synthesizer block. Designed for applications in a DAB receiver, the circuit down-converts incoming L-band signals in the frequency range of 1452 MHz to 1492 MHz to an IF frequency in the range of 190 MHz to 230 MHz, which can be handled by a subsequent DAB tuner. A block diagram of this circuit is shown in Figure 1-1 on page 2.

3.1 Gain-controlled Amplifier

RF signals applied to the RF input pin are amplified by a gain-controlled amplifier. The complementary pin NRF is not internally blocked; it is recommended to block this pin carefully by an external capacitor. The gain-control voltage is generated by internal gain-control circuitry. The output signal of this amplifier is fed to a gain-controlled mixer.

3.2 Gain-controlled Mixer and Output Buffer

The purpose of this mixer is to down-convert the L-band signal in the frequency range of 1452 MHz to 1492 MHz to an IF frequency in the range of about 190 MHz to 230 MHz. Like the amplifier, the gain of the mixer is controlled by the gain-control circuitry. The IF signal is buffered and filtered by a one-pole low-pass filter at a 3 dB frequency of about 500 MHz, and then it is fed to the single-ended output pin IF.

3.3 Gain-control Circuitry

The gain-control circuitry measures the signal power, compares it with a certain power level and generates control voltages for the gain-controlled amplifier and mixer. An equivalent circuit of this functional block is shown in Figure 10-1 on page 14.

In order to meet this functionality, the output signal of the buffer amplifier is weakly band-pass filtered (transition range of about 60 MHz to 550 MHz), rectified, low-pass filtered, and fed to a comparator whose threshold can be defined by an external resistor, RTH, at pin TH. By varying the value of this resistor, a power threshold of about –33 dBm to –20 dBm can be selected. In order to achieve a good intermodulation ratio, it is recommended to keep the power threshold below –25 dBm. An appropriate application is shown in Figure 8-1 on page 12. Depending on the selection made by the comparator, a charge pump charges or discharges a capacitor which is applied to the AGC pin. By varying this capacitor, different time constants of the AGC loop can be realized. The voltage arising at the AGC pin is used to control the gain setting of the gain-controlled amplifier and mixer. The voltage at pin AGC is in the range of 5.75V for maximum gain and 0.3V for minimum gain. This voltage can be use to control a dual-gate GaAs-FET in front of the ATR2730 to achieve an extended AGC range. By applying an external voltage to the AGC pin, the internal AGC loop can be overdriven.

3.4 Voltage-controlled Oscillator

A voltage-controlled oscillator supplies an LO signal to the mixer. An equivalent circuit of this oscillator is shown in Figure 10-2 on page 14. In the application circuits (Figure 10-3 on page 15 and Figure 11-1 on page 16), a ceramic coaxial resonator is applied to the oscillator's TANK and VREF pins. It should be noted that V_{ref} has to be blocked carefully. Figure 11-1 shows a different application where the oscillator is overdriven by an external oscillator. In either case, a DC path at a low impedance must be established between the TANK and VREF pins. The output signal of the oscillator is fed to the LO divider block of the frequency synthesizer unit which locks the VCO's frequency on the frequency of a reference oscillator. Figure 9-1 on page 13 shows the typical phase-noise performance of the oscillator in locked state.

3.5 Overall Properties of the Signal Path

The overall gain of this circuit amounts to 24 dB, the gain-control range is about 30 dB. With a new AGC concept in the amplifier and mixer, the ATR2730 reaches better intermodulation distances (DIM3) at higher IF-output power levels.

3.6 Power Save Mode

For VPSM > 2V (pin 1) the power consumption in the analog part (gain-controlled amplifier and mixer and gain-controlled circuitry) is reduced by 80%. The VCO and the PLL is not influenced by the power-down mode.

3.7 Frequency Synthesizer

The frequency synthesizer block consists of a reference oscillator, a reference divider, an LO divider in order to divide the frequency of the internal oscillator, a tri-state phase detector, a lock detector, a programmable charge pump, a loop filter amplifier, a control interface, and a test interface. The control interface is accessed by three control pins, CI, SI1 and SI2. The test interface provides test signals which represent output signals of the reference and the LO divider.

The purpose of this unit is to lock the frequency f_{VCO} of the internal VCO on the frequency f_{ref} of the reference signal applied to the input pin OSCB phase-locked loop according to the following equation:

$$f_{VCO} = SF \times f_{ref} / SF_{ref}$$

where: SF = 2464,

SF_{ref} is the scaling factor of the reference divider according to Table 3-1

Table 3-1. Scaling Factors of the Reference Frequency

Voltage at Pin SI1	Voltage at Pin SI2	SF_{ref}	Reference Oscillator Frequency
GND	OPEN	36	18.432 MHz
GND	VCC	33	–
GND	GND	48	24.576 MHz
OPEN	OPEN	65	–
OPEN	VCC	63	–
OPEN	GND	64	32.768 MHz
VCC	OPEN	35	17.920 MHZ
VCC	VCC	32	16.384 MHz
VCC	GND	49	–

3.8 Reference Oscillator

An on-chip crystal oscillator generates the reference signal which is fed to the reference divider. By connecting a quartz crystal to pins OSCE and OSCB according to Figure 11-2 on page 16, this oscillator generates a highly stable reference signal. The ATR2731 (Atmel's one-chip front-end IC) offers the reference signal at pin FREF. This reference signal (LC filtered to suppress harmonics) can be used to overdrive the oscillator. In this application (see Figure 11-3 on page 16) the reference signal has to be applied to the pin OSCB and the pin OSCE must be left open.

3.9 Reference Divider

Nine different scaling factors of the reference divider can be selected by different voltage settings at the input pins SI1 and SI2: 32, 33(1), 35, 36, 48, 49(1), 63(1), 64, 65(1). The reference divider factors result in reference oscillator frequencies shown in Table 3-1.

Note: 1. These scaling factors result in an output frequency of the reference divider of 512 kHz. If harmonics of the Bd. 3 VCO fall in the L-band reception band, these spurious signals can influence the AGC of ATR2730, which could be a problem for small incoming signals. In this case it is possible to switch the reference divider from n_{ref} to n_{ref} + 1.

3.10 LO Divider

The LO divider is operated at the fixed division ratio 2464. Assuming the settings described in the section "Reference Divider" , the oscillator's frequency is controlled to be 1261.568 MHz in the locked state, and the output frequency of the RF divider is 512 kHz.

3.11 Phase Comparator, Charge Pump and Loop Filter

The tri-state phase detector causes the charge pump to source or sink current at the output pin PD depending on the phase relation of its input signals, which are provided by the reference and the RF divider respectively. Using the control pin CI, two different values of this current can be selected, and the charge-pump current can be switched off.

The input of the high-gain amplifier (output pin CD), which is implemented in order to construct a loop filter as shown in the application circuit, can be switched to GND by means of the control pin CI (see Table 3-2 on page 8). In the application circuit, the loop filter is completed by connecting the pins PD and CD by an appropriate RC network.

3.12 Lock Detector

An internal lock detector checks if the phase difference of the input signals of the phase detector is smaller than approximately 250 ns in seven subsequent comparisons. If a phase lock is detected, the open collector output pin PLCK is set to HIGH. It should be noted that the output current of this pin must be limited by external circuitry as it is not limited internally. If the voltage at the control pin CI is chosen to be half the supply voltage, or if this control pin is left open, the lock-detector function is deactivated and the logical value of the PLCK output is undefined.

3.13 Test Interface

If the input control pin CI is left open (high impedance state), a test signal, which monitors the output frequency of the reference divider, appears at the output pin TI.

Analogous to the reference divider, a test signal monitoring the output frequency of the RF divider appears at the test interface output pin TI, if the input control pin CI is connected to $V_{CC}/2$.

Table 3-2. Control Interface (CI) Settings

CI	PD	PLCK	TI
GND	200 µA	Ok	–
V_s	300 µA	Ok	–
$V_{CC}/2$	0 µA	Undefined	RF divider
Open	Connected to GND	Undefined	Reference divider

4. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Pins	Symbol	Value	Unit
Supply voltage	3, 9, 20 and 28	V_{CC}	–0.3 to +9.5	V
RF input voltage	25 and 26	V_{RF}	750	mV_{pp}
Voltage at pin AGC	18	V_{AGC}	0.5 to 6	V
Voltage at pin TH	17	V_{TH}	–0.3 to +4.0	V
Input voltage at pin TANK (internal oscillator overdriven)	5	V_{TANK}	1	V_{pp}
Current at IF output	19	I_{IF}	4.0	mA
Reference input voltage (diff.)	15	OSCB	1	V_{pp}
Control input voltage	1, 2, 10 and 27	CI, SI1, SI2, PD	–0.3 to +9.5	V
PLCK output current	14	I_{PLCK}	0.5	mA
PLCK output voltage	14	V_{PLCK}	–0.3 to +5.5	V
Junction temperature		T_j	125	°C
Storage temperature		T_{stg}	–40 to +125	°C

5. Operating Range

Parameters	Pins	Symbol	Value	Unit
Supply voltage	3, 9, 20 and 28	V_{CC}	8 to 9.35	V
Ambient Temperature		T_{amb}	–40 to +85	°C

6. Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient SSO28 (mod.)	R_{thJA}	50	K/W

7. Electrical Characteristics

Operating conditions: V_{CC} = 8.5V, T_{amb} = 25° C unless otherwise specified. (See application circuit Figure 10-3 on page 15.)

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1.1	Supply current (max. gain)	p_{RF} = –60 dBm V_{PSM} < 0.5V		$I_{S,MAX}$		40	48	mA	A
1.2	Supply current (min. gain)	p_{RF} = –10 dBm V_{PSM} < 0.5V		$I_{S,MIN}$		41	50	mA	B
1.3	Supply current (power-save mode)	p_{RF} = –10 dBm V_{PSM} > 2V		$I_{S,PD}$		20	24	mA	A
2	**Amplifier Mixer Pin 26**		**26 →19**						
2.1	Maximum conversion gain	p_{RF} = –60 dBm		$g_{c,max}$	20	24		dB	A
2.2	Minimum conversion gain	p_{RF} = –15 dBm		$g_{c,min}$		–8		dB	B
2.3	AGC range			Δg_c	28	32		dB	A
2.4	Third-order 2-tone intermodulation ratio	p_{RF1} + p_{RF2} = –10 dBm p_{RF1} + p_{RF2} = –15 dBm		dim3	30 35	35 40		dB dB	B A
2.5	DSB noise figure (50Ω system)	Maximum gain Minimum gain		NF		10 30		dB dB	D
3	**RF Input**		**26**						
3.1	Frequency range			$f_{in,RF}$	1400		1550	MHz	C
3.2	Maximum input power	dim3 ≥ 20 dB		$p_{in,max,RF}$		–6		dBm	C
3.3	Input impedance			$Z_{in,RF}$		200 || 1		Ω || pF	D
4	**IF Output**		**19**						
4.1	Frequency range			$f_{out,IF}$	150		250	MHz	C
4.2	Output impedance			$Z_{out,IF}$		50		Ω	D
4.3	Voltage standing wave ratio			$VSWR_{IF}$		2.0			D
5	**Gain Control**								
5.1	Threshold adjustment	External resistor	17	R_{TH}		100		kΩ	D
5.2	Charge pump current	p_{RF} = –10 dBm V_{AGC} = 3.5V	18	$I_{CP,P}$	75	100	125	µA	A
		p_{RF} = –60 dBm V_{AGC} = 3.5V		$I_{CP,N}$	–125	–100	–75	µA	A
5.3	Minimum gain control voltage	p_{RF} = –10 dBm	18	V_{AGCmin}		0.1	0.6	V	A
5.4	Maximum gain control voltage	p_{RF} = –60 dBm	18	V_{AGC}max	5.5	5.75		V	A
6	**VCO**		**5**						
6.1	Frequency			f_{LO}	1000	1261.568	1500	MHz	
6.2	Phase noise	1 kHz distance		L_{1kHz}		–75		dBc/Hz	C
6.3	Minimum input power	VCO overdriven, see “Application Circuit” (Figure 10-3 on page 15)		$p_{LO,MIN}$		–11		dBm	C
6.4	Maximum input power			$p_{LO,MAX}$		–5		dBm	C
7	**Frequency Synthesizer**								
7.1	RF divide factor			SF		2464			A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

7. Electrical Characteristics (Continued)

Operating conditions: V_{CC} = 8.5V, T_{amb} = 25° C unless otherwise specified. (See application circuit Figure 10-3 on page 15.)

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
7.2	Reference divide factor	SI1 = GND, SI2 = GND SI1 = GND, SI2 = VCC SI1 = GND, SI2 = open SI1 = VCC, SI2 = GND SI1 = VCC, SI2 = VCC SI1 = VCC, SI2 = open SI1 = open, SI2 = GND SI1 = open, SI2 = VCC SI1 = open, SI2 = open		SF_{ref}		48 33 36 49 32 35 64 63 65			A
7.3	Input frequency range			f_{ref}	5		50	MHz	C
7.4	Input sensitivity		15	V_{refs}			30	mV_{rms}	C
7.5	Maximum input signal		15	V_{refmax}		300		mV_{rms}	C
7.6	Input impedance	Single-ended		Z_{ref}		2.7k ‖ 2.5		kΩ ‖ pF	D
8	**Phase Detector**								
8.1	Charge-pump current	Pin CI connected to GND	13	I_{PD2}	160	200	240	µA	A
		Pin CI connected to V_{CC}		I_{PD1}	240	300	360	µA	A
		Pin CI connected to $V_{CC}/2$		$I_{PD1,tri}$			100	nA	A
8.2	Output voltage PD	Pin CI open	13	V_{PD}			0.3	V	A
8.3	Internal reference frequency			f_{PD}		512		kHz	B
8.4	Typical tuning voltage range		12	V_{tune}	0.3		5	V	C
9	**Lock Indication PLCK**		**14**						
9.1	Leakage current	V_{PLCK} = 5.5V		I_{PLCK}			10	µA	A
9.2	Saturation voltage	I_{PLCK} = 0.25 mA		$V_{PLCK,sat}$			0.5	V	A
10	**Control Inputs SI**		**2 and 27**						
10.1	Input voltage	Pin connected to GND		V_L	0		0.1	V_{CC}	A
10.2		Pin open		V_M		Open			A
10.3		Pin connected to V_{CC}		V_H	0.9		1	V_{CC}	A
11	**Control Input CI**		**10**						
11.1	Input voltage	Pin connected to GND		V_L	0		0.1	V_{CC}	A
11.2		Pin connected to $V_{CC}/2$		V_M		0.5		V_{CC}	A
11.3		Pin open		V_{open}		Open			A
11.4		Pin connected to V_{CC}		V_H	0.9		1	V_{CC}	A
12	**Test Interface TI**		**11**						
12.1	Reference test frequency	Pin CI open		$f_{test,ref}$		512		kHz	B
12.2	LO test frequency	Pin CI = $V_{CC}/2$		$f_{test,LO}$		512		kHz	B
12.3	Voltage swing	$R_{load} \geq 1$ MΩ, $C_{load} \leq 15$ pF, Pin CI open or $V_{CC}/2$		V_{sw}		400		mV_{pp}	C
13	**Power-save Mode PSM**		**1**						
13.1		PSM not active		V_{PSM}			0.6	V	A
13.2		PSM active		V_{PSM}	2.0			V	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

8. Gain Control Characteristics

Operating conditions: V_{CC} = 8.5V, T_{amb} = 27° C, f_{RF} = 1490 MHz, F_{LO} = 1261.568 MHz

Figure 8-1. IF Output Power (Pin 19)

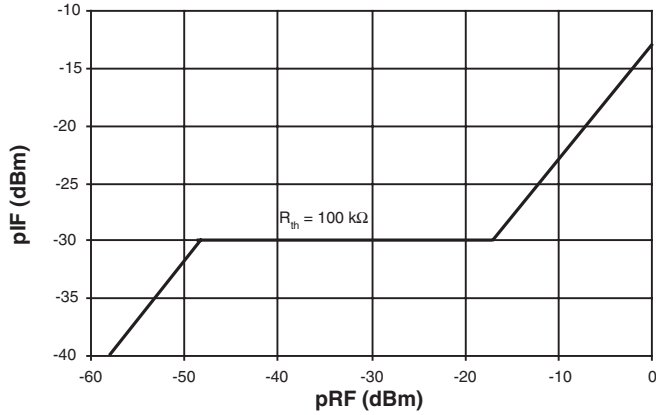
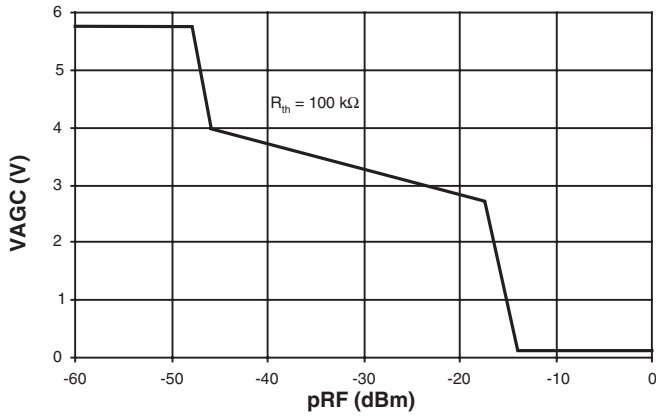


Figure 8-2. Gain Control Voltage (Pin 11)



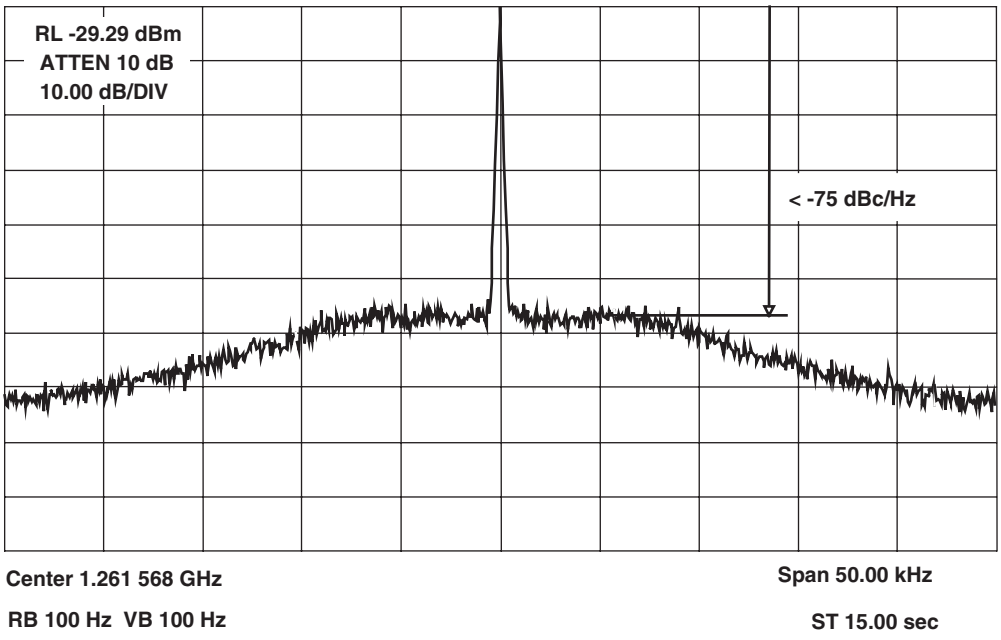
9. Phase-noise Performance

Measurement conditions:

Values acquired at pin 19 with HP 70000 spectrum analyzer. RF input (pin 26) is blocked with 100 pF to GND.

A low phase-noise signal generator (Marconi® 2042) was taken as PLL reference.

Figure 9-1. Phase-noise Performance Operating Conditions: f_{REF} = 17.92 MHz, –10 dB, I_{PD} = 200 µA



10. Equivalent Circuits

Figure 10-1. AGC Control Circuit

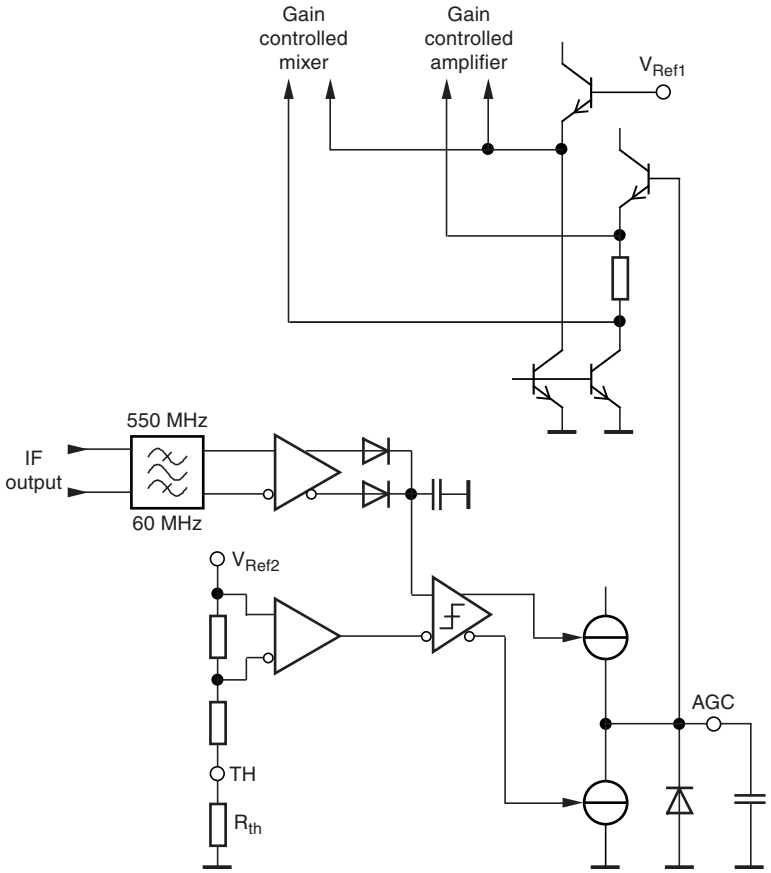
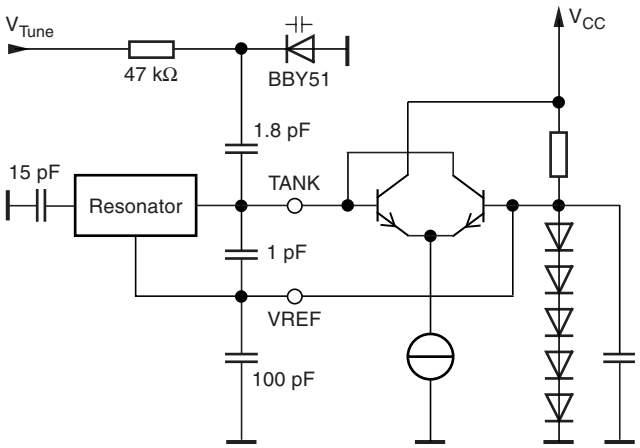
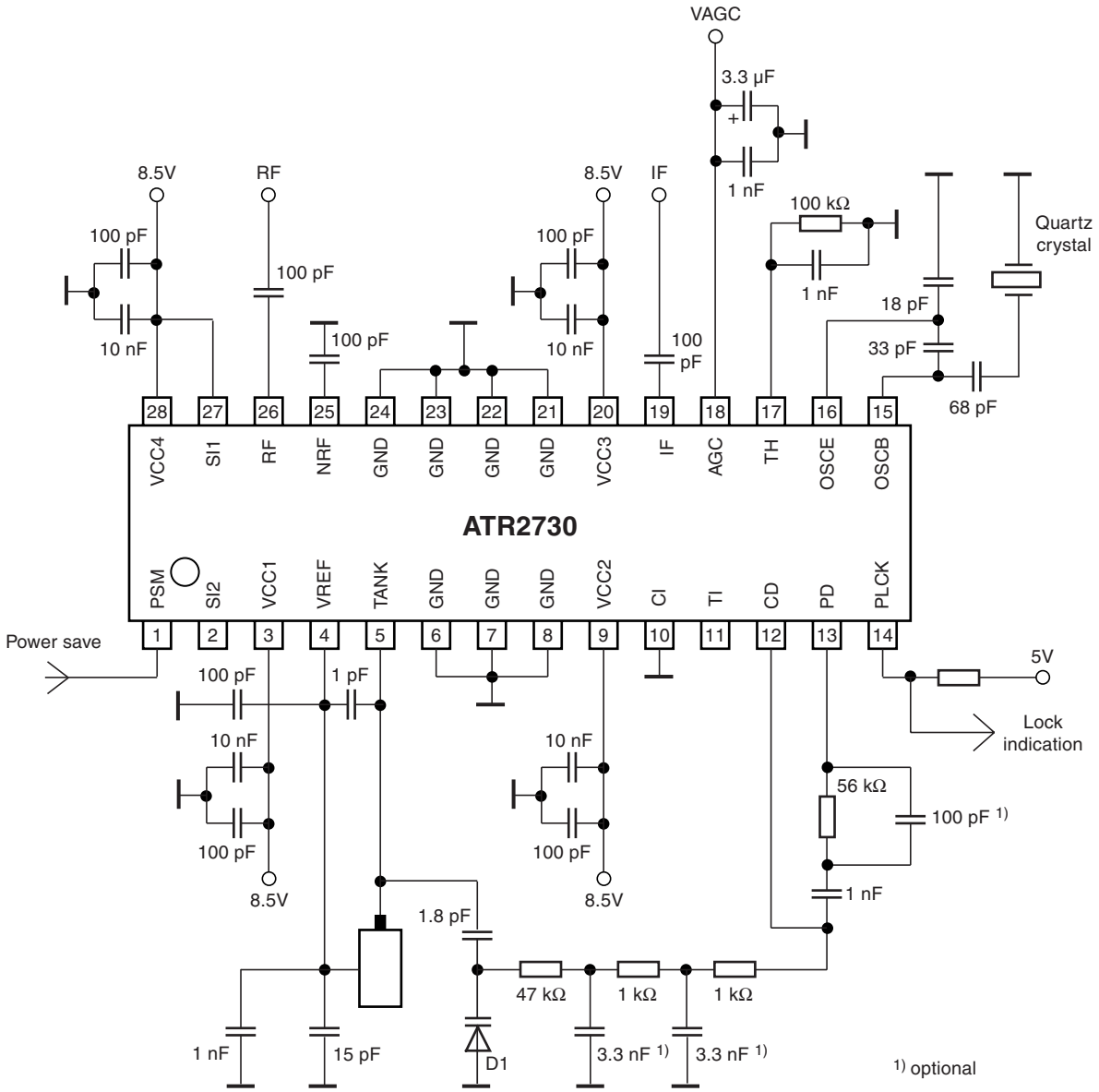


Figure 10-2. VCO Circuit



Resonator: Ceramic coaxial resonator
Murata® 3 × 3 mm, 1.6 GHz
DRR030 KE1R600TC

Figure 10-3. Application Circuit



Example: reference divider factor = 35, f_{REF} = 17.92 MHz, charge-pump current = 200 µA

11. Application Circuit for External LO Signal

With an external LO signal it is possible to overdrive the VCO. In this case, the internal VCO acts as an LO buffer.

Figure 11-1. Application Circuit for External LO Signal

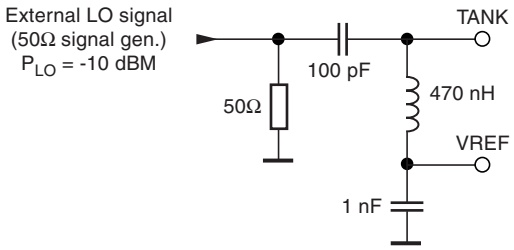


Figure 11-2. Reference Oscillator Operation

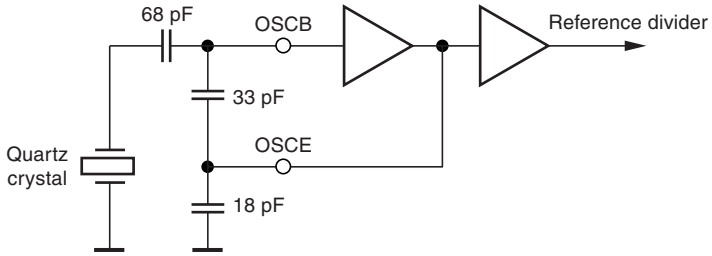
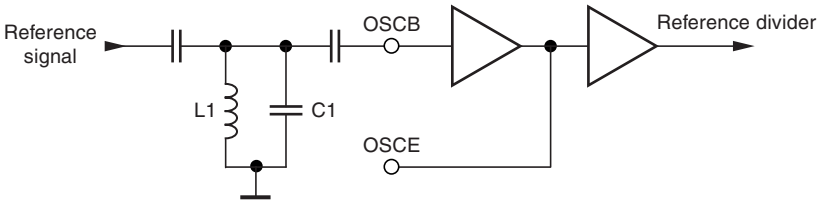


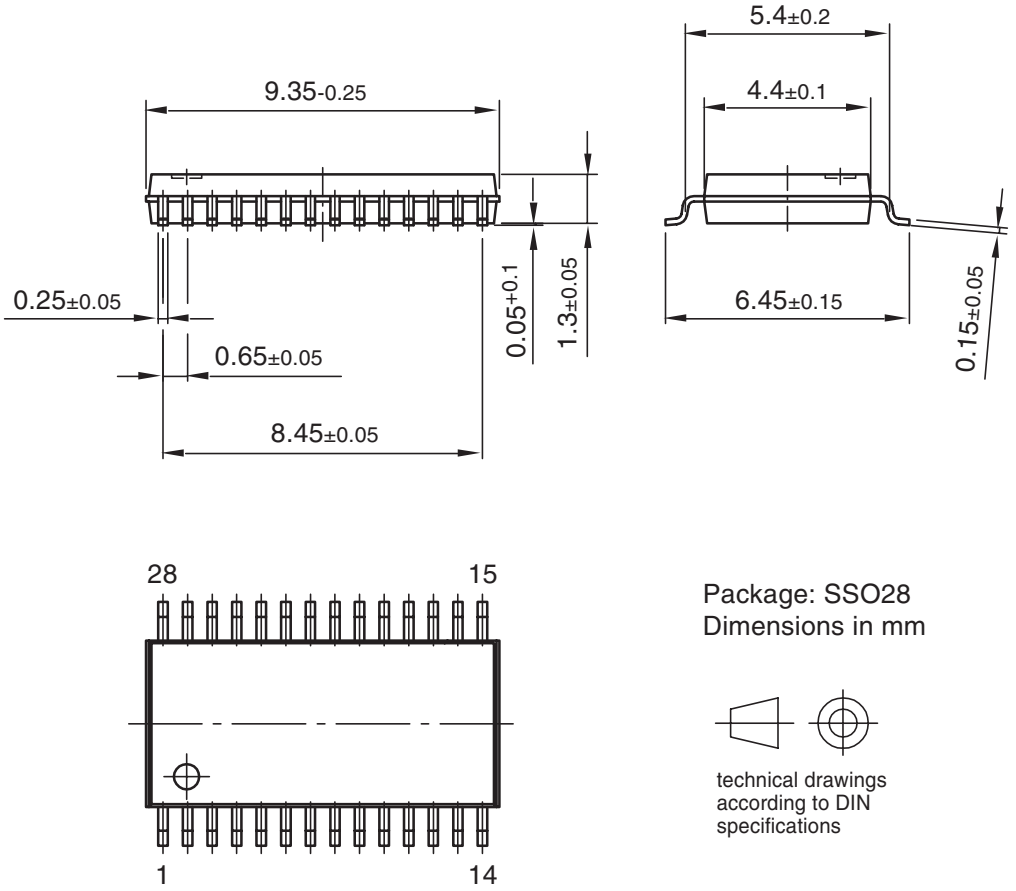
Figure 11-3. Reference Oscillator Overdriven



12. Ordering Information

Extended Type Number	Package	Remarks
ATR2730-TLSY	SSO28	Tube, Pb-free
ATR2730-TLPY	SSO28	Taped and reeled according to IEC 286-3, 180 µm size, Pb-free
ATR2730-TLQY	SSO28	Taped and reeled according to IEC 286-3, 330 µm size, Pb-free

13. Package Information



Package: SSO28
Dimensions in mm

technical drawings
according to DIN
specifications

Drawing-No.: 6.543-5056.03-4
Issue: 1; 10.03.04

14. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4903C-DAB-03/07	• Put datasheet in a new template • Section 12 “Ordering Information” on page 17 changed

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