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## Features

- Reference Oscillator up to 15 MHz
- Two Programmable 16-bit Dividers Adjustable from 2 to 65535
- Fine Tuning Steps
  - AM  $\geq$  1 kHz
  - FM  $\geq$  2 kHz
- Four Programmable Switching Outputs (Open Drain up to 15V)
- Integrated Loop-push-pull Stage for AM/FM
- High Signal/Noise Ratio



## 1. Description

The ATR4285 is an integrated circuit in BiCMOS technology for frequency synthesizers. It performs all the functions of a PLL radio tuning system and is controlled by a 2-wire bus. The device is designed for all frequency synthesizer applications in radio receivers, as well as for RDS (Radio Data System) applications.



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**AM/FM PLL with  
4 Switches**

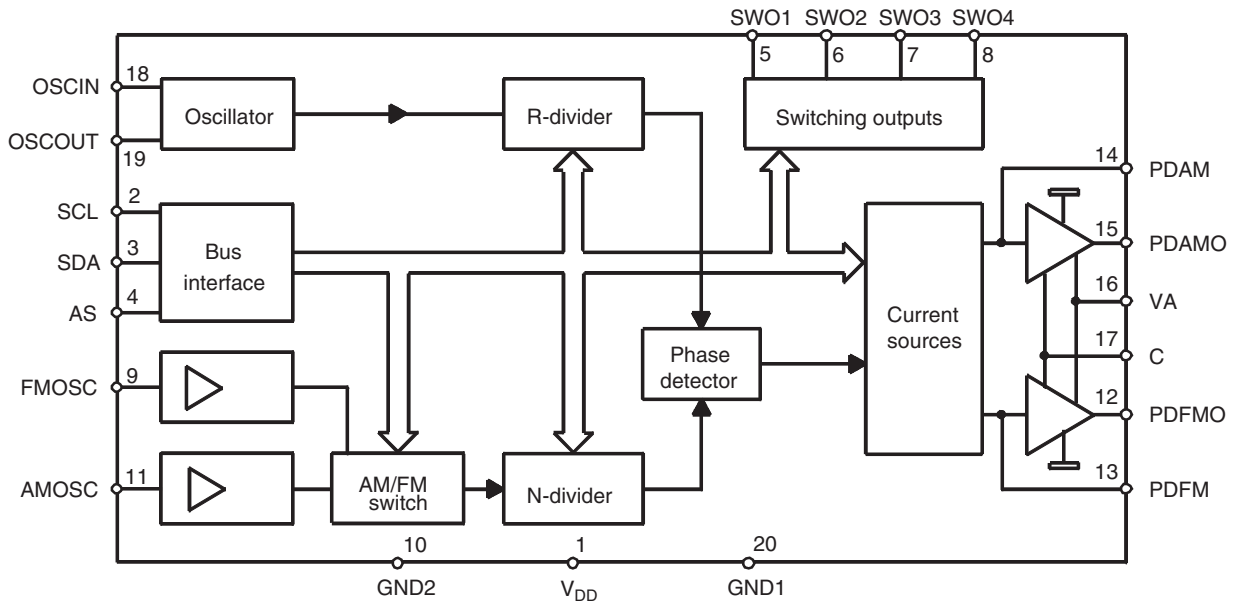
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**ATR4285**

Rev. 4884A–AUDR–08/05



**Figure 1-1.** Block Diagram



## 2. Pin Configuration

Figure 2-1. Pinning SSO20

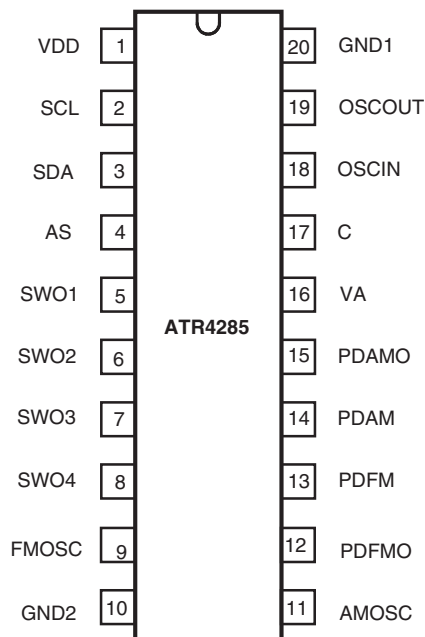


Table 2-1. Pin Description

Pin	Symbol	Function
1	VDD	Supply voltage
2	SCL	Bus clock
3	SDA	Bus data
4	AS	Address selection
5	SWO1	Switching output 1
6	SWO2	Switching output 2
7	SWO3	Switching output 3
8	SWO4	Switching output 4
9	FMOSC	FM oscillator input
10	GND2	Ground 2 (analog)
11	AMOSC	AM oscillator input
12	PDFMO	FM analog output
13	PDFM	FM current output
14	PDAM	AM current output
15	PDAMO	AM analog output
16	VA	Analog supply voltage
17	C	Capacitor
18	OSCIN	Oscillator input
19	OSCOUT	Oscillator output
20	GND1	Ground 1 (digital)

### 3. Functional Description

The ATR4285 is controlled via the 2-wire bus. One module-address byte, two subaddress bytes, and five data bytes enable programming.

The module address contains a programmable address bit A1, which (along with address select input AS, pin 4) enables the operation of two ATR4285 devices in one system. If bit A1 is identical with the status of the address select input AS, the chip is selected.

The subaddress determines which of the data bytes is transmitted first. If the subaddress of the R-divider is transmitted, the sequence of the next data bytes is DB 0 (status), DB 1 and DB 2. If the subaddress of the N-divider is transmitted, the sequence of the next data bytes is DB 3 and DB 4. The bit organization of the module address, subaddress and data bytes is shown in Table [“Bit Organization” on page 9](#).

Each transmission on the bus begins with the "START" condition and must be ended by the "STOP" condition (see Table [“Transmission Protocol” on page 9](#)).

The integrated circuit ATR4285 has two separate inputs for the AM and FM oscillators. Pre-amplified AM and FM signals are fed to the 16-bit N-divider via the AM/FM switch. The AM/FM switch is software controlled. Tuning steps can be selected by the 16-bit R-divider.

Furthermore, the device provides a digital memory phase detector and two separate current sources for AM and FM amplifiers (charge pump) as given in the Table [“Electrical Characteristics” on page 5](#). The separate current sources (charge pumps) allow independent gain adjustment, providing high current for high-speed tuning and low current for stable tuning.

## 4. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Pins	Symbol	Value	Unit
Supply voltage	1	$V_{DD}$	-0.3 to +6	V
Input voltage	2, 3, 4, 9, 11, 18, 19	$V_I$	-0.3 to $V_{DD} + 0.3$	V
Output current	3, 5, 6, 7, 8	$I_O$	-1 to +5	mA
Output drain voltage	5, 6, 7, 8	$V_{OD}$	15	V
Analog supply voltage with 220 $\Omega$ serial resistance 2 minutes <sup>(1)</sup>	16	$V_A$ $V_A$	6 to 15 24	V V
Output current	12, 15	$I_{AO}$	-1 to +20	mA
Ambient temperature range		$T_{amb}$	-30 to +85	°C
Storage temperature range		$T_{stg}$	-40 to +125	°C
Junction temperature		$T_j$	125	°C
Electrostatic handling (modified MIL STD 883 D method 3015.7: all supply pins connected together)		$\pm V_{ESD}$	1000	V

Note: 1. Corresponding to the application circuit (Figure 9-1 on page 10)

## 5. Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	$R_{thJA}$	160	K/W

## 6. Electrical Characteristics

$V_{DD} = 5V$ ,  $V_A = 10V$ ,  $T_{amb} = 25^\circ C$ , unless otherwise specified

Parameters	Test Conditions	Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage		1	$V_{DD}$	4.5	5.0	5.5	V
Quiescent supply current	AM mode/FM mode	1	$I_{DD}$		4.0	7.0	mA
FM input sensitivity, $R_G = 50\Omega$ , FMOSC	$f_i = 70$ MHz to 120 MHz	9	$V_{SF\text{M}}$	40			mV <sub>rms</sub>
	$f_i = 160$ MHz	9	$V_{SF\text{M}}$	150			mV <sub>rms</sub>
AM input sensitivity, $R_G = 50\Omega$ , AMOSC	$f_i = 0.6$ MHz to 35 MHz	11	$V_{S\text{AM}}$	40			mV <sub>rms</sub>
Oscillator input sensitivity, $R_G = 50\Omega$ , OSCIN	$f_i = 0.1$ MHz to 15 MHz	18	$V_{S\text{OSC}}$	100			mV <sub>rms</sub>
<b>Switching Output SWO1, SWO2, SWO3, SWO4 (Open Drain)</b>							
Output voltage LOW	$I_L = 1$ mA	5, 6, 7, 8	$V_{SW\text{OL}}$		100	400	mA
Output leakage current HIGH	V5, V6, V7, V8 = 10V	5, 6, 7, 8	$I_{O\text{HL}}$			100	nA
<b>Phase Detector PDFM</b>							
Output current 1		13	$\pm I_{PDF\text{M}}$	1600	2000	2400	$\mu\text{A}$
Output current 2		13	$\pm I_{PDF\text{M}}$	400	500	600	$\mu\text{A}$

## 6. Electrical Characteristics (Continued)

$V_{DD} = 5V$ ,  $V_A = 10V$ ,  $T_{amb} = 25^\circ C$ , unless otherwise specified

Parameters	Test Conditions	Pins	Symbol	Min.	Typ.	Max.	Unit
Leakage current		13	$\pm I_{PDFML}$			20	nA
<b>Phase Detector PDAM</b>							
Output current 1		14	$\pm I_{PDAM}$	160	200	240	$\mu A$
Output current 2		14	$\pm I_{PDAM}$	40	50	60	$\mu A$
Leakage current		14	$\pm I_{PDAML}$			20	$\mu A$
<b>Analog Output PDFMO, PDAMO</b>							
Saturation voltage LOW	$I = 15\text{ mA}$	12, 15	$V_{satL}$		200	400	mW
Saturation voltage HIGH	$I = 15\text{ mA}$	12, 15	$V_{satH}$	9.5	9.95		V
<b>Bus SCL, SDA, AS</b>							
Input voltage HIGH		2, 3, 4	$V_{IBUS}$	3.0		$V_{DD}$	V
Input voltage LOW		2, 3, 4	$V_{IBUS}$	0		1.5	V
Output voltage acknowledge LOW	$I_{SDA} = 3\text{ mA}$	3	$V_O$			0.4	V
Clock frequency		2	$f_{SCL}$			100	kHz
Rise time SDA, SCL		2, 3	$t_r$			1	$\mu s$
Fall time SDA, SCL		2, 3	$t_f$			300	ns
Period of SCL HIGH	HIGH	2	$t_H$	4.0			$\mu s$
Period of SCL LOW	LOW	2	$t_L$	4.7			$\mu s$
<b>Set-up Time</b>							
Start condition			$t_{sSTA}$	4.7			$\mu s$
Data			$t_{sDAT}$	250			$\mu s$
Stop condition			$t_{sSTOP}$	4.7			$\mu s$
Time space <sup>(1)</sup>			$t_{wSTA}$	4.7			$\mu s$
<b>Hold Time</b>							
Start condition			$t_{hSTA}$	4.0			$\mu s$
Data			$t_{hDAT}$	0			$\mu s$

Note: 1. This is a period of time where the bus must be free from data transmission before a new transmission can be started.

Figure 6-1. FM Input Sensitivity, T = 85°C

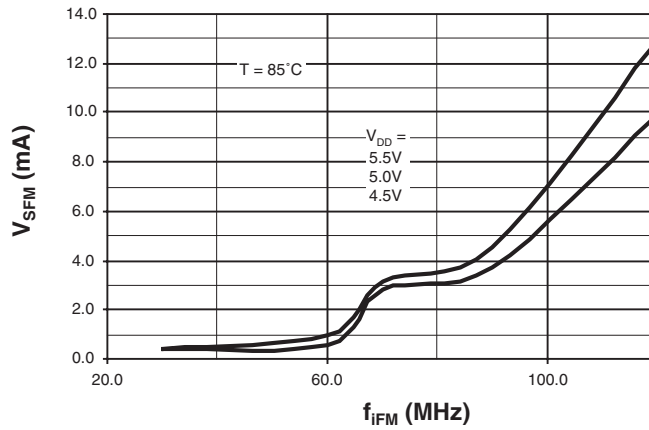


Figure 6-2. FM Input Sensitivity, T = -30°C

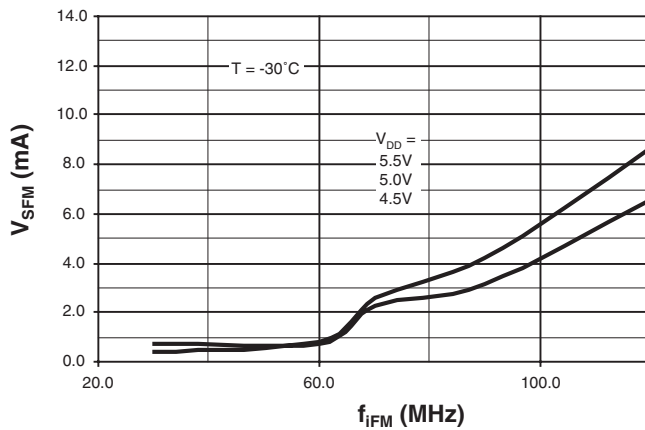
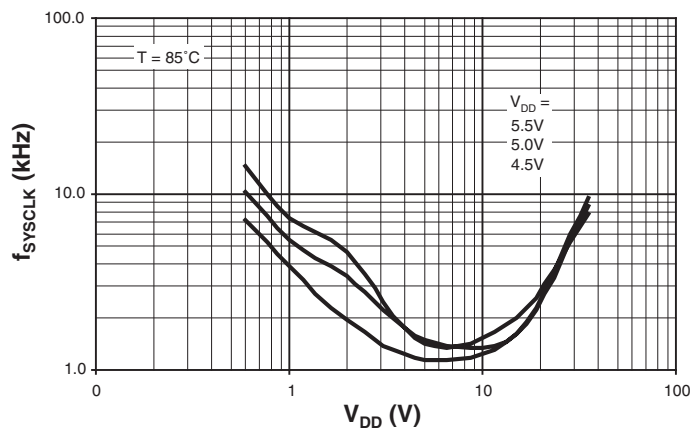
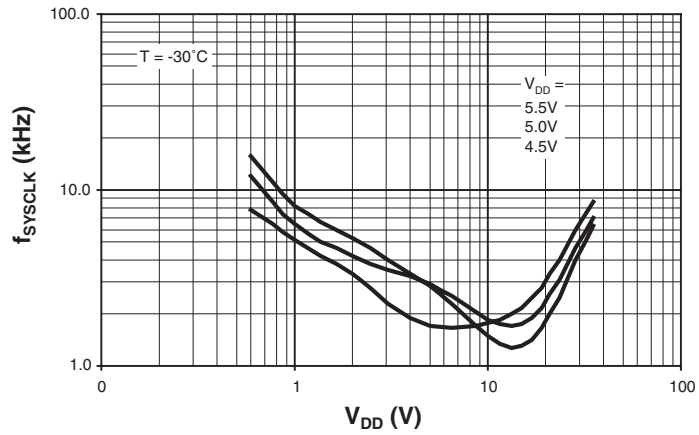


Figure 6-3. AM Input Sensitivity, T = 85°C

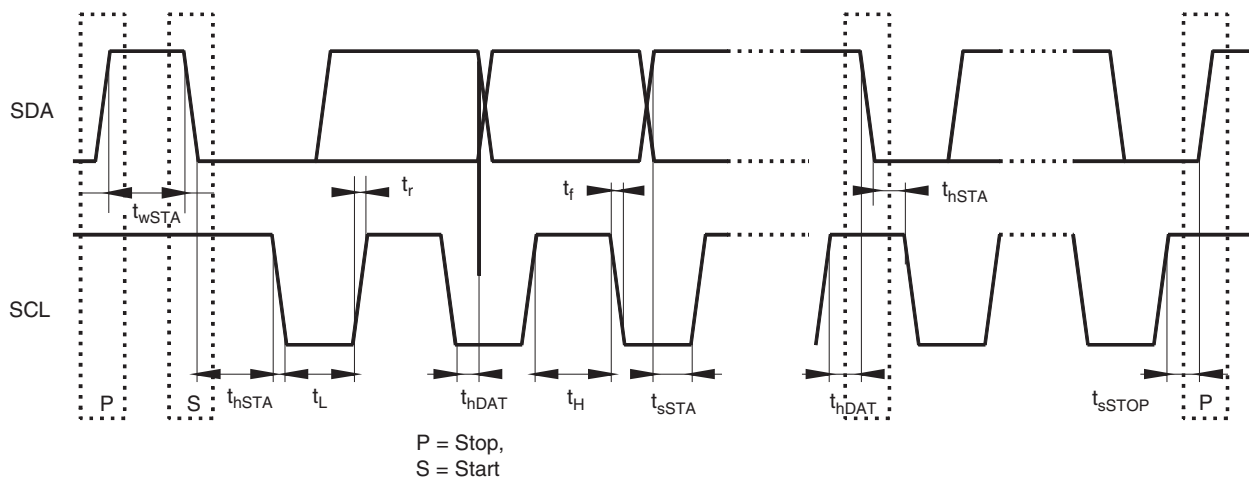




**Figure 6-4.** AM Input Sensitivity,  $T = -30^{\circ}\text{C}$



**Figure 6-5.** Bus Timing



## 7. Bit Organization

**Table 7-1.** Bit Organization

	MSB							LSB
Module address	1	1	0	0	1	0	0/1	0
	A7	A6	A5	A4	A3	A2	A1	A0
Subaddress (R-divider)	X	X	X	0	0	1	X	X
Subaddress (N-divider)	X	X	X	X	1	1	X	X
Data byte 0 (Status)	SWO1	SWO2	SWO3	SWO4	AM/FM	PD - ANA	PD - POL	PD - CUR
	D7	D6	D5	D4	D3	D2	D1	D0
Data byte 1	2 <sup>15</sup> R-divider							2 <sup>8</sup>
Data byte 2	2 <sup>7</sup> R-divider							2 <sup>0</sup>
Data byte 3	2 <sup>15</sup> N-divider							2 <sup>8</sup>
Data byte 4	2 <sup>7</sup> N-divider							2 <sup>0</sup>

**Table 7-2.** Function Mode

Bit Description	Mode	LOW	HIGH
D3	AM/FM	FM operation	AM operation
D2	PD - ANA	PD analog	Test
D1	PD - POL	Negative polarity	Positive polarity
D0	PD - CUR	Output current 2	Output current 1

## 8. Transmission Protocol

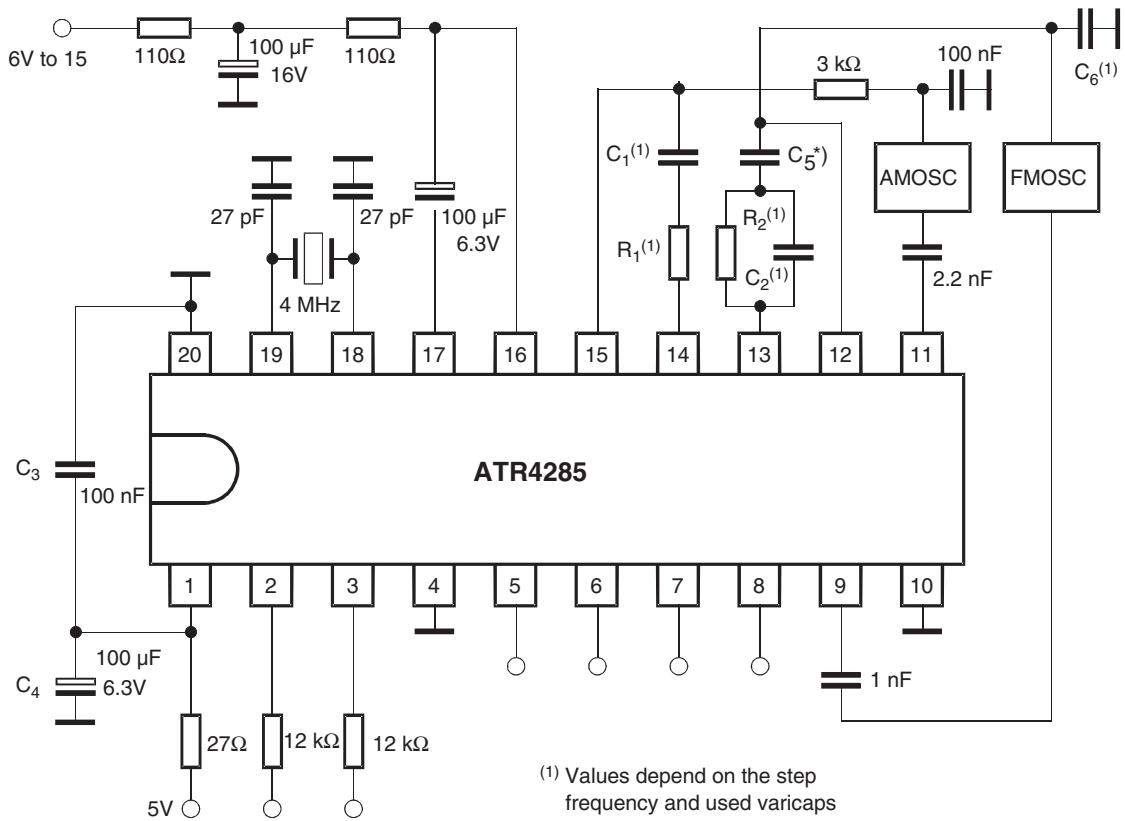
	MSB	LSB										
S	Address		A	Subaddress	A	Data 0	A	Data 1	A	Data 2	A	P
	A0	A7		R-divider								

	MSB	LSB									
S	Address		A	Subaddress	A	Data 3	A	Data 4	A	P	
	A0	A7		N-divider							

Note: S = Start, P = Stop, A = Acknowledge

## 9. Application

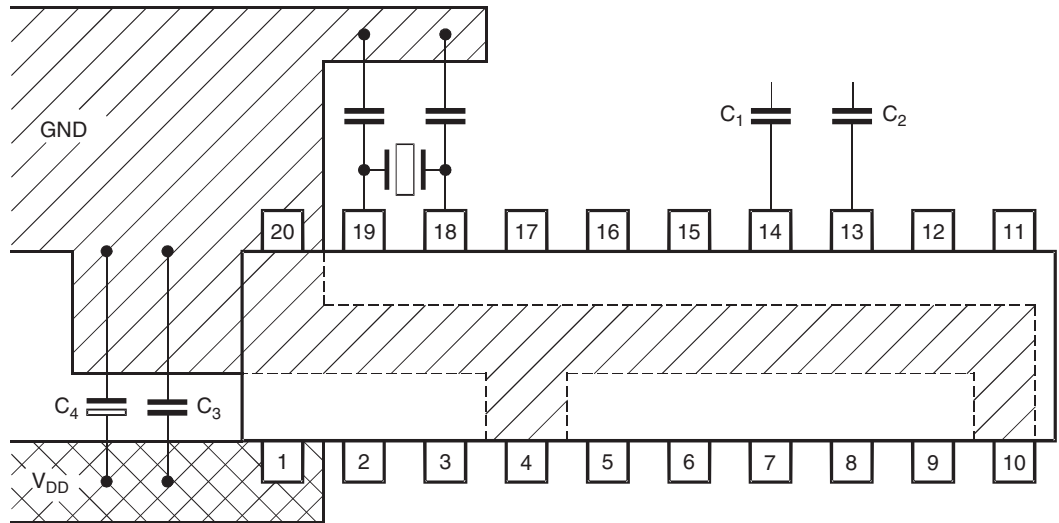
Figure 9-1. Application Circuit



### 9.1 Recommendations for Applications

- $C_3 = 100\text{ nF}$  should be very close to pin 1 ( $V_{DD}$ ) and pin 20 (GND 1)
- GND 2 (pin 10 — analog ground) and GND 1 (pin 20 — digital ground) must be connected according to [Figure 9-1](#)
- 4 MHz crystal must be very close to pin 18 and pin 19
- Components of the charge pump ( $C_1/R_1$  for AM and  $C_2/R_2$  for FM) should be very close to pin 14 with respect to pin 13

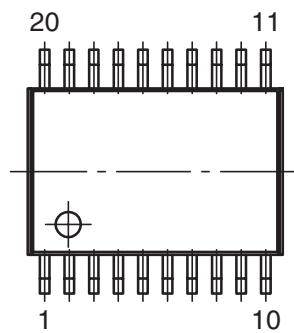
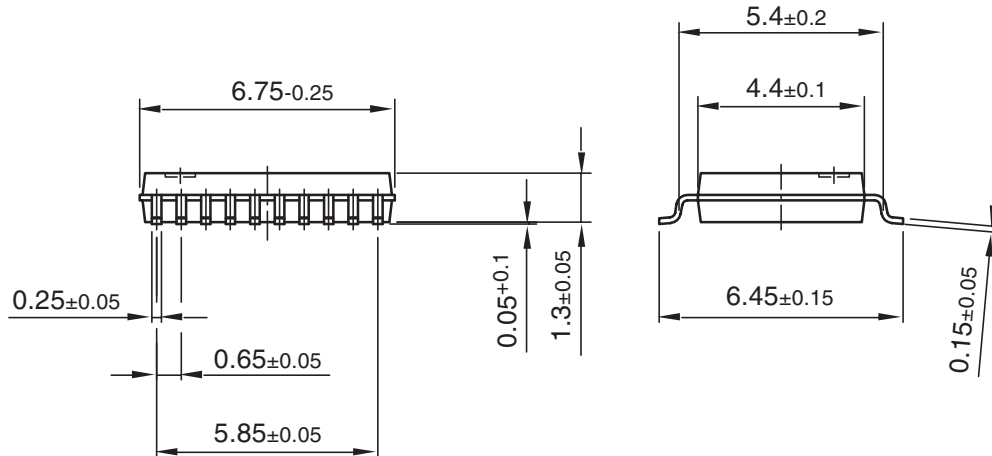
Figure 9-2. PCB Layout



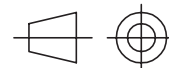
## 10. Ordering Information

Extended Type Number	Package	Remarks
ATR4285-TKSY	SSO20 plastic	Pb-free
ATR4285-TKQY	SSO20 plastic	Taping according to IEC-286-3, Pb-free

## 11. Package Information



Package: SSO20  
Dimensions in mm



technical drawings  
according to DIN  
specifications

Drawing-No.: 6.543-5056.01-4

Issue: 1; 10.03.04



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