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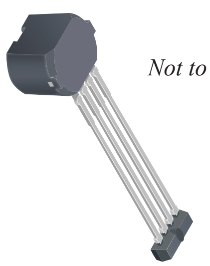
True Zero Speed, Low Jitter, High Accuracy Position Sensor IC

FEATURES AND BENEFITS

- Highly accurate in presence of:
  - □ Anomalous target geometry (tooth-tooth variation)
  - □ Signature teeth or valleys
  - □ Target runout
- Highly repeatable output edges (low jitter)
- True zero-speed operation
- Undervoltage lockout
- Air gap independent switchpoints
- Defined power-on state
- High operating temperature
- Single-chip sensing IC for high reliability
- Enhanced quality through Scan Path and IDDQ measurement
- Enhanced EMC performance

PACKAGE: 4-pin SIP (suffix SG)



Not to scale

DESCRIPTION

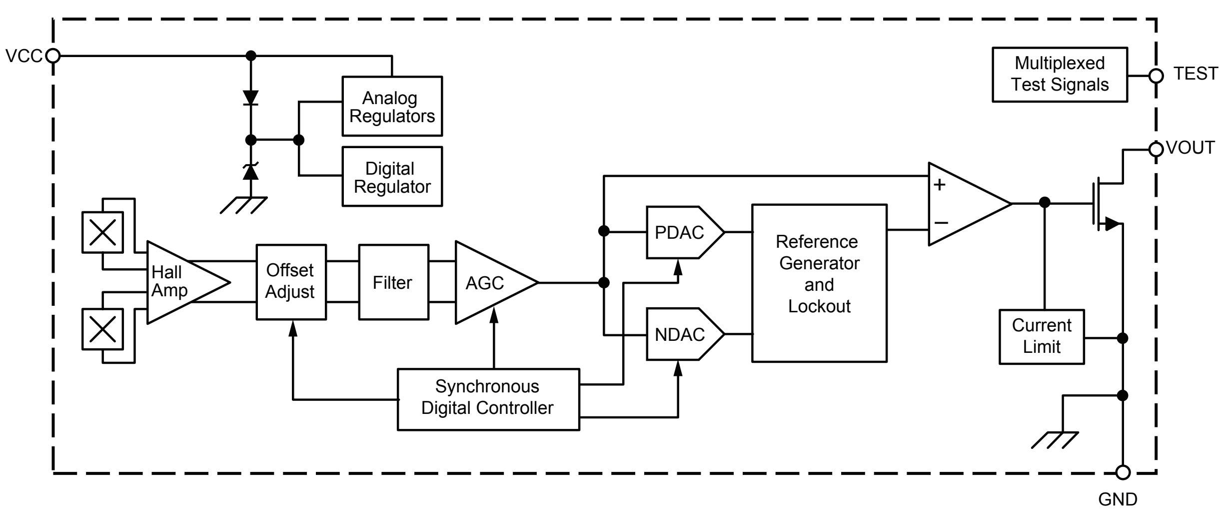
The ATS627 is a true zero-speed gear tooth sensor IC consisting of an optimized Hall IC and rare earth pellet configuration in a single overmolded package. The integrated circuit provides a manufacturer-friendly solution for digital gear tooth sensing applications. This small package can be easily assembled and used in conjunction with gears of various shapes and sizes.

The dual-element Hall IC switches in response to differential magnetic signals created by a ferrous target. Digital processing of the analog signal provides zero-speed performance independent of air gap as well as dynamic adaptation of device performance to the typical operating conditions found in automotive applications.

High-resolution peak detecting DACs are used to set the adaptive switching thresholds of the device. Bounded tracking and switchpoint hysteresis reduce the negative effects of any anomalies in the magnetic signal associated with the targets used in many automotive applications. This sensor IC system is optimized for engine crank applications that use targets possessing signature regions.

This device is available in a lead (Pb) free 4-pin SIP package (SG) with a 100% matte tin-plated leadframe.

Functional Block Diagram



SELECTION GUIDE

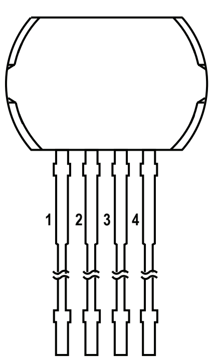
Part Number	Packing*
ATS627LSGTN-T	800 pieces per 13-in. reel

*Contact Allegro™ for additional packing options

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{CC}	Refer to Power Derating section	26.5	V
Output Off Voltage	V_{OUTOFF}		26.5	V
Reverse Supply Voltage	V_{RCC}		–18	V
Reverse Output Voltage	V_{ROUT}		–0.5	V
Output Current	$I_{OUTSINK}$		25	mA
Operating Ambient Temperature	T_A	L temperature range	–40 to 150	°C
Maximum Junction Temperature	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

Pinout Diagram



Terminal List Table

Number	Name	Function
1	VCC	Supply voltage
2	VOUT	Open drain output
3	TEST	Test pin
4	GND	Ground

OPERATING CHARACTERISTICS: Valid through full operating supply voltage and ambient temperature ranges, using Reference Target 60+2; unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
ELECTRICAL CHARACTERISTICS						
Supply Voltage [2]	V_{CC}	Operating, T_J < T_J(max)	4.0	–	24	V
Undervoltage Lockout	$V_{CC(UV)}$	V_{CC} = 0 → 5 V or 5 → 0 V	–	3.6	3.95	V
Reverse Supply Current [3]	I_{RCC}	V_{CC} = V_{RCC}(max)	–	–	–10	mA
Supply Zener Clamp Voltage	$V_{Zsupply}$	I_{CC} = I_{CC}(max) + 3 mA, T_A = 25°C	28	–	–	V
Supply Current	I_{CC}		–	7	12	mA
Test Pin Zener Clamp Voltage [4]	V_{ZTEST}		–	6	–	V
POWER-ON CHARACTERISTICS						
Power-On State	POS	V_{OUT}, IC connected as in figure 9	–	High	–	V
OUTPUT STAGE CHARACTERISTICS						
Low Output Voltage	$V_{OUT(SAT)}$	VOUT = On (V_{OUT} = low), I_{OUT} = 20 mA	0	–	450	mV
Output Zener Clamp Voltage	$V_{ZOUTPUT}$	I_{OUT} = 3 mA, T_A = 25°C	28	–	–	V
Output Leakage Current	$I_{OUT(OFF)}$	VOUT = Off (V_{OUT} = high)	–	–	10	μA
Output Current Limit	$I_{OUT(LIM)}$	VOUT = On (V_{OUT} = low), T_J < T_J(max)	25	45	70	mA
Output Rise Time	$t_{r(OUT)}$	V_{PU} = 12 V, R_{PU} = 1.0 kΩ, C_{LOAD} = 4.7 nF , see figure 1	–	10	–	μs
Output Fall Time	$t_{f(OUT)}$	V_{PU} = 12 V, R_{PU} = 1.0 kΩ, C_{LOAD} = 4.7 nF, see figure 1	–	0.6	2	μs
DAC CHARACTERISTICS						
Allowable User-Induced Offset [5]	$B_{DIFFEXT}$		–60	–	60	G
OTHER OPERATING CHARACTERISTICS, WITH CONTINUOUS UPDATE METHOD, BOUNDED FOR INCREASING AND DECREASING AG						
Running Mode Lockout Enable	LOE		–	115	–	mV
Running Mode Lockout Release	LOR		–	220	–	mV
Operate Point	B_{OP}	% of peak-to-peak V_{PROC}, referenced from PDAC to NDAC, V_{OUT} high → low	–	60	–	%
Release Point	B_{RP}	% of peak-to-peak V_{PROC}, referenced from PDAC to NDAC, V_{OUT} low → high	–	40	–	%
Bandwidth	f_{-3dB}	Cutoff frequency for low pass filter	–	20	–	kHz
Operational Speed	S_{ROT}		0	–	12 000	rpm
PERFORMANCE CHARACTERISTICS						
Operational Magnetic Range	B_{IN}	Peak-to-peak differential signal	30	–	1200	G
Air Gap	AG	Compliant to accuracy specifications, measured from package branded face to target tooth	0.5	–	2.5	mm
		No missed edges, measured from package branded face to target tooth	0.5	–	3.0	mm
Relative Timing Accuracy, Sequential Mechanical Rising Edges	ERR_{RR}	0.5 mm ≤ AG ≤ 2.5 mm; constant target speed, Running mode; relative to measurement taken at AG = 1.5 mm	–	–	±0.4	degrees

Continued on the next page…

OPERATING CHARACTERISTICS (continued): Valid through full operating supply voltage and ambient temperature ranges, using Reference Target 60+2; unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
PERFORMANCE CHARACTERISTICS (continued)						
Relative Timing Accuracy, Sequential Mechanical Falling Edges	ERR_{FF}	0.5 mm ≤ AG ≤ 2.5 mm; constant target speed, Running mode; relative to measurement taken at AG = 1.5 mm	–	–	±0.4	degrees
Relative Timing Accuracy, Signature Mechanical Rising Edge	ERR_{SIGR}	0.5 mm ≤ AG ≤ 2.5 mm; constant target speed, Running mode; relative to measurement taken at AG = 1.5 mm	–	–	±0.4	degrees
Relative Timing Accuracy, Signature Mechanical Falling Edge	ERR_{SIGF}	0.5 mm ≤ AG ≤ 2.5 mm; constant target speed, Running mode; relative to measurement taken at AG = 1.5 mm	–	–	±1.5	degrees
Relative Repeatability, Sequential Rising and Falling Edges [6]	$T_{\Theta E}$	0.5 mm ≤ AG ≤ 2.5 mm	–	–	0.08	degrees
Output Propagation Delay	$t_{d(OUT)}$	See figure 1	–	20	–	μs
INITIAL EDGE ACCURACY [7]						
Edge Accuracy – First and Second Output Edges		See figure 2	$-T_{TARGET}$	–	T_{TARGET}	degrees
Edge Accuracy – Third through Sixth Output Edges		See figure 2	$-0.5 \times T_{TARGET}$	–	$+0.5 \times T_{TARGET}$	degrees
Full Edge Accuracy		Output edge count (see figure 2), B_{SIG}/B_{SEQ} = 1, or no signature tooth encountered	–	–	6	–
		Output edge count (see figure 2), signature region encountered during calibration, and $B_{SIG}/B_{SEQ} \neq 1$	–	9	–	–
INPUT MAGNETIC CHARACTERISTICS						
Allowable Differential Sequential Signal Variation [8]	$B_{SEQ(min)}$ / $B_{SEQ(max)}$	Total variation over 60 cycles (see figure 3)	0.5	–	–	–
	$B_{SEQ(n+1)}$ / $B_{SEQ(n)}$	Single cycle-to-cycle variation (see figure 3)	0.6	–	–	–
Allowable Signature Amplitude Ratio	B_{SIG} / B_{SEQ}	One instance per target revolution (see figure 3)	0.8	–	1.6	–

[1] Typical values are at T_A = 25°C and V_{CC} = 12 V.
[2] Maximum voltage must be adjusted for power dissipation and junction temperature; see Power Derating section.
[3] Negative current is defined as current coming out of (sourced from) the specified device terminal.
[4] Sustained voltages beyond the clamp voltage may cause permanent damage to the IC.
[5] 1 G (gauss) = 0.1 mT (millitesla).
[6] The repeatability specification is based on statistical evaluation of a sample population, evaluated at 1000 Hz.
[7] Power-on frequencies ≤ 200 Hz. Higher power-on frequencies may result in a delay of full output accuracy or undetected target edges.
[8] Excludes effects caused by signature region.

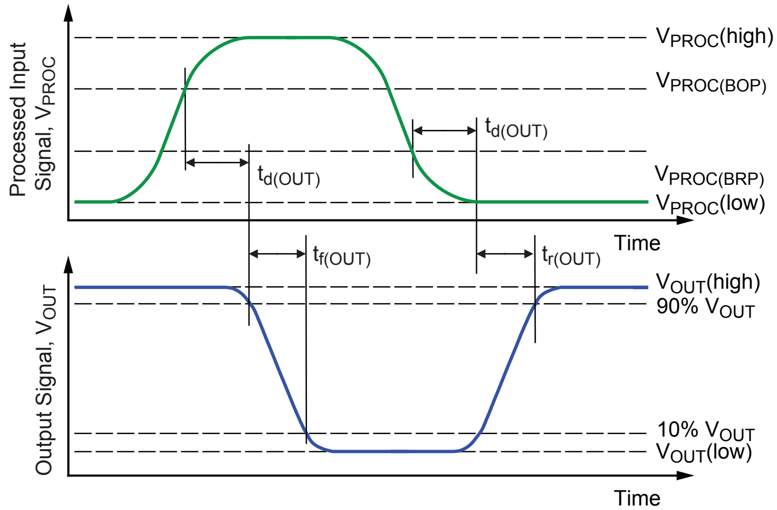
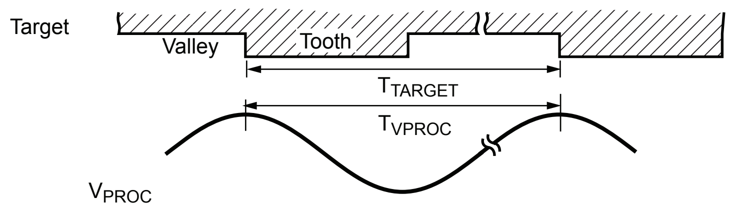


Figure 1. Definition of Output Delay Time, $t_{d(OUT)}$, Output Fall Time, $t_{f(OUT)}$, and Output Rise Time, $t_{r(OUT)}$.



V_{PROC} = the processed analog signal of the sinusoidal magnetic input (per channel)
T_{TARGET} = period between successive sensed target mechanical edges of the same orientation (either both rising or both falling)

Figure 2. Definition of T_{TARGET}

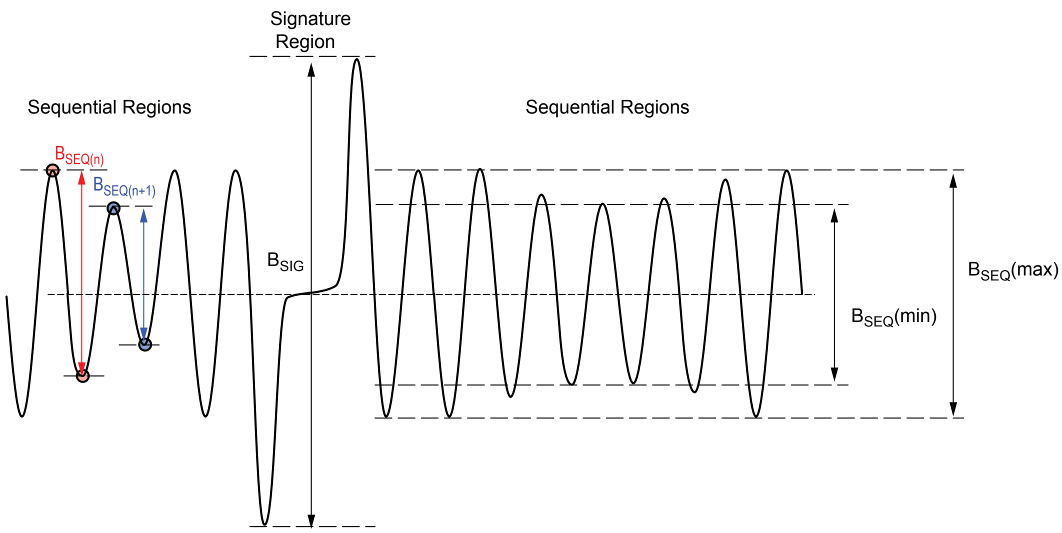
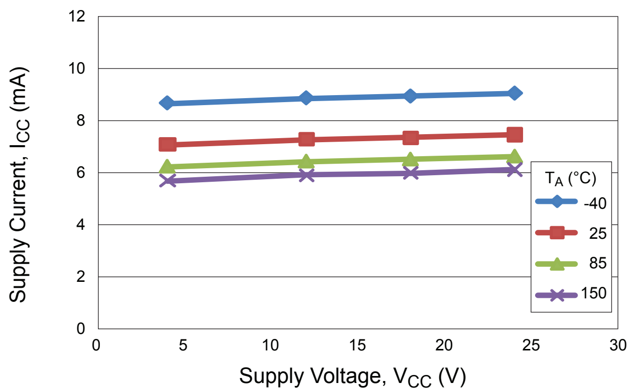


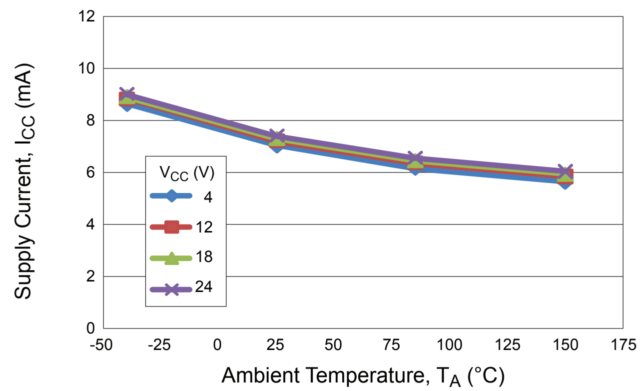
Figure 3. Differential signature amplification and sequential signal variation

CHARACTERISTIC PERFORMANCE

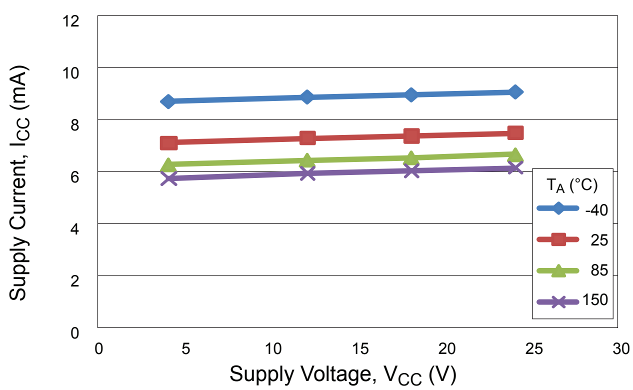
Supply Current (On) versus Supply Voltage



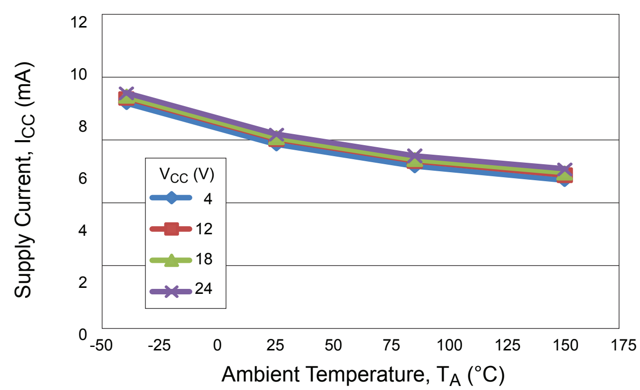
Supply Current (On) versus Temperature



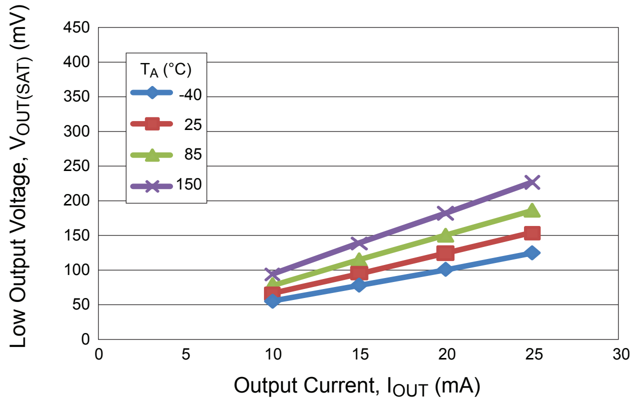
Supply Current (Off) versus Supply Voltage



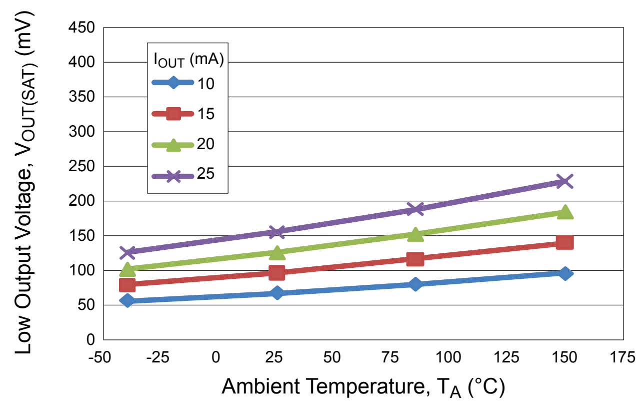
Supply Current (Off) versus Temperature



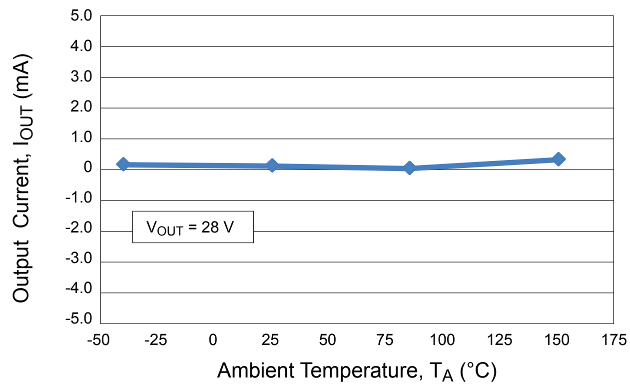
Output Voltage (On) versus Output Current



Output Voltage (On) versus Temperature

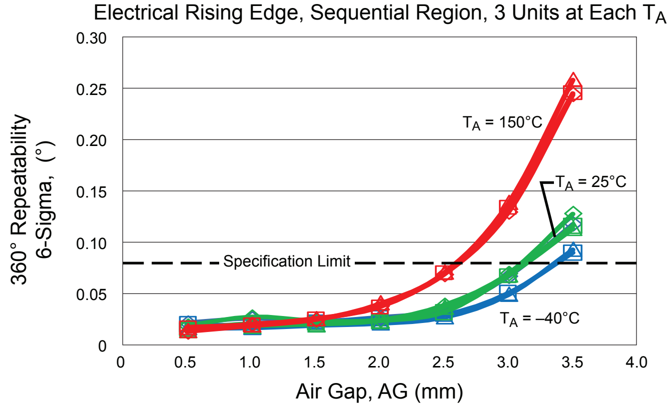


Output Current (Off) versus Temperature



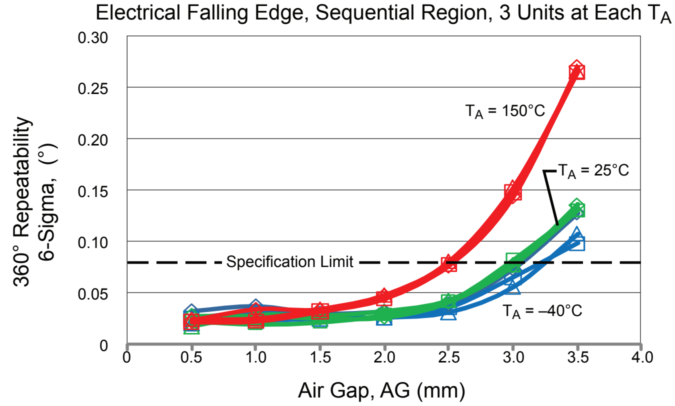
360° Repeatability versus Air Gap

Electrical Rising Edge, Sequential Region, 3 Units at Each T_A

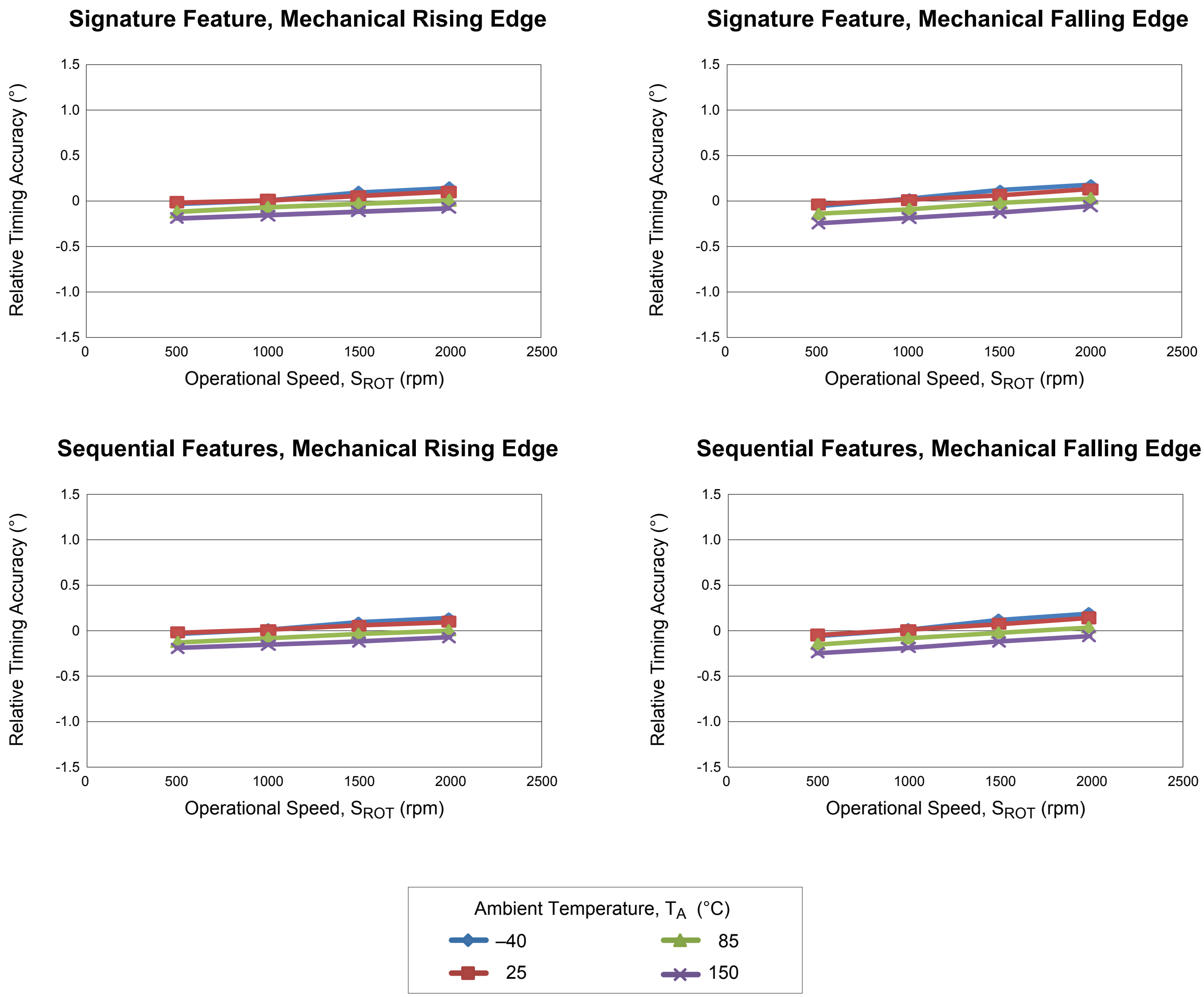


360° Repeatability versus Air Gap

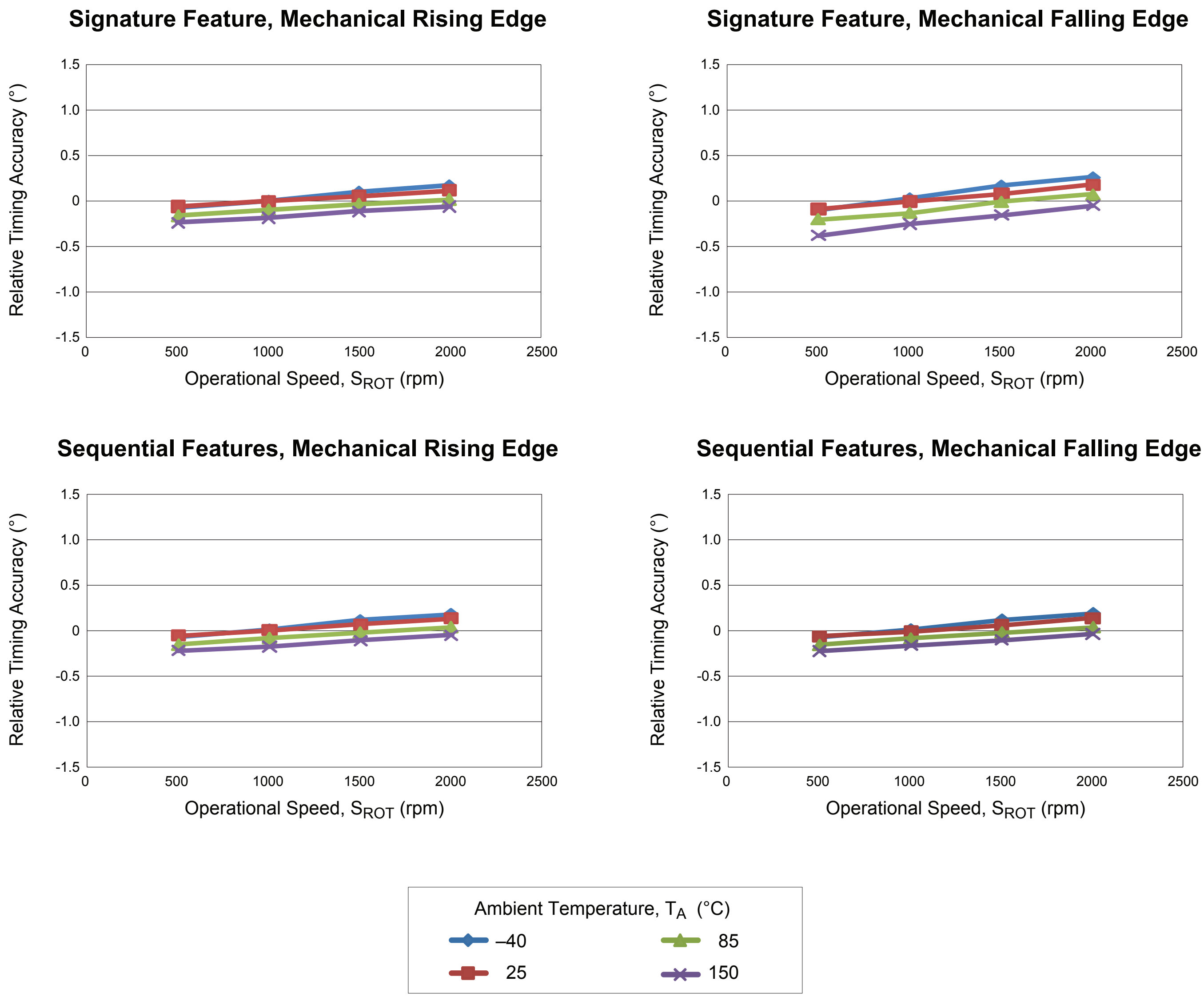
Electrical Falling Edge, Sequential Region, 3 Units at Each T_A



Timing Accuracy versus Operational Speed
AG = 0.5 mm; relative to T_A = 25°C, S_{ROT} = 1000 rpm



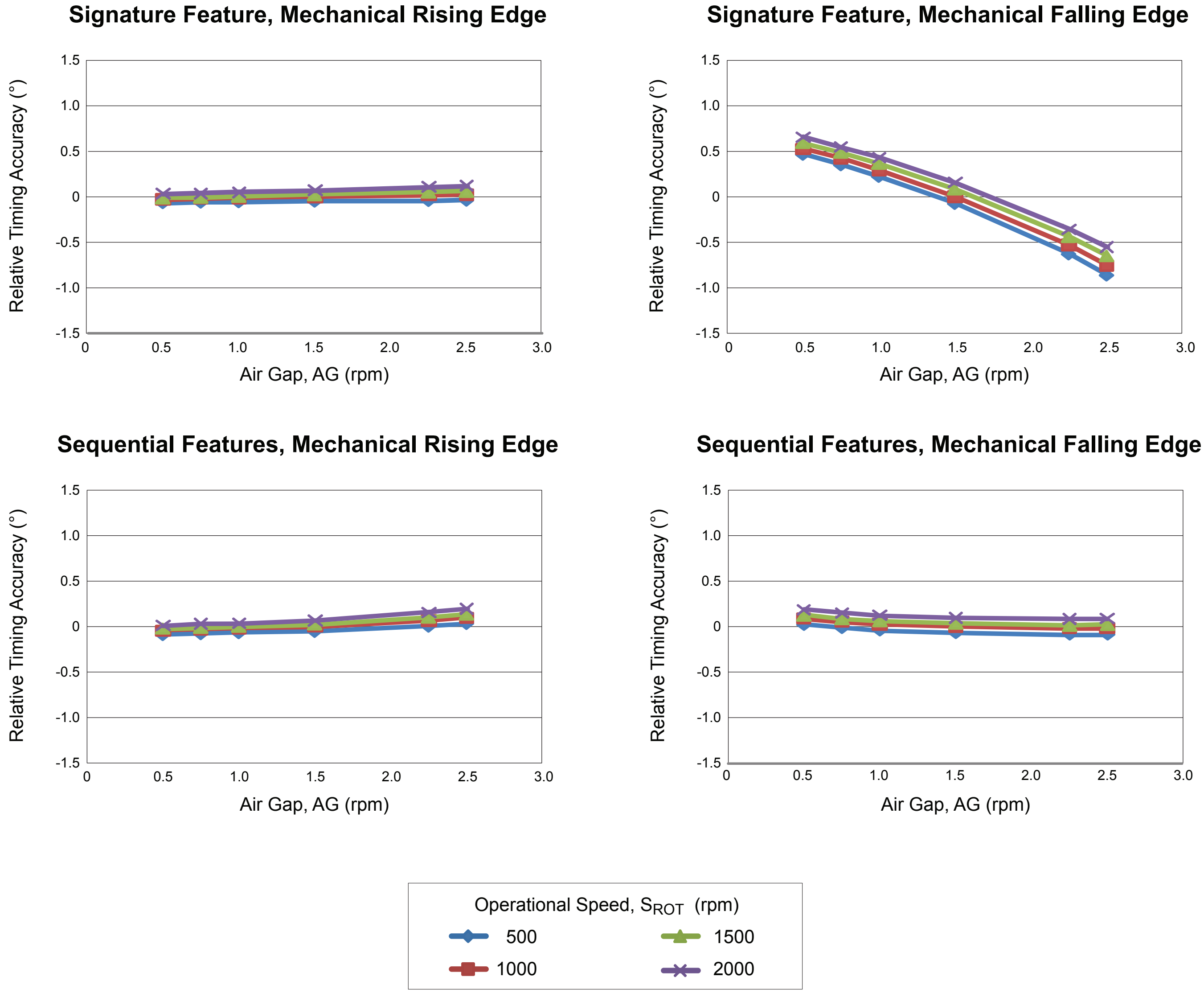
Timing Accuracy versus Operational Speed
AG = 2.5 mm; relative to T_A = 25°C, S_{ROT} = 1000 rpm



Allegro MicroSystems, LLC
115 Northeast Cutoff
Worcester, Massachusetts 01615-0036 U.S.A.
1.508.853.5000; www.allegromicro.com

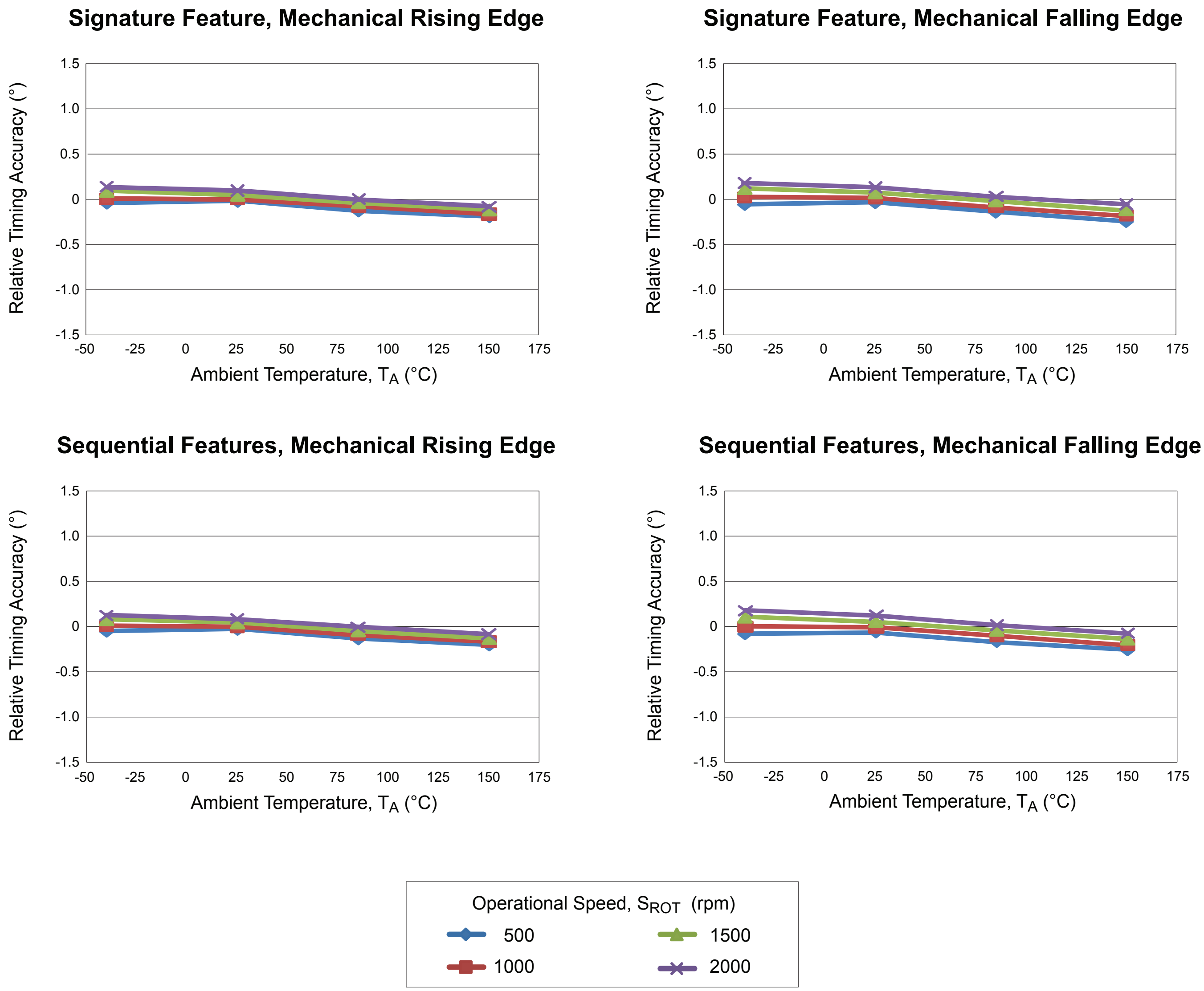
Timing Accuracy versus Air Gap

T_A = 25°C; relative to AG = 1.5 mm, S_{ROT} = 1000 rpm

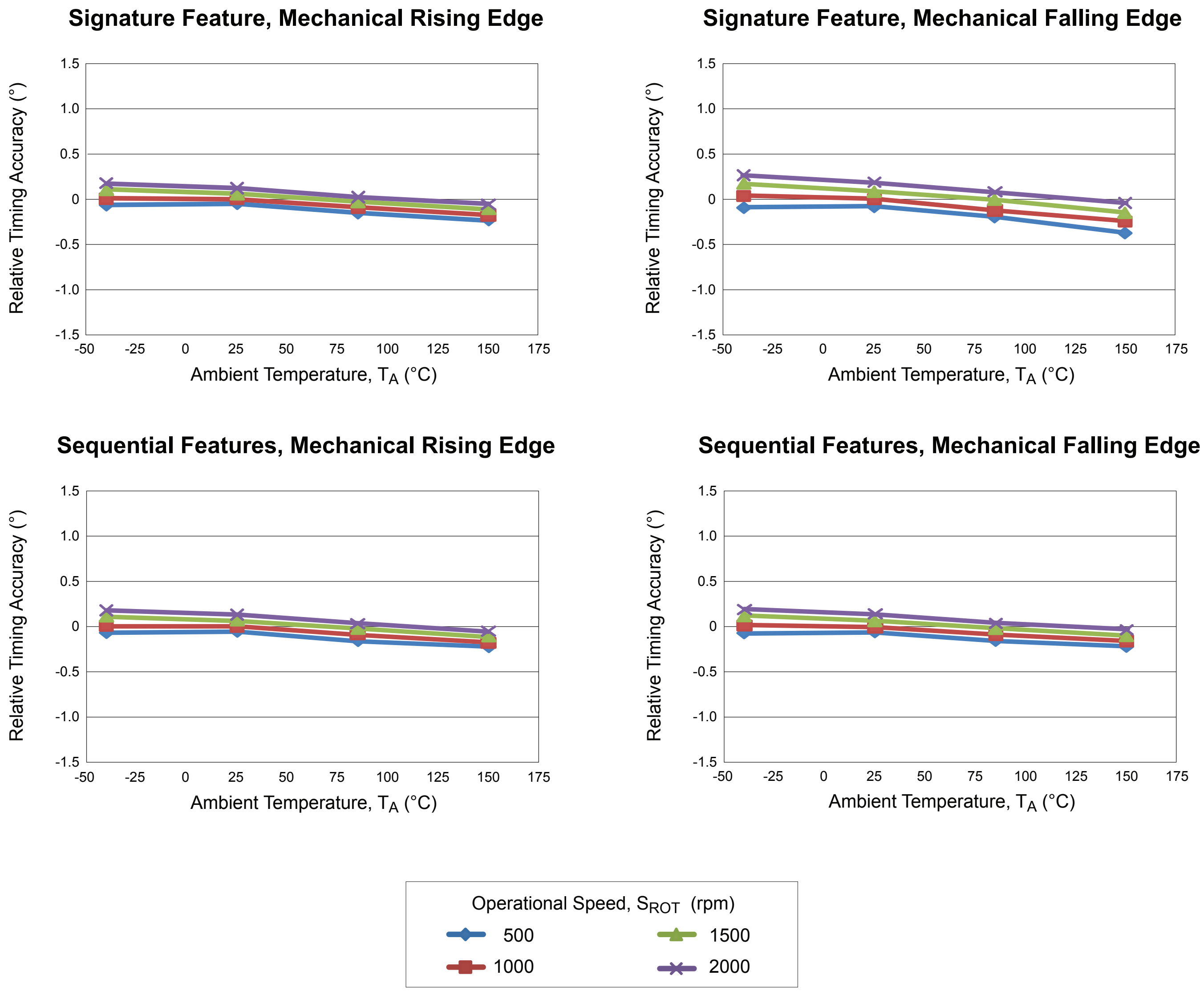


Timing Accuracy versus Ambient Temperature

AG = 0.5 mm; relative to T_A = 25°C, S_{ROT} = 1000 rpm



Timing Accuracy versus Ambient Temperature
AG = 2.5 mm; relative to T_A = 25°C, S_{ROT} = 1000 rpm



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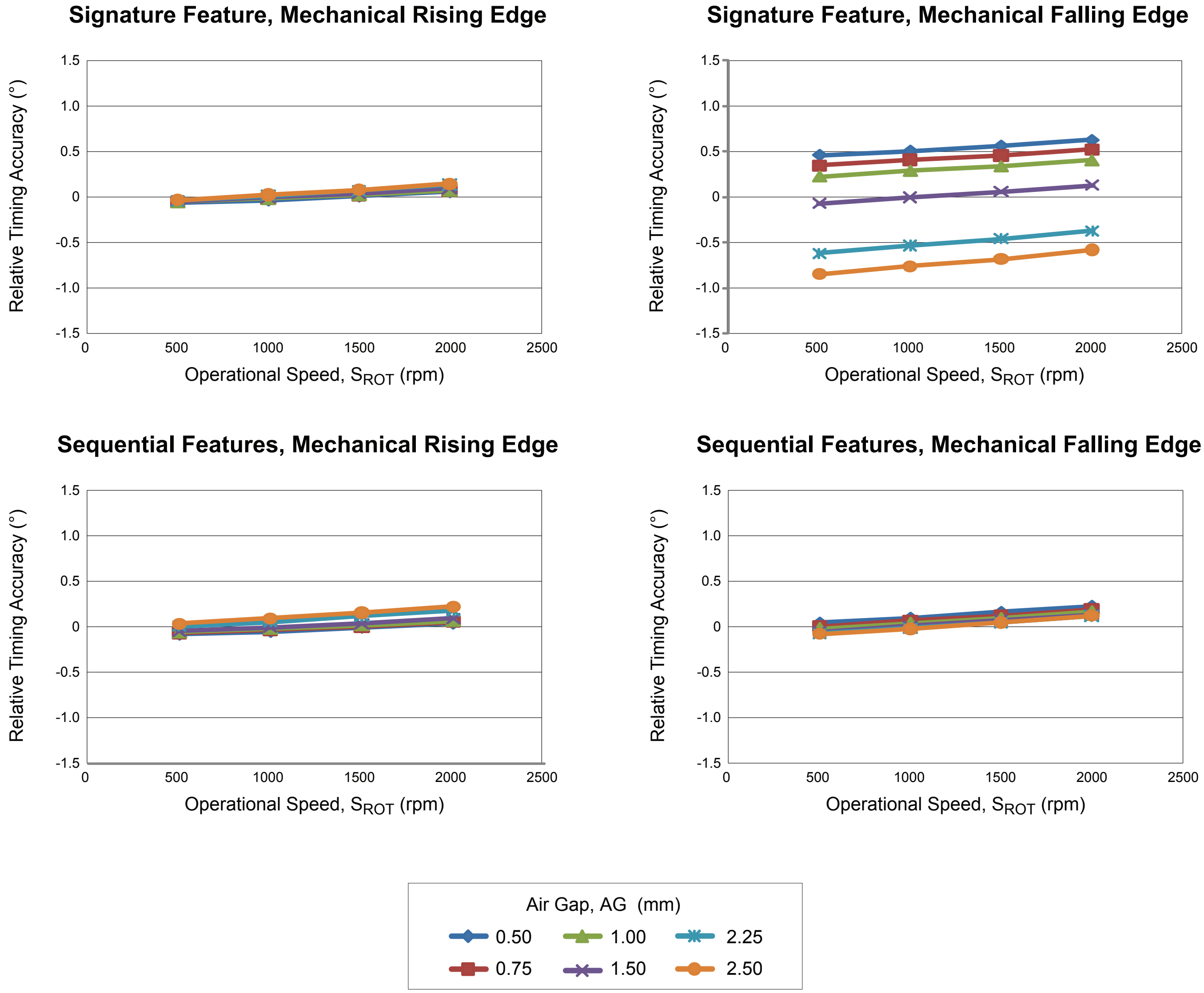
1.508.853.5000; www.allegromicro.com

Timing Accuracy versus Operational Speed

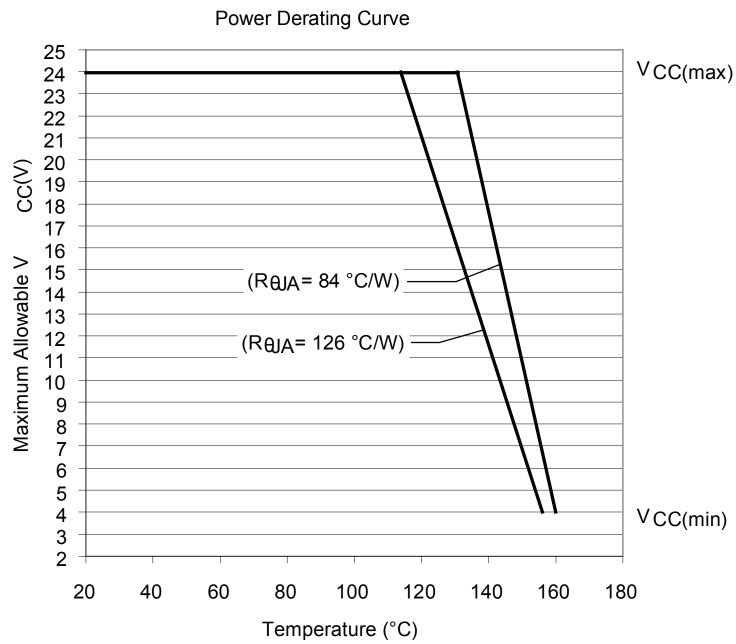
T_A = 25°C; relative to AG = 1.5 mm, S_{ROT} = 1000 rpm

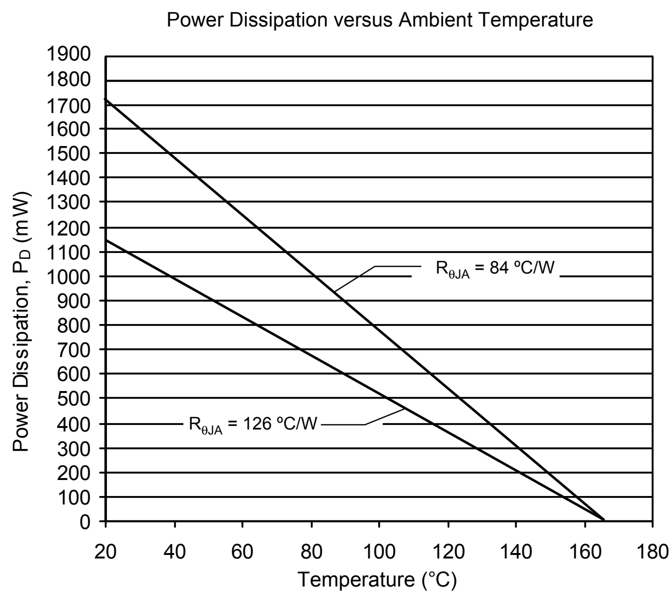


THERMAL CHARACTERISTICS: May require derating at maximum conditions; see Power Derating section

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	Single layer PCB, with copper limited to solder pads	126	°C/W
		Single layer PCB, with copper limited to solder pads and 3.57 in.^{2} (23.03 cm^2) copper area each side	84	°C/W

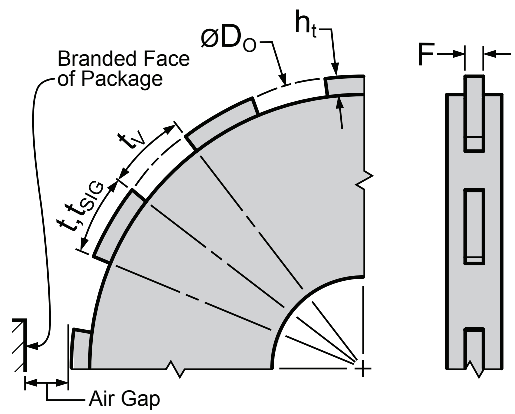
*Additional thermal information available on the Allegro website

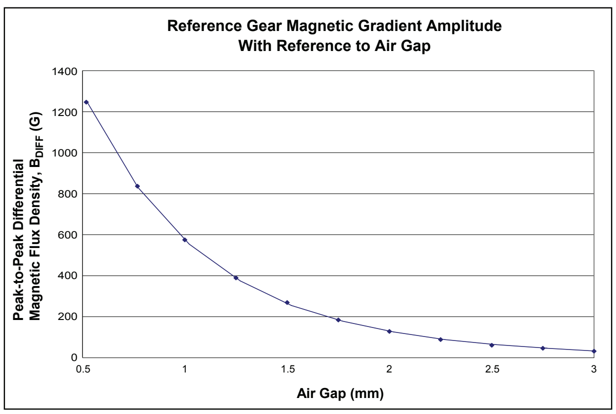


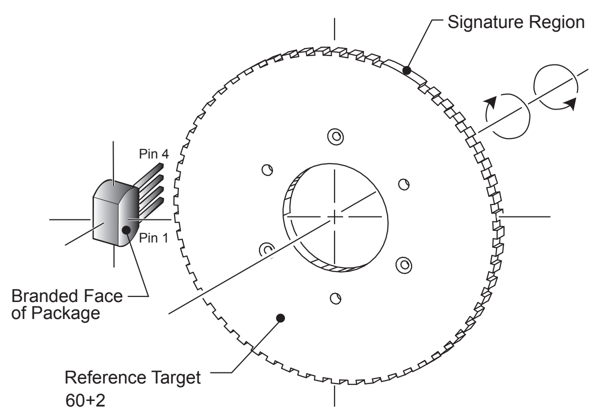


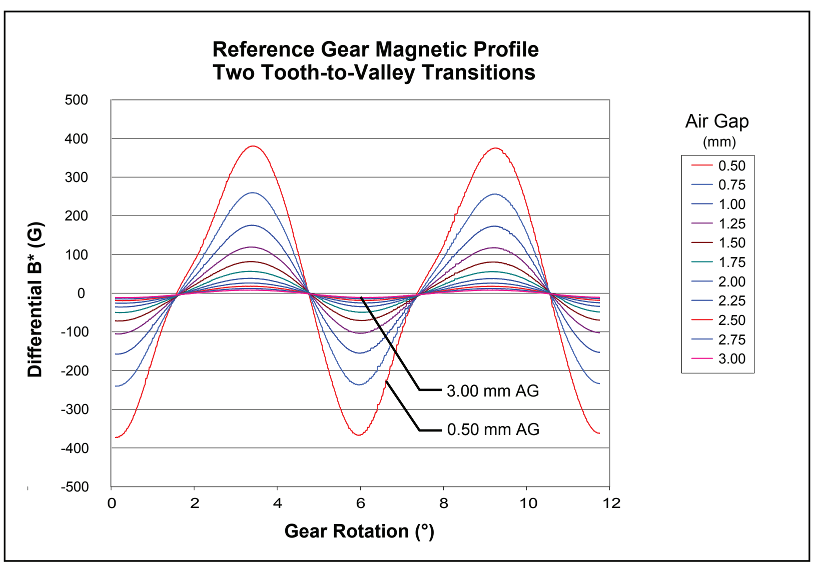
Reference Target Characteristics

Reference Target 60+2

Characteristics	Symbol	Test Conditions	Typ.	Unit	Symbol Key
Outside Diameter	D_o	Outside diameter of target	120	mm	
Face Width	F	Breadth of tooth, with respect to branded face	6	mm	
Angular Tooth Thickness	t	Length of tooth, with respect to branded face; measured at D_o	3	degrees	
Signature Region Angular Tooth Thickness	t_{SIG}	Length of signature tooth, with respect to branded face; measured at D_o	15	degrees	
Angular Valley Thickness	t_v	Length of valley, with respect to branded face; measured at D_o	3	degrees	
Tooth Whole Depth	h_t		3	mm	
Material		Low Carbon Steel	–	–	







FUNCTIONAL DESCRIPTION

Sensing Technology

The ATS627 contains a single-chip differential Hall-effect sensor IC, a samarium cobalt pellet, and a flat ferrous pole piece (concentrator). As shown in figure 5, the Hall IC supports two Hall elements, which sense the magnetic profile of the ferrous gear target simultaneously, but at different points (spaced at a 2.2 mm pitch), generating a differential internal analog voltage, V_{PROC}, that is processed for precise switching of the digital output signal.

The Hall IC is self-calibrating and also possesses a temperature-compensated amplifier and offset cancellation circuitry. The built-in voltage regulator provides supply noise rejection throughout the operating voltage range. Changes in temperature do not greatly affect this device due to the stable amplifier design and the offset compensation circuitry. The Hall transducers and signal processing electronics are integrated on the same silicon substrate, using a proprietary BiCMOS process.

Target Profiling During Operation

An operating device is capable of providing digital information that is representative of the mechanical features of a rotating gear. The waveform diagram in figure 7 presents the automatic translation of the mechanical profile, through the magnetic profile that it induces, to the digital output signal of the ATS627. No additional optimization is needed and minimal processing circuitry is required. This ease of use reduces design time and incremental assembly costs for most applications.

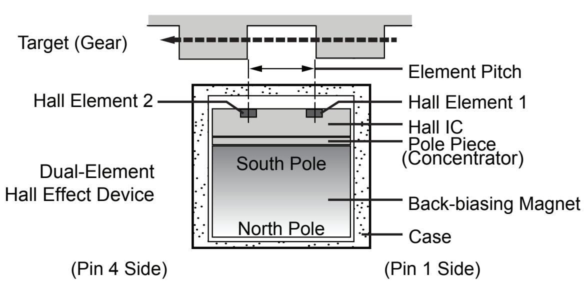


Figure 5. Relative motion of the target is detected by the dual Hall elements in the Hall IC.

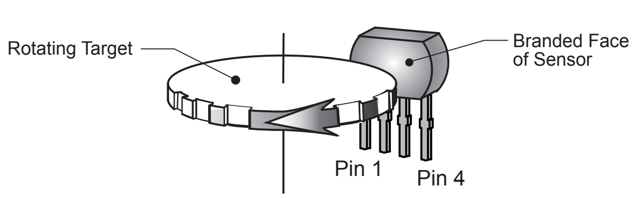


Figure 6. This left-to-right (pin 1 to pin 4) direction of target rotation results in a high output state when a tooth of the target gear is nearest the package face (see figure 3). A right-to-left (pin 4 to pin 1) rotation inverts the output signal polarity.

Determining Output Signal Polarity

In figure 7, the top panel, labeled Mechanical Position, represents the mechanical features of the target gear and orientation to the device. The bottom panel, labeled Device Output Signal, displays the square waveform corresponding to the digital output signal that results from a rotating gear configured as shown in figure 6, and electrically connected as in figure 9. That direction of rotation (of the gear side adjacent to the package face) is: perpendicular to the leads, across the face of the device, from the pin 1 side to the pin 4 side. This results in the IC output switching from low state to high state as the leading edge of a tooth (a rising mechanical edge, as detected by the IC) passes the package face. In this configuration, the device output switches to its high polarity when a tooth is the target feature nearest to the package. If the direction of rotation is reversed so that the gear rotates from the pin 4 side to the pin 1 side, the output polarity inverts; that is, the output signal goes high when a falling edge is detected and a valley is nearest to the package.

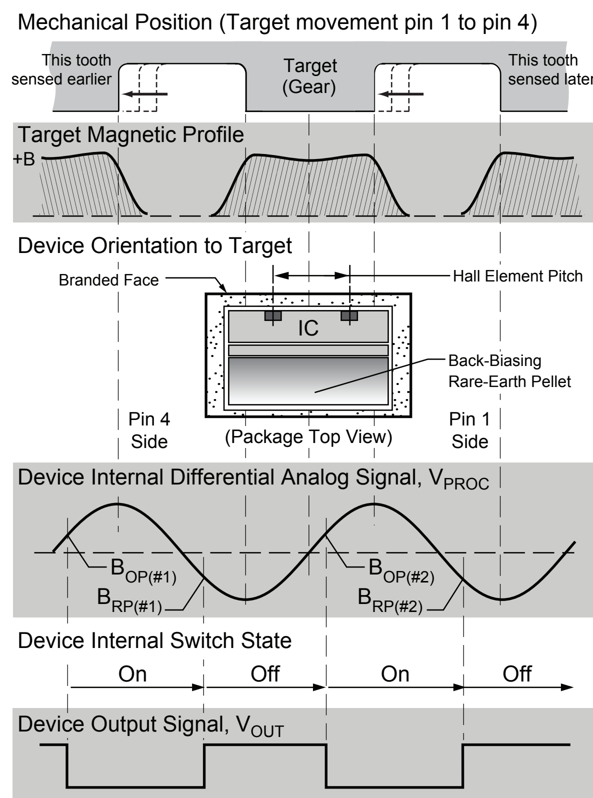


Figure 7: The magnetic profile reflects the geometry of the target, allowing the ATS627 to present an accurate digital output response.

Undervoltage Lockout

When the supply voltage falls below the undervoltage lockout voltage, $V_{CC(UV)}$, the device enters Reset, where the output state returns to the Power-On State (POS) until sufficient V_{CC} is supplied. This lockout feature prevents false signals, caused by undervoltage conditions, from propagating to the output of the IC.

Power Supply Protection

The device contains an on-chip regulator and can operate over a wide V_{CC} range. For devices that must operate from an unregulated power supply, transient protection must be added externally. For applications using a regulated line, EMI/RFI protection may still be required. Contact Allegro for information on the circuitry needed for compliance with various EMC specifications. Refer to figure 9 for an example of a basic application circuit.

Automatic Gain Control (AGC)

This feature allows the device to operate with an optimal internal electrical signal, regardless of the air gap (within the AG specification). At power-on, the device determines the peak-to-peak amplitude of the signal generated by the target.

This feature is also active in Running mode, though very conservatively invoked, to optimize the signal amplitude in the scenario where signal amplitude during the initial calibration period is not representative of the Running mode signal.

Automatic Offset Adjust (AOA)

The AOA circuitry automatically compensates for the effects of chip, magnet, and installation offsets. This circuitry is continuously active, including during both Power-on mode and Running mode, compensating for any offset drift (within the Allowable User-Induced Differential Offset). Continuous operation also allows it to compensate for offsets induced by temperature variations over time. This circuitry works with the AGC during calibration to adjust V_{PROC} in the internal range to allow the DACs to acquire the signal peaks.

Bounded Update

The ATS627 continuously updates its switchpoints based on the actual signal being received from the target. When the output switches, the sensor resets the tracking DACs so that each proper magnetic signal peak can be acquired. To prevent establishing switchpoints on outlier signal maxima, tracking is limited, or bounded, in magnitude. If such limiting were not applied, then anomalous target features, such as bent, broken, or misformed teeth, could create significant output accuracy errors (see figure 8).

Running Mode Lockout

The ATS627 has a Running mode lockout feature to prevent switching in response to small amplitude input signals that are characteristic of vibration signals. The internal logic of the chip interprets small signal amplitudes below a certain level to be the result of target vibration. The output is held to the state present prior to lockout, until the amplitude of the signal returns to normal operational levels.

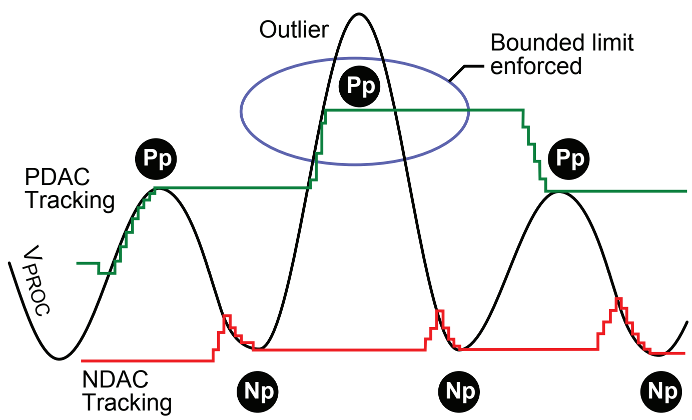


Figure 8. Operation of Bounded Update method (for illustrative purposes only, values may not be to scale)

- Two DACs track the V_{PROC} signal: PDAC tracks positive (high) peaks, and NDAC tracks negative (low) peaks.
- The DACs track the V_{PROC} signal until a peak is reached or the bounding limit is reached. Successive Pp and Np values are used to establish the next switchpoint.

APPLICATION INFORMATION

Power Derating

The device must be operated below the maximum junction temperature of the device, T_J(max). Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems website.)

The Package Thermal Resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is a relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as: T_A= 25°C, V_{CC} = 12 V, I_{CC} = 7 mA, and $R_{\theta JA}$ = 126 °C/W, then:

$$P_D = V_{CC} \times I_{CC} = 12\ V \times 7\ mA = 84\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 84\ mW \times 126\ °C/W = 10.6°C$$

$$T_J = T_A + \Delta T = 25°C + 10.6°C = 35.6°C$$

A worst-case estimate, P_D(max), represents the maximum allowable power level (V_{CC}(max), I_{CC}(max)), without exceeding T_J(max), at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{CC} at T_A=150°C, package SG, using single layer PCB.

Observe the worst-case ratings for the device, specifically: $R_{\theta JA}$=126°C/W, T_J(max)=165°C, $V_{CC(absmax)}$=24 V, and I_{CC} = 12 mA.

Calculate the maximum allowable power level, P_D(max). First, invert equation 3:

$$\Delta T(max) = T_J(max) - T_A = 165°C - 150°C = 15°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_D(max) = \Delta T(max) \div R_{\theta JA} = 15°C \div 126°C/W = 119\ mW$$

Finally, invert equation 1 with respect to voltage:

$$V_{CC(est)} = P_D(max) \div I_{CC} = 119\ mW \div 12\ mA = 9.9\ V$$

The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages $\leq V_{CC(est)}$.

Compare $V_{CC(est)}$ to V_{CC}(max). If $V_{CC(est)} \leq V_{CC}$(max), then reliable operation between $V_{CC(est)}$ and V_{CC}(max) requires enhanced $R_{\theta JA}$. If $V_{CC(est)} \geq V_{CC(max)}$, then operation between $V_{CC(est)}$ and V_{CC}(max) is reliable under these conditions.

Typical Application

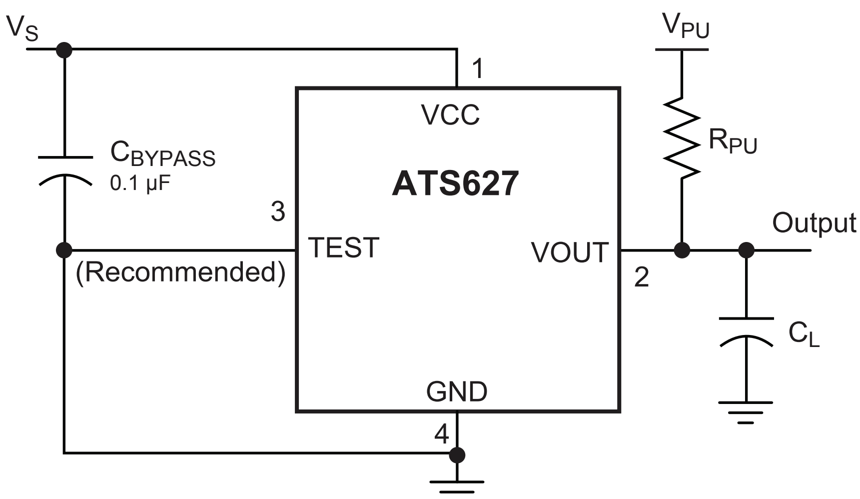
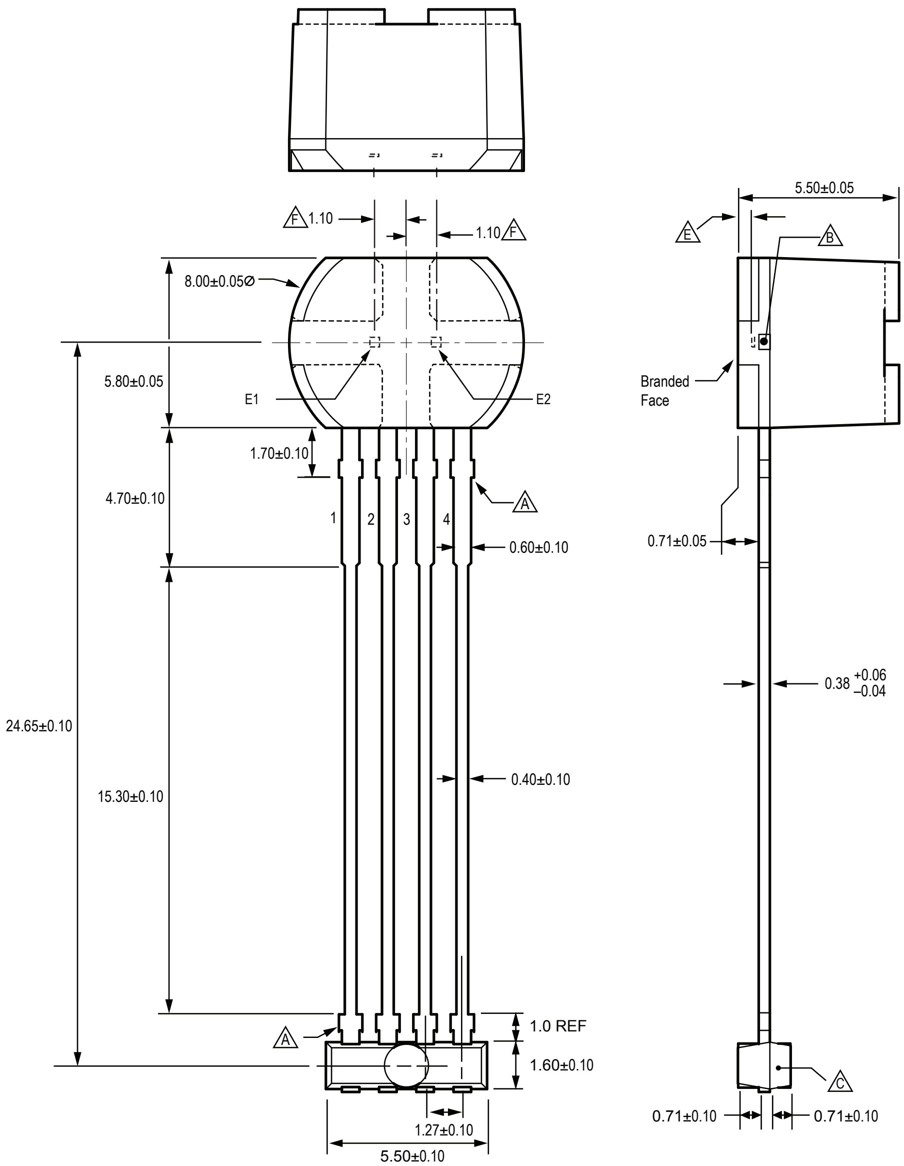
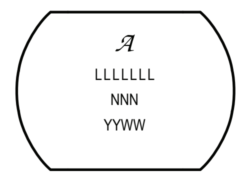


Figure 9. Basic typical application circuit

Package SG, 4-Pin SIP





D Standard Branding Reference View

- A = Supplier emblem
- L = Lot identifier
- N = Last three numbers of device part number
- Y = Last two digits of year of manufacture
- W = Week of manufacture

For Reference Only, not for tooling use (reference DWG-9002)
Dimensions in millimeters

- A Dambar removal protrusion (16X)
- B Metallic protrusion, electrically connected to pin 4 and substrate (both sides)
- C Molded Lead Bar for alignment during shipment
- D Branding scale and appearance at supplier discretion
- E Active Area Depth, 0.43 mm
- F Hall elements (E1, E2), not to scale

Revision History

Number	Date	Description
1	August 8, 2011	Add t_r and t_f definition, update derating example
2	December 12, 2017	Updated graph titles and subtitles (p. 7-13)

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