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SAM3S

Atmel | SMART ARM-based Flash MCU

DATASHEET

Description

The Atmel® | SMART SAM3S series is a member of a family of Flash microcontrollers based on the high performance 32-bit ARM® Cortex®-M3 processor. It operates at a maximum speed of 64 MHz and features up to 256 Kbytes of Flash and up to 48 Kbytes of SRAM. The peripheral set includes a Full Speed USB Device port with embedded transceiver, a High Speed MCI for SDIO/SD/MMC, an External Bus Interface featuring a Static Memory Controller providing connection to SRAM, PSRAM, NOR Flash, LCD Module and NAND Flash, 2x USARTs, 2x UARTs, 2x TWIs, 3x SPI, an I2S, as well as 1 PWM timer, two 3-channel general-purpose 16-bit timers an RTC, an ADC, a 12-bit DAC and an analog comparator.

The SAM3S device is a medium range general purpose microcontroller with the best ratio in terms of reduced power consumption, processing power and peripheral set. This enables the SAM3S to sustain a wide range of applications including consumer, industrial control, and PC peripherals.

It operates from 1.62V to 3.6V and is available in 48-, 64- and 100-pin QFP, 48- and 64-pin QFN, and 100-pin TFBGA packages.

The SAM3S series is the ideal migration path from the SAM7S series for applications that require more performance.The SAM3S series is pin-to-pin compatible with the SAM3N, SAM4S series (64- and 100-pin versions) and SAM7S series (64-pin versions).

Features

- Core
  - ARM® Cortex®-M3 revision 2.0 running at up to 64 MHz
  - Memory Protection Unit (MPU)
  - Thumb®-2 instruction set
- Pin-to-pin compatible with AT91SAM7S series (48- and 64-pin versions)
- Memories
  - From 64 to 256 Kbytes embedded Flash, 128-bit wide access, memory accelerator, single plane
  - From 16 to 48 Kbytes embedded SRAM
  - 16 Kbytes ROM with embedded bootloader routines (UART, USB) and IAP routines
  - 8-bit Static Memory Controller (SMC): SRAM, PSRAM, NOR and NAND Flash support
  - Memory Protection Unit (MPU)
- System
  - Embedded voltage regulator for single supply operation
  - Power-on-Reset (POR), Brown-out Detector (BOD) and Watchdog for safe operation
  - Quartz or ceramic resonator oscillators: 3 to 20 MHz main power with Failure Detection and optional low power 32.768 kHz for RTC or device clock
  - High precision 8/12 MHz factory trimmed internal RC oscillator with 4 MHz default frequency for device startup. In-application trimming access for frequency adjustment
  - Slow Clock Internal RC oscillator as permanent low-power mode device clock
  - Two PLLs up to 130 MHz for device clock and for USB
  - Temperature Sensor
  - Up to 22 peripheral DMA (PDC) channels
- Low Power Modes
  - Sleep and Backup modes, down to 1.8 µA in Backup mode
  - Ultra low power RTC
- Peripherals
  - USB 2.0 Device: 12 Mbps, 2668 byte FIFO, up to 8 bidirectional Endpoints. On-Chip Transceiver
  - Up to 2 USARTs with ISO7816, IrDA®, RS-485, SPI, Manchester and Modem Mode
  - Two 2-wire UARTs
  - Up to 2 Two Wire Interface (I2C compatible), 1 SPI, 1 Serial Synchronous Controller (I2S), 1 High Speed Multimedia Card Interface (SDIO/SD Card/MMC)
  - Up to two 3-channel 16-bit Timer Counters with capture, waveform, compare and PWM mode. Quadrature Decoder Logic and 2-bit Gray Up/Down Counter for Stepper Motor
  - 4-channel 16-bit PWM with Complementary Output, Fault Input, 12-bit Dead Time Generator Counter for Motor Control
  - 32-bit Real-time Timer and RTC with calendar and alarm features
  - Up to 15-channel, 1Msps ADC with differential input mode and programmable gain stage
  - One 2-channel 12-bit 1Msps DAC
  - One Analog Comparator with flexible input selection, Selectable input hysteresis
  - 32-bit Cyclic Redundancy Check Calculation Unit (CRCCU)
  - Write Protected Registers

- I/O
  - Up to 79 I/O lines with external interrupt capability (edge or level sensitivity), debouncing, glitch filtering and on-die Series Resistor Termination
  - Three 32-bit Parallel Input/Output Controllers, Peripheral DMA assisted Parallel Capture Mode
- Packages
  - 100-lead LQFP, 14 x 14 mm, pitch 0.5 mm/100-ball TFBGA, 9 x 9 mm, pitch 0.8 mm
  - 64-lead LQFP, 10 x 10 mm, pitch 0.5 mm/64-pad QFN 9x9 mm, pitch 0.5 mm
  - 48-lead LQFP, 7 x 7 mm, pitch 0.5 mm/48-pad QFN 7x7 mm, pitch 0.5 mm

1. Configuration Summary

The SAM3S microcontrollers differ in memory size, package and features list. Table 1-1 below summarizes the configurations of the device family

Table 1-1. Configuration Summary

Device	Flash	SRAM	Timer Counter Channels	GPIOs	UART/ USARTs	ADC	12-bit DAC Output	External Bus Interface	HSMCI	Package
SAM3S4C	256 Kbytes single plane	48 Kbytes	6	79	2/2[1]	15 ch.	2	8-bit data, 4 chip selects, 24-bit address	1 port 4 bits	LQFP100 TFBGA100
SAM3S4B	256 Kbytes single plane	48 Kbytes	6[2]	47	2/2[1]	10 ch.	2	-	1 port 4 bits	LQFP64 QFN 64
SAM3S4A	256 Kbytes single plane	48 Kbytes	6[2]	34	2/1	8 ch.	-	-	-	LQFP48 QFN 48
SAM3S2C	128 Kbytes single plane	32 Kbytes	6	79	2/2[1]	15 ch.	2	8-bit data, 4 chip selects, 24-bit address	1 port 4 bits	LQFP100 TFBGA100
SAM3S2B	128 Kbytes single plane	32 Kbytes	6[2]	47	2/2[1]	10 ch.	2	-	1 port 4 bits	LQFP64 QFN 64
SAM3S2A	128 Kbytes single plane	32 Kbytes	6[2]	34	2/1	8 ch.	-	-	-	LQFP48 QFN 48
SAM3S1C	64 Kbytes single plane	16 Kbytes	6	79	2/2[1]	15 ch.	2	8-bit data, 4 chip selects, 24-bit address	1 port 4 bits	LQFP100 TFBGA100
SAM3S1B	64 Kbytes single plane	16 Kbytes	6[2]	47	2/2[1]	10 ch.	2	-	1 port 4 bits	LQFP64 QFN 64
SAM3S1A	64 Kbytes single plane	16 Kbytes	6[2]	34	2/1	8 ch.	-	-	-	LQFP48 QFN 48

Notes: 1. Full Modem support on USART1.
2. Three TC channels are reserved for internal use.

2. Block Diagram

Figure 2-1. SAM3S 100-pin Version Block Diagram

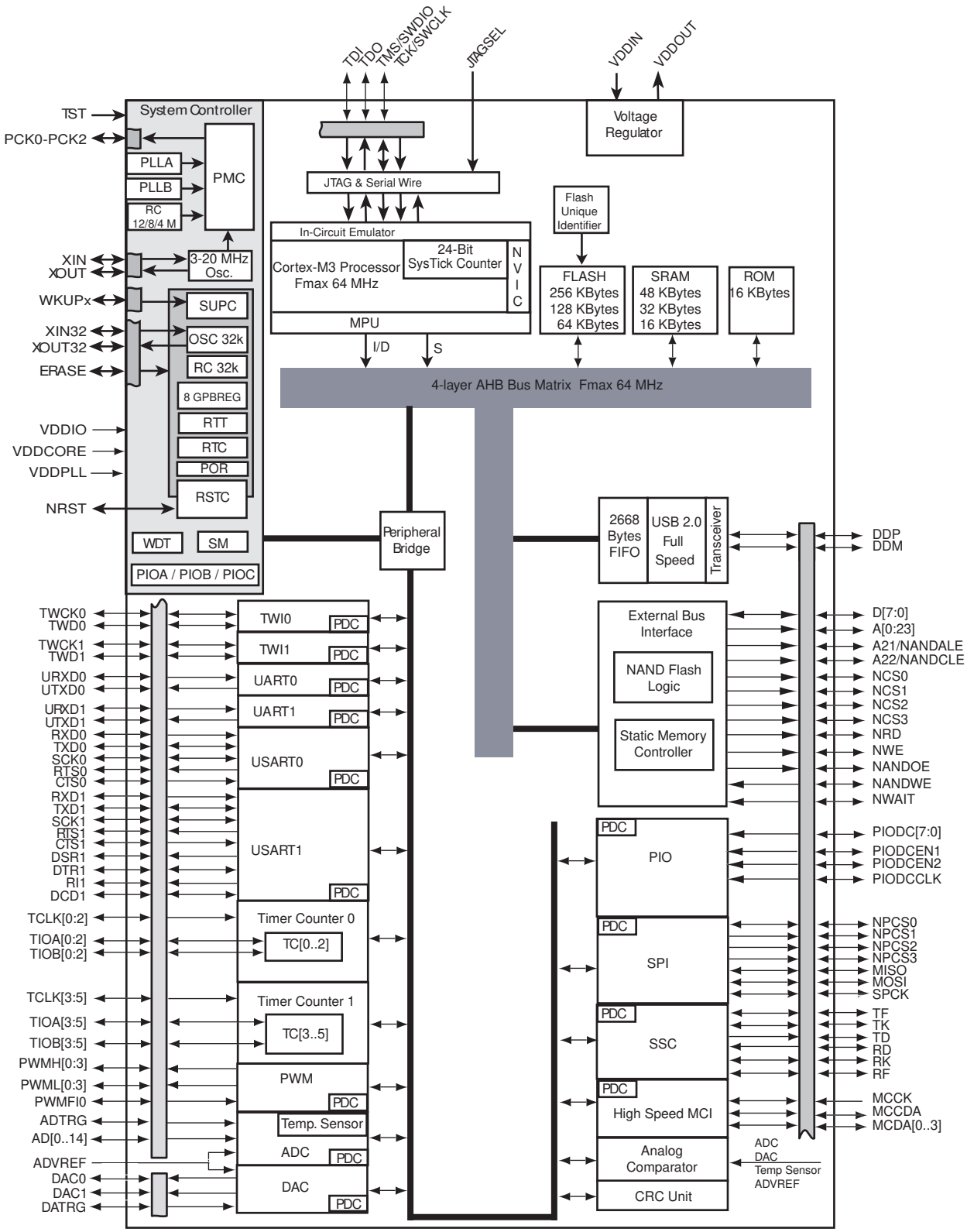


Figure 2-2. SAM3S 64-pin Version Block Diagram

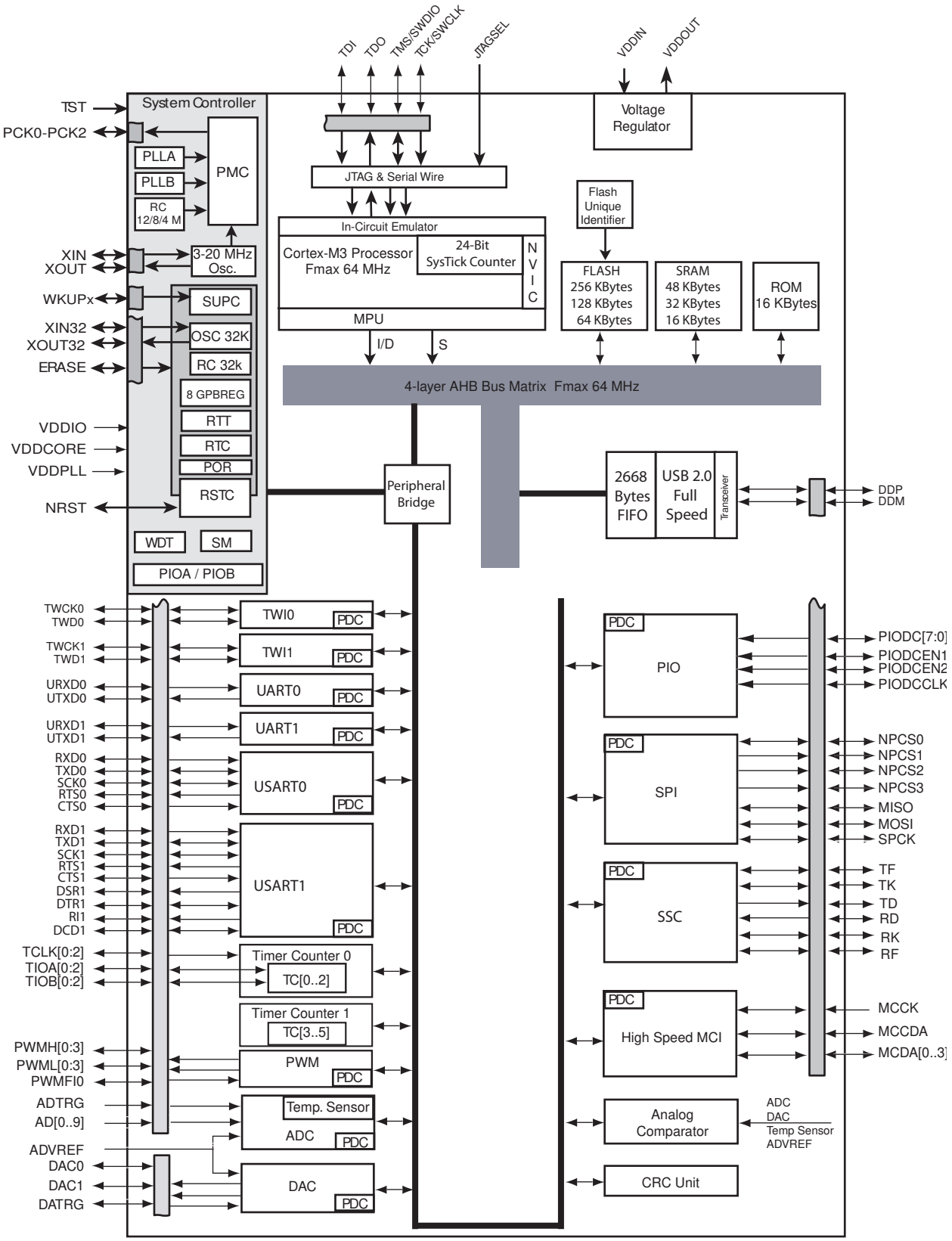
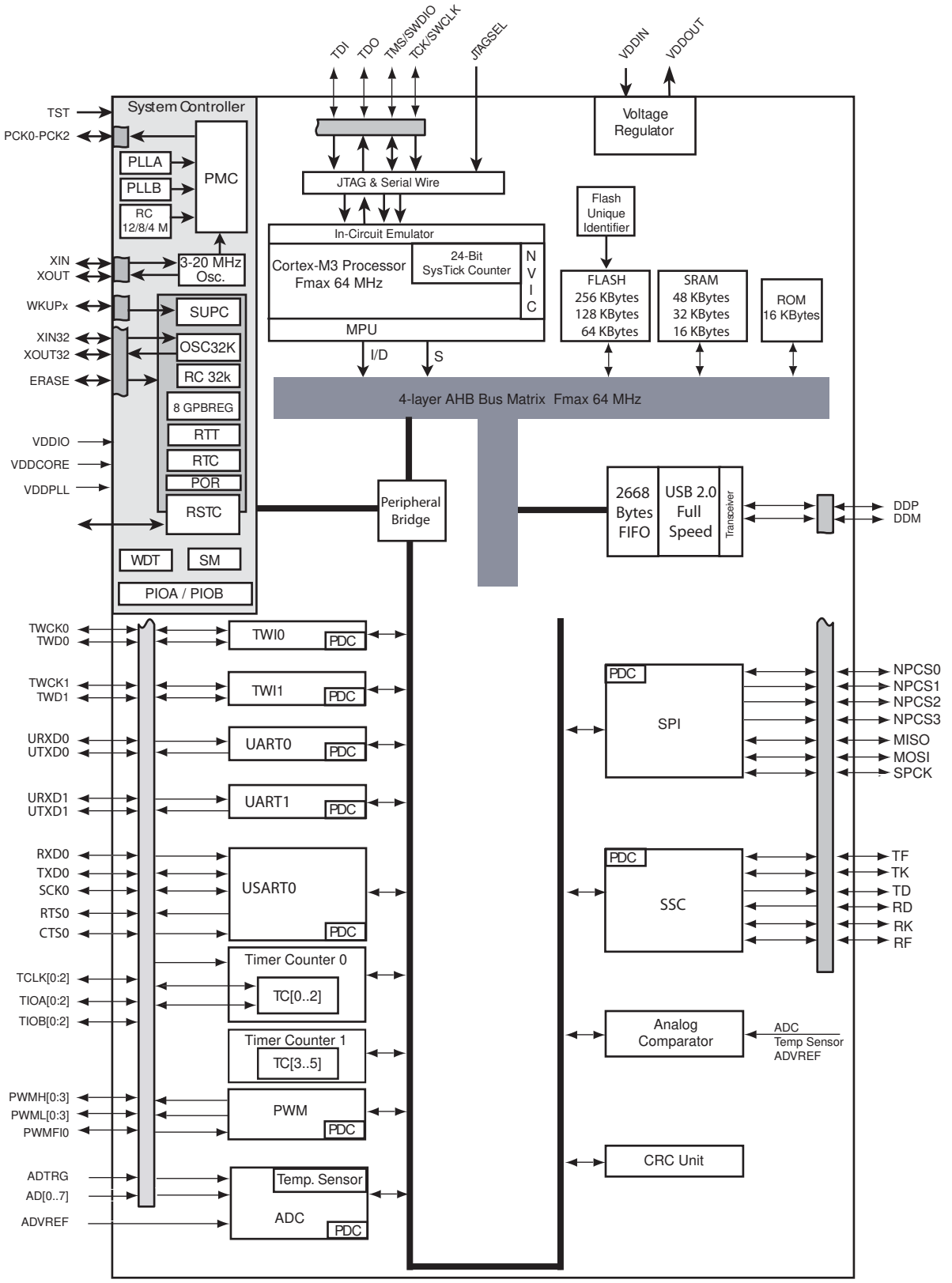


Figure 2-3. SAM3S 48-pin Version Block Diagram



3. Signal Description

Table 3-1 gives details on the signal names classified by peripheral.

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Voltage reference	Comments
Power Supplies					
VDDIO	Peripherals I/O Lines and USB transceiver Power Supply	Power			1.62V to 3.6V
VDDIN	Voltage Regulator Input, ADC, DAC and Analog Comparator Power Supply	Power			1.8V to 3.6V(4)
VDDOUT	Voltage Regulator Output	Power			1.8V Output
VDDPLL	Oscillator and PLL Power Supply	Power			1.62 V to 1.95V
VDDCORE	Power the core, the embedded memories and the peripherals	Power			1.62V to 1.95V
GND	Ground	Ground			
Supply Controller - SUPC					
WKUPx	Wake Up input pins	Input		VDDIO	Reset State: - PIO Input - Internal Pull-up disabled - Schmitt Trigger enabled(1)
Clocks, Oscillators and PLLs					
XIN	Main Oscillator Input	Input		VDDIO	Reset State: - PIO Input - Internal Pull-up disabled - Schmitt Trigger enabled(1)
XOUT	Main Oscillator Output	Output			
XIN32	Slow Clock Oscillator Input	Input			
XOUT32	Slow Clock Oscillator Output	Output			
PCK0 - PCK2	Programmable Clock Output	Output			Reset State: - PIO Input - Internal Pull-up enabled - Schmitt Trigger enabled(1)
Serial Wire/JTAG Debug Port - SWJ-DP					
TCK/SWCLK	Test Clock/Serial Wire Clock	Input		VDDIO	Reset State: - SWJ-DP Mode - Internal pull-up disabled(5) - Schmitt Trigger enabled(1)
TDI	Test Data In	Input			
TDO/TRACESWO	Test Data Out / Trace Asynchronous Data Out	Output			
TMS/SWDIO	Test Mode Select /Serial Wire Input/Output	Input / I/O			
JTAGSEL	JTAG Selection	Input	High		Permanent Internal pull-down
Flash Memory					
ERASE	Flash and NVM Configuration Bits Erase Command	Input	High	VDDIO	Reset State: - Erase Input - Internal pull-down enabled - Schmitt Trigger enabled(1)

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage reference	Comments
Reset/Test					
NRST	Synchronous Microcontroller Reset	I/O	Low	VDDIO	Permanent Internal pull-up
TST	Test Select	Input			Permanent Internal pull-down
Universal Asynchronous Receiver Transmitter - UARTx					
URXDx	UART Receive Data	Input			
UTXDx	UART Transmit Data	Output			
PIO Controller - PIOA - PIOB - PIOC					
PA0 - PA31	Parallel IO Controller A	I/O		VDDIO	Reset State: - PIO or System IOs(2) - Internal pull-up enabled - Schmitt Trigger enabled(1)
PB0 - PB14	Parallel IO Controller B	I/O			
PC0 - PC31	Parallel IO Controller C	I/O			
PIO Controller - Parallel Capture Mode (PIOA Only)					
PIODC0-PIODC7	Parallel Capture Mode Data	Input		VDDIO	
PIODCCLK	Parallel Capture Mode Clock	Input			
PIODCEN1-2	Parallel Capture Mode Enable	Input			
External Bus Interface					
D0 - D7	Data Bus	I/O			
A0 - A23	Address Bus	Output			
NWAIT	External Wait Signal	Input	Low		
Static Memory Controller - SMC					
NCS0 - NCS3	Chip Select Lines	Output	Low		
NRD	Read Signal	Output	Low		
NWE	Write Enable	Output	Low		
NAND Flash Logic					
NANDOE	NAND Flash Output Enable	Output	Low		
NANDWE	NAND Flash Write Enable	Output	Low		
High Speed Multimedia Card Interface - HSMCI					
MCCK	Multimedia Card Clock	I/O			
MCCDA	Multimedia Card Slot A Command	I/O			
MCDA0 - MCDA3	Multimedia Card Slot A Data	I/O			
Universal Synchronous Asynchronous Receiver Transmitter USARTx					
SCKx	USARTx Serial Clock	I/O			
TXDx	USARTx Transmit Data	I/O			
RXDx	USARTx Receive Data	Input			
RTSx	USARTx Request To Send	Output			
CTSx	USARTx Clear To Send	Input			

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage reference	Comments
DTR1	USART1 Data Terminal Ready	I/O			
DSR1	USART1 Data Set Ready	Input			
DCD1	USART1 Data Carrier Detect	Input			
RI1	USART1 Ring Indicator	Input			
Synchronous Serial Controller - SSC					
TD	SSC Transmit Data	Output			
RD	SSC Receive Data	Input			
TK	SSC Transmit Clock	I/O			
RK	SSC Receive Clock	I/O			
TF	SSC Transmit Frame Sync	I/O			
RF	SSC Receive Frame Sync	I/O			
Timer/Counter - TC					
TCLKx	TC Channel x External Clock Input	Input			
TIOAx	TC Channel x I/O Line A	I/O			
TIOBx	TC Channel x I/O Line B	I/O			
Pulse Width Modulation Controller- PWMC					
PWMHx	PWM Waveform Output High for channel x	Output			
PWMLx	PWM Waveform Output Low for channel x	Output			only output in complementary mode when dead time insertion is enabled
PWMFI0	**PWM Fault Input**	Input			
Serial Peripheral Interface - SPI					
MISO	Master In Slave Out	I/O			
MOSI	Master Out Slave In	I/O			
SPCK	SPI Serial Clock	I/O			
SPI_NPCS0	SPI Peripheral Chip Select 0	I/O	Low		
SPI_NPCS1 - SPI_NPCS3	SPI Peripheral Chip Select	Output	Low		
Two-Wire Interface- TWI					
TWDx	TWIx Two-wire Serial Data	I/O			
TWCKx	TWIx Two-wire Serial Clock	I/O			
Analog					
ADVREF	ADC, DAC and Analog Comparator Reference	Analog			
Analog-to-Digital Converter - ADC					
AD0 - AD14	Analog Inputs	Analog, Digital			
ADTRG	ADC Trigger	Input		VDDIO	

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage reference	Comments
12-bit Digital-to-Analog Converter - DAC					
DAC0 - DAC1	Analog output	Analog, Digital			
DACTRG	DAC Trigger	Input		VDDIO	

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage reference	Comments
Fast Flash Programming Interface - FFPI					
PGMEN0-PGMEN2	Programming Enabling	Input		VDDIO	
PGMM0-PGMM3	Programming Mode	Input		VDDIO	
PGMD0-PGMD15	Programming Data	I/O			
PGMRDY	Programming Ready	Output	High		
PGMNVALID	Data Direction	Output	Low		
PGMNOE	Programming Read	Input	Low		
PGMCK	Programming Clock	Input			
PGMNCMD	Programming Command	Input	Low		
USB Full Speed Device					
DDM	USB Full Speed Data -	Analog, Digital		VDDIO	Reset State: - USB Mode - Internal Pull-down(3)
DDP	USB Full Speed Data +				

Notes:
1. Schmitt Triggers can be disabled through PIO registers.
2. Some PIO lines are shared with System IOs.
3. Refer to the “USB” sub section in the product “Electrical Characteristics” Section for Pull-down value in USB Mode.
4. See Section 5.4 “Typical Powering Schematics” for restriction on voltage range of Analog Cells.
5. TDO pin is set in input mode when the Cortex-M3 Core is not in debug mode. Thus the internal pull-up corresponding to this PIO line must be enabled to avoid current consumption due to floating input.

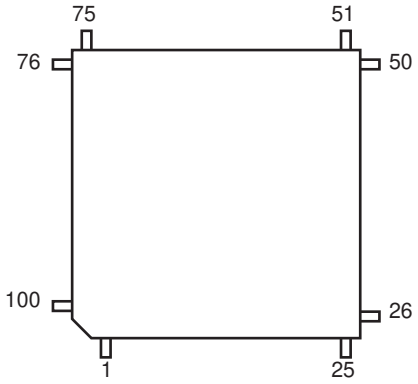
4. Package and Pinout

4.1 SAM3S4/S2/S1C Package and Pinout

Figure 4-2 shows the orientation of the 100-ball TFBGA Package

4.1.1 100-lead LQFP Package Outline

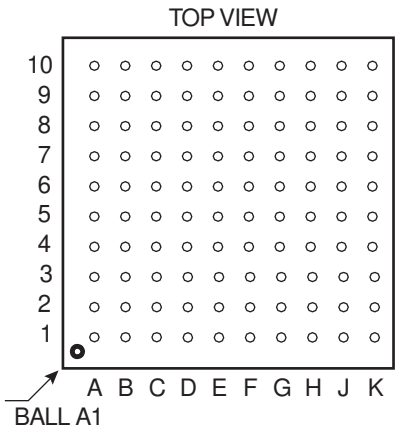
Figure 4-1. Orientation of the 100-lead LQFP Package



4.1.2 100-ball TFBGA Package Outline

The 100-Ball TFBGA package has a 0.8 mm ball pitch and respects Green Standards. Its dimensions are 9 x 9 x 1.1 mm.

Figure 4-2. Orientation of the 100-BALL TFBGA Package



4.1.3 100-Lead LQFP Pinout

Table 4-1. 100-lead LQFP SAM3S4/S2/S1C Pinout

1	ADVREF	26	GND	51	TDI/PB4	76	TDO/TRACESWO/PB5
2	GND	27	VDDIO	52	PA6/PGMNOE	77	JTAGSEL
3	PB0/AD4	28	PA16/PGMD4	53	PA5/PGMRDY	78	PC18
4	PC29/AD13	29	PC7	54	PC28	79	TMS/SWDIO/PB6
5	PB1/AD5	30	PA15/PGMD3	55	PA4/PGMNCMD	80	PC19
6	PC30/AD14	31	PA14/PGMD2	56	VDDCORE	81	PA31
7	PB2/AD6	32	PC6	57	PA27/PGMD15	82	PC20
8	PC31	33	PA13/PGMD1	58	PC8	83	TCK/SWCLK/PB7
9	PB3/AD7	34	PA24/PGMD12	59	PA28	84	PC21
10	VDDIN	35	PC5	60	NRST	85	VDDCORE
11	VDDOUT	36	VDDCORE	61	TST	86	PC22
12	PA17/PGMD5/AD0	37	PC4	62	PC9	87	ERASE/PB12
13	PC26	38	PA25/PGMD13	63	PA29	88	DDM/PB10
14	PA18/PGMD6/AD1	39	PA26/PGMD14	64	PA30	89	DDP/PB11
15	PA21/PGMD9/AD8	40	PC3	65	PC10	90	PC23
16	VDDCORE	41	PA12/PGMD0	66	PA3	91	VDDIO
17	PC27	42	PA11/PGMM3	67	PA2/PGMEN2	92	PC24
18	PA19/PGMD7/AD2	43	PC2	68	PC11	93	PB13/DAC0
19	PC15/AD11	44	PA10/PGMM2	69	VDDIO	94	PC25
20	PA22/PGMD10/AD9	45	GND	70	GND	95	GND
21	PC13/AD10	46	PA9/PGMM1	71	PC14	96	PB8/XOUT
22	PA23/PGMD11	47	PC1	72	PA1/PGMEN1	97	PB9/*PGMCK/XIN*
23	PC12/AD12	48	PA8/XOUT32/ PGMM0	73	PC16	98	VDDIO
24	PA20/PGMD8/AD3	49	PA7/XIN32/ PGMNVALID	74	PA0/PGMEN0	99	PB14/DAC1
25	PC0	50	VDDIO	75	PC17	100	VDDPLL

4.1.4 100-ball TFBGA Pinout

Table 4-2. 100-ball TFBGA SAM3S4/S2/S1C Pinout

A1	PB1/AD5	C6	TCK/SWCLK/PB7	F1	PA18/PGMD6/AD1	H6	PC4
A2	PC29	C7	PC16	F2	PC26	H7	PA11/PGMM3
A3	VDDIO	C8	PA1/PGMEN1	F3	VDDOUT	H8	PC1
A4	PB9/PGMCK/XIN	C9	PC17	F4	GND	H9	PA6/PGMNOE
A5	PB8/XOUT	C10	PA0/PGMEN0	F5	VDDIO	H10	TDI/PB4
A6	PB13/DAC0	D1	PB3/AD7	F6	PA27/PGMD15	J1	PC15/AD11
A7	DDP/PB11	D2	PB0/AD4	F7	PC8	J2	PC0
A8	DDM/PB10	D3	PC24	F8	PA28	J3	PA16/PGMD4
A9	TMS/SWDIO/PB6	D4	PC22	F9	TST	J4	PC6
A10	JTAGSEL	D5	GND	F10	PC9	J5	PA24/PGMD12
B1	PC30/AD14	D6	GND	G1	PA21/PGMD9/AD8	J6	PA25/PGMD13
B2	ADVREF	D7	VDDCORE	G2	PC27	J7	PA10/PGMM2
B3	GNDANA	D8	PA2/PGMEN2	G3	PA15/PGMD3	J8	GND
B4	PB14/DAC1	D9	PC11	G4	VDDCORE	J9	VDDCORE
B5	PC21	D10	PC14	G5	VDDCORE	J10	VDDIO
B6	PC20	E1	PA17/PGMD5/AD0	G6	PA26/PGMD14	K1	PA22/PGMD10/AD9
B7	PA31	E2	PC31	G7	PA12/PGMD0	K2	PC13/AD10
B8	PC19	E3	VDDIN	G8	PC28	K3	PC12/AD12
B9	PC18	E4	GND	G9	PA4/PGMNCMD	K4	PA20/PGMD8/AD3
B10	TDO/TRACESWO/ PB5	E5	GND	G10	PA5/PGMRDY	K5	PC5
C1	PB2/AD6	E6	NRST	H1	PA19/PGMD7/AD2	K6	PC3
C2	VDDPLL	E7	PA29/AD13	H2	PA23/PGMD11	K7	PC2
C3	PC25	E8	PA30	H3	PC7	K8	PA9/PGMM1
C4	PC23	E9	PC10	H4	PA14/PGMD2	K9	PA8/XOUT32/PGMM0
C5	ERASE/PB12	E10	PA3	H5	PA13/PGMD1	K10	PA7/XIN32/ PGMNVALID

4.2 SAM3S4/S2/S1B Package and Pinout

Figure 4-3. Orientation of the 64-pad QFN Package

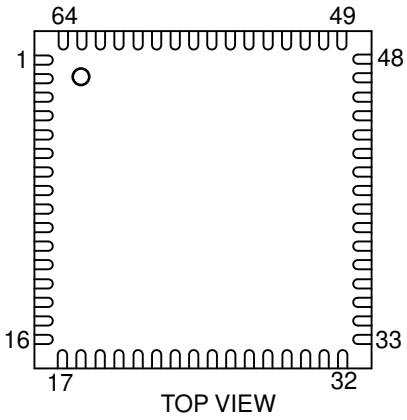
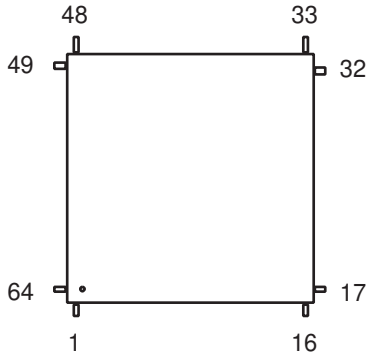


Figure 4-4. Orientation of the 64-lead LQFP Package



4.2.1 64-Lead LQFP and QFN Pinout

64-pin version SAM3S devices are pin-to-pin compatible with AT91SAM7S legacy products. Furthermore, SAM3S products have new functionalities shown in italic in Table 4-3.

Table 4-3. 64-pin SAM3S4/2/1B Pinout

1	ADVREF	17	GND	33	TDI/PB4	49	TDO/TRACESWO/PB5
2	GND	18	VDDIO	34	PA6/PGMNOE	50	JTAGSEL
3	PB0/AD4	19	PA16/PGMD4	35	PA5/PGMRDY	51	TMS/SWDIO/PB6
4	PB1/AD5	20	PA15/PGMD3	36	PA4/PGMNCMD	52	PA31
5	PB2/AD6	21	PA14/PGMD2	37	PA27/PGMD15	53	TCK/SWCLK/PB7
6	PB3/AD7	22	PA13/PGMD1	38	PA28	54	VDDCORE
7	VDDIN	23	PA24/PGMD12	39	NRST	55	ERASE/PB12
8	VDDOUT	24	VDDCORE	40	TST	56	DDM/PB10
9	PA17/PGMD5/AD*0*	25	PA25/PGMD13	41	PA29	57	DDP/PB11
10	PA18/PGMD6/AD1	26	PA26/PGMD14	42	PA30	58	VDDIO
11	PA21/PGMD9/AD8	27	PA12/PGMD0	43	PA3	59	PB13/DAC0
12	VDDCORE	28	PA11/PGMM3	44	PA2/PGMEN2	60	GND
13	PA19/PGMD7/AD2	29	PA10/PGMM2	45	VDDIO	61	XOUT/PB8
14	PA22/PGMD10/AD9	30	PA9/PGMM1	46	GND	62	XIN/PGMCK/PB9
15	PA23/PGMD11	31	PA8/*XOUT32*/PGMM0	47	PA1/PGMEN1	63	PB14/DAC1
16	PA20/PGMD8/AD3	32	PA7/*XIN32*/PGMNVALID	48	PA0/PGMEN0	64	VDDPLL

Note: The bottom pad of the QFN package must be connected to ground.

4.3 SAM3S4/2/1A Package and Pinout

Figure 4-5. Orientation of the 48-pad QFN Package

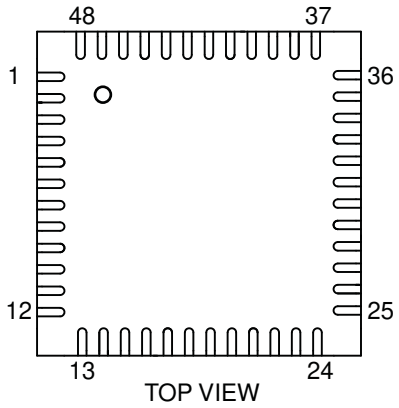
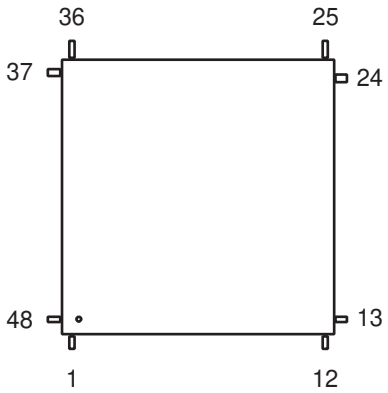


Figure 4-6. Orientation of the 48-lead LQFP Package



4.3.1 48-Lead LQFP and QFN Pinout

Table 4-4. 48-pin SAM3S4/2/1A Pinout

1	ADVREF	13	VDDIO	25	TDI/PB4	37	TDO/TRACESWO/ PB5
2	GND	14	PA16/PGMD4	26	PA6/PGMNOE	38	JTAGSEL
3	PB0/AD4	15	PA15/PGMD3	27	PA5/PGMRDY	39	TMS/SWDIO/PB6
4	PB1/AD5	16	PA14/PGMD2	28	PA4/PGMNCMD	40	TCK/SWCLK/PB7
5	PB2/AD6	17	PA13/PGMD1	29	NRST	41	VDDCORE
6	PB3/AD7	18	VDDCORE	30	TST	42	ERASE/PB12
7	VDDIN	19	PA12/PGMD0	31	PA3	43	DDM/PB10
8	VDDOUT	20	PA11/PGMM3	32	PA2/PGMEN2	44	DDP/PB11
9	PA17/PGMD5/AD0	21	PA10/PGMM2	33	VDDIO	45	XOUT/PB8
10	PA18/PGMD6/AD1	22	PA9/PGMM1	34	GND	46	XIN/PB9/PGMCK
11	PA19/PGMD7/AD2	23	PA8/*XOUT32*/ PGMM0	35	PA1/PGMEN1	47	VDDIO
12	PA20/AD3	24	PA7/*XIN32*/ PGMNVALID	36	PA0/PGMEN0	48	VDDPLL

Note: The bottom pad of the QFN package must be connected to ground.

5. Power Considerations

5.1 Power Supplies

The SAM3S product has several types of power supply pins:

- VDDCORE pins: Power the core, the embedded memories and the peripherals. Voltage ranges from 1.62V to 1.95V.
- VDDIO pins: Power the Peripherals I/O lines (Input/Output Buffers); USB transceiver; Backup part, 32 kHz crystal oscillator and oscillator pads; ranges from 1.62V to 3.6V.
- VDDIN pin: Voltage Regulator Input, ADC, DAC and Analog Comparator Power Supply; Voltage ranges from 1.8V to 3.6V
- VDDPLL pin: Powers the PLLA, PLLB, the Fast RC and the 3 to 20 MHz oscillator; voltage ranges from 1.62V to 1.95V.

5.2 Power-up Considerations

5.2.1 VDDIO Versus VDDCORE

VDDIO must always be higher than or equal to VDDCORE.

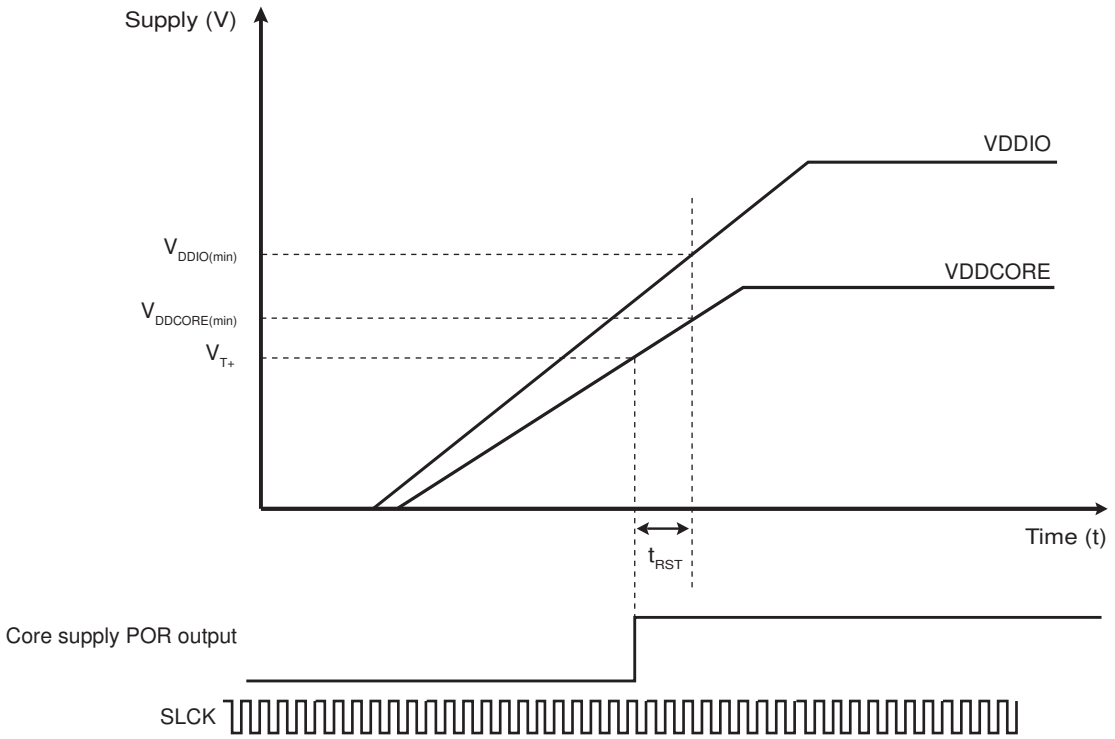
VDDIO must reach its minimum operating voltage (1.62 V) before VDDCORE has reached the following thresholds:

- the minimum V_{T+} of the core power supply brownout detector (1.36 V)
- the minimum value of t_{RST} (100 µs)

If VDDCORE rises at the same time as VDDIO, the VDDIO rising slope must be higher than or equal to 5 V/ms.

If VDDCORE is powered by the internal regulator, all power-up considerations are met.

Figure 5-1. VDDCORE and VDDIO Constraints at Startup



5.2.2 VDDIO Versus VDDIN

At power-up, VDDIO needs to reach 0.6 V before VDDIN reaches 1.0 V.

VDDIO voltage needs to be equal to or below (VDDIN voltage + 0.5 V).

5.3 Voltage Regulator

The SAM3S embeds a voltage regulator that is managed by the Supply Controller.

This internal regulator is intended to supply the internal core of SAM3S. It features two different operating modes:

- In Normal mode, the voltage regulator consumes less than 700 µA static current and draws 80 mA of output current. Internal adaptive biasing adjusts the regulator quiescent current depending on the required load current. In Wait Mode quiescent current is only 7 µA.
- In Backup mode, the voltage regulator consumes less than 1 µA while its output (VDDOUT) is driven internally to GND. The default output voltage is 1.80V and the start-up time to reach Normal mode is inferior to 100 µs.

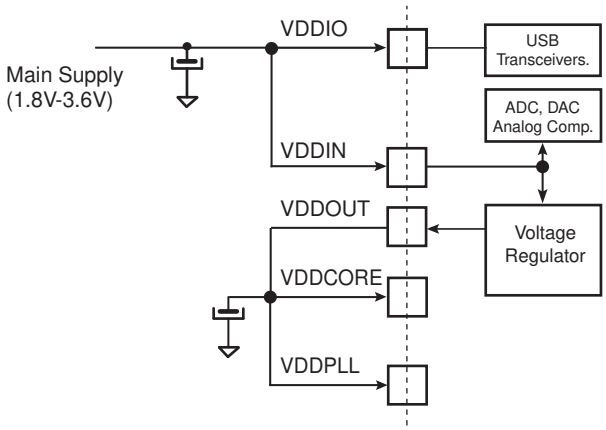
For adequate input and output power supply decoupling/bypassing, refer to the “Voltage Regulator” section in the “Electrical Characteristics” section of the datasheet.

5.4 Typical Powering Schematics

The SAM3S supports a 1.62V-3.6V single supply mode. The internal regulator input connected to the source and its output feeds VDDCORE. Figure 5-2 shows the power schematics.

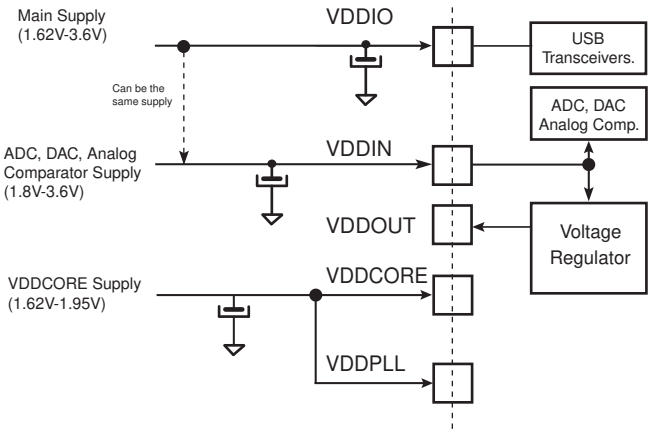
As VDDIN powers the voltage regulator, the ADC/DAC and the analog comparator, when the user does not want to use the embedded voltage regulator, it can be disabled by software via the SUPC (note that it is different from Backup mode).

Figure 5-2. Single Supply



Note: For USB, VDDIO needs to be greater than 3.0V.
For ADC, VDDIN needs to be greater than 2.0V.
For DAC, VDDIN needs to be greater than 2.4V.

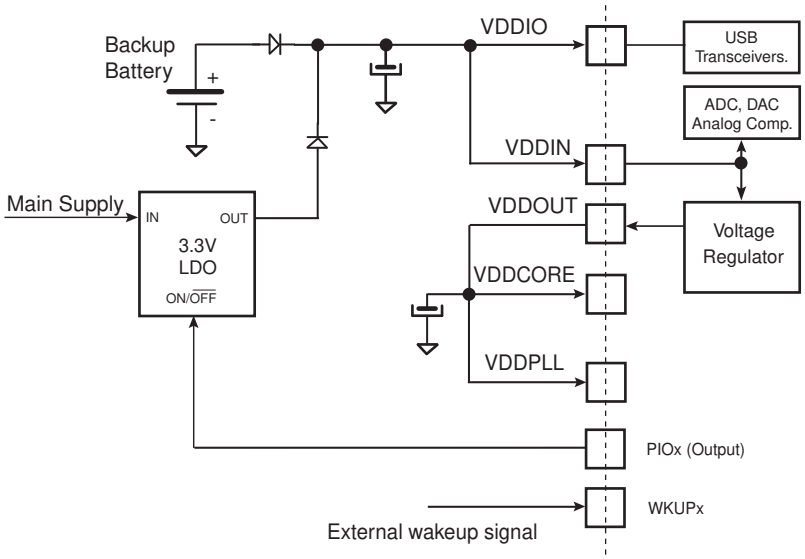
Figure 5-3. Core Externally Supplied.



Note: For USB, VDDIO needs to be greater than 3.0V
For ADC, VDDIN needs to be greater than 2.0V.
For DAC, VDDIN needs to be greater than 2.4V.

Figure 5-4 below provides an example of the powering scheme when using a backup battery. Since the PIO state is preserved when in backup mode, any free PIO line can be used to switch off the external regulator by driving the PIO line at low level (PIO is input, pull-up enabled after backup reset). External wake-up of the system can be from a push button or any signal. See Section 5.7 “Wake-up Sources” for further details.

Figure 5-4. Backup Battery



Note: The two diodes provide a “switchover circuit” (for illustration purpose) between the backup battery and the main supply when the system is put in backup mode.

Note: For ADC, VDDIN needs to be greater than 2.0V.
For DAC, VDDIN needs to be greater than 2.4V.

5.5 Active Mode

Active mode is the normal running mode with the core clock running from the fast RC oscillator, the main crystal oscillator or the PLLA. The power management controller can be used to adapt the frequency and to disable the peripheral clocks.

5.6 Low Power Modes

The various low power modes of the SAM3S are described below:

5.6.1 Backup Mode

The purpose of backup mode is to achieve the lowest power consumption possible in a system which is performing periodic wake-ups to perform tasks but not requiring fast startup time (<0.1ms). Total current consumption is 3 µA typical.

The Supply Controller, zero-power power-on reset, RTT, RTC, Backup registers and 32 kHz oscillator (RC or crystal oscillator selected by software in the Supply Controller) are running. The regulator and the core supply are off.

Backup mode is based on the Cortex-M3 deepsleep mode with the voltage regulator disabled.

The SAM3S can be awakened from this mode through WKUP0-15 pins, the supply monitor (SM), the RTT or RTC wake-up event.

Backup mode is entered by using WFE instructions with the SLEEPDEEP bit in the System Control Register of the Cortex-M3 set to 1. (See the Power management description in The ARM Cortex-M3Processor section of the product datasheet).

Exit from Backup mode happens if one of the following enable wake up events occurs:

- WKUPEN0-15 pins (level transition, configurable debouncing)
- Supply Monitor alarm
- RTC alarm
- RTT alarm

5.6.2 Wait Mode

The purpose of the wait mode is to achieve very low power consumption while maintaining the whole device in a powered state for a startup time of less than 10 µs. Current Consumption in Wait mode is typically 15 µA (total current consumption) if the internal voltage regulator is used or 8 µA if an external regulator is used.

In this mode, the clocks of the core, peripherals and memories are stopped. However, the core, peripherals and memories power supplies are still powered. From this mode, a fast start up is available.

This mode is entered via Wait for Event (WFE) instructions with LPM = 1 (Low Power Mode bit in PMC_FSMR). The Cortex-M3 is able to handle external events or internal events in order to wake-up the core (WFE). This is done by configuring the external lines WKUP0-15 as fast startup wake-up pins (refer to Section 5.8 “Fast Startup”). RTC or RTT Alarm and USB wake-up events can be used to wake up the CPU (exit from WFE).

Entering Wait Mode:

- Select the 4/8/12 MHz fast RC oscillator as Main Clock
- Set the LPM bit in the PMC Fast Startup Mode Register (PMC_FSMR)
- Execute the Wait-For-Event (WFE) instruction of the processor

Note: Internal Main clock resynchronization cycles are necessary between the writing of MOSCRCEN bit and the effective entry in Wait mode. Depending on the user application, Waiting for MOSCRCEN bit to be cleared is recommended to ensure that the core will not execute undesired instructions.

The bit MOSCRCEN should be automatically set to '0'. So you have to add after this instruction the following: while (MOSCRCEN ==0); so that you are sure to stay in the loop until you awake from the wait mode. In that case you

are sure the core will not continue to fetch the code but once you have exited the wait mode (in that case MOSCRCEN will be automatically set to '1').

5.6.3 Sleep Mode

The purpose of sleep mode is to optimize power consumption of the device versus response time. In this mode, only the core clock is stopped. The peripheral clocks can be enabled. The current consumption in this mode is application dependent.

This mode is entered via Wait for Interrupt (WFI) or Wait for Event (WFE) instructions with LPM = 0 in PMC_FSMR.

The processor can be awakened from an interrupt if WFI instruction of the Cortex-M3is used, or from an event if the WFE instruction is used to enter this mode.

5.6.4 Low Power Mode Summary Table

The modes detailed above are the main low power modes. Each part can be set to on or off separately and wake up sources can be individually configured. Table 5-1 below shows a summary of the configurations of the low power modes.

Table 5-1. Low Power Mode Configuration Summary

Mode	SUPC, 32 kHz Oscillator RTC RTT Backup Registers, POR (Backup Region)	Regulator	Core Memory Peripherals	Mode Entry	Potential Wake Up Sources	Core at Wake Up	PIO State while in Low Power Mode	PIO State at Wake Up	Consumption (2) (3)	Wake-up Time(1)
Backup Mode	ON	OFF	OFF (Not powered)	WFE +SLEEPDEEP bit = 1	WKUP0-15 pins SM alarm RTC alarm RTT alarm	Reset	Previous state saved	PIOA & PIOB & PIOC Inputs with pull ups	3 µA typ(4)	< 0.1 ms
Wait Mode	ON	ON	Powered (Not clocked)	WFE +SLEEPDEEP bit = 0 +LPM bit = 1	Any Event from: Fast startup through WKUP0-15 pins RTC alarm RTT alarm USB wake-up	Clocked back	Previous state saved	Unchanged	5 µA/15 µA (5)	< 10 µs
Sleep Mode	ON	ON	Powered(7) (Not clocked)	WFE or WFI +SLEEPDEEP bit = 0 +LPM bit = 0	Entry mode =WFI Interrupt Only; Entry mode =WFE Any Enabled Interrupt and/or Any Event from: Fast start-up through WKUP0-15 pins RTC alarm RTT alarm USB wake-up	Clocked back	Previous state saved	Unchanged	(6)	(6)

Notes:
1. When considering wake-up time, the time required to start the PLL is not taken into account. Once started, the device works with the 4/8/12 MHz fast RC oscillator. The user has to add the PLL start-up time if it is needed in the system. The wake-up time is defined as the time taken for wake up until the first instruction is fetched.
2. The external loads on PIOs are not taken into account in the calculation.
3. Supply Monitor current consumption is not included.
4. Total Current consumption.
5. 5 µA on VDDCORE, 15 µA for total current consumption (using internal voltage regulator), 8 µA for total current consumption (without using internal voltage regulator).
6. Depends on MCK frequency.
7. In this mode the core is supplied and not clocked but some peripherals can be clocked.