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SAM3U Series

Atmel | SMART ARM-based Flash MCU

DATASHEET

Description

The Atmel® | SMART SAM3U series is a member of a family of Flash microcontrollers based on the high performance 32-bit ARM® Cortex®-M3 RISC processor. It operates at a maximum speed of 96 MHz and features up to 256 Kbytes of Flash and up to 52 Kbytes of SRAM. The peripheral set includes a High Speed USB Device Port with embedded transceiver, a High Speed MCI for SDIO/SD/MMC, an External Bus Interface with NAND Flash controller, up to 4 USARTs, up to 2 TWIs, up to 5 SPIs, as well as 4 PWM timers, one 3-channel 16-bit general-purpose timer, a low-power RTC, a 12-bit ADC and a 10-bit ADC.

The SAM3U devices have three software-selectable low-power modes: Sleep, Wait, and Backup. In Sleep mode, the processor is stopped while all other functions can be kept running. In Wait mode, all clocks and functions are stopped but some peripherals can be configured to wake up the system based on predefined conditions. In Backup mode, only the RTC, RTT, and wake-up logic are running.

The Real-time Event Managment allows peripherals to receive, react to and send events in Active and Sleep modes without processor intervention.

The SAM3U architecture is specifically designed to sustain high speed data transfers. It includes a multi-layer bus matrix as well as multiple SRAM banks, PDC and DMA channels that enable it to run tasks in parallel and maximize data throughput.

It can operate from 1.62V to 3.6V and comes in 100-pin and 144-pin LQFP and BGA packages.

The SAM3U device is particularly well suited for USB applications: data loggers, PC peripherals and any high speed bridge (USB to SDIO, USB to SPI, USB to External Bus Interface).

1. Features

- Core
  - ARM Cortex-M3 revision 2.0 running at up to 96 MHz
  - Memory Protection Unit (MPU)
  - Thumb®-2 instruction set
- Memories
  - 64 to 256 Kbytes embedded Flash, 128-bit wide access, memory accelerator, dual bank
  - 16 to 48 Kbytes embedded SRAM with dual banks
  - 16 Kbytes ROM with embedded bootloader routines (UART, USB) and IAP routines
  - Static Memory Controller (SMC): SRAM, NOR, NAND support. NAND Flash controller with 4 Kbytes RAM buffer and ECC
- System
  - Embedded voltage regulator for single supply operation
  - POR, BOD and Watchdog for safe reset
  - Quartz or resonator oscillators: 3 to 20 MHz main and optional low power 32.768 kHz for RTC or device clock
  - High precision 8/12 MHz factory trimmed internal RC oscillator with 4 MHz Default Frequency for fast device startup
  - Slow Clock Internal RC oscillator as permanent clock for device clock in low power mode
  - One PLL for device clock and one dedicated PLL for USB 2.0 High Speed Device
  - Up to 17 Peripheral DMA Controller (PDC) channels and 4-channel central DMA
- Low Power Modes
  - Sleep, Wait, and Backup modes, down to 1.65 µA in Backup mode with RTC, RTT, and GPBR
- Peripherals
  - USB 2.0 Device: 480 Mbps, 4-Kbyte FIFO, up to 7 bidirectional Endpoints, dedicated DMA
  - Up to 4 USARTs (ISO7816, IrDA®, Flow Control, SPI, Manchester support) and one UART
  - Up to 2 TWI (I2C compatible)
  - 1 Serial Perpheral Interface (SPI)
  - 1 Synchronous Serial Controller (SSC) (I2S)
  - 1 High Speed Multimedia Card Interface (HSMCI) (SDIO/SD/MMC)
  - 3-channel 16-bit Timer/Counter (TC) for capture, compare and PWM
  - 4-channel 16-bit PWM (PWMC)
  - 32-bit Real-time Timer (RTT) and Real-time Clock (RTC) with calendar and alarm features
  - 8-channel 12-bit 1 msps ADC with differential input mode and programmable gain stage
  - 8-channel 10-bit ADC
- I/O
  - Up to 96 I/O lines with external interrupt capability (edge or level sensitivity), debouncing, glitch filtering and on-die Series Resistor Termination
  - Three 32-bit Parallel Input/Outputs (PIO)
- Packages
  - 100-lead LQFP – 14 × 14 mm, pitch 0.5 mm
  - 100-ball TFBGA – 9 × 9 mm, pitch 0.8 mm
  - 144-lead LQFP – 20 × 20 mm, pitch 0.5 mm
  - 144-ball LFBGA – 10 × 10 mm, pitch 0.8 mm

1.1 Configuration Summary

The SAM3U series devices differ in memory sizes, package and features list. Table 1-1 summarizes the configurations of the six devices.

Table 1-1. Configuration Summary

Feature	ATSAM3U4E	ATSAM3U2E	ATSAM3U1E	ATSAM3U4C	ATSAM3U2C	ATSAM3U1C
Flash	2 x 128 Kbytes Dual plane	128 Kbytes Single plane	64 Kbytes Single plane	2 x 128 Kbytes Dual plane	128 Kbytes Single plane	64 Kbytes Single plane
SRAM	52 Kbytes	36 Kbytes	20 Kbytes	52 Kbytes	36 Kbytes	20 Kbytes
Package	LQFP144 BGA144	LQFP144 BGA144	LQFP144 BGA144	LQFP100 BGA100	LQFP100 BGA100	LQFP100 BGA100
External Bus Interface	8 or 16 bits, 4 chip selects, 24-bit address	8 or 16 bits, 4 chip selects, 24-bit address	8 or 16 bits, 4 chip selects, 24-bit address	8 bits, 2 chip selects, 8-bit address	8 bits, 2 chip selects, 8-bit address	8 bits, 2 chip selects, 8-bit address
Number of PIOs	96	96	96	57	57	57
SPI	5	5	5	4	4	4
TWI	2	2	2	1	1	1
USART	4	4	4	3	3	3
ADC 12-bit	8 channels	8 channels	8 channels	4 channels	4 channels	4 channels
ADC 10-bit	8 channels	8 channels	8 channels	4 channels	4 channels	4 channels
FWUP, SHDN pins	Yes	Yes	Yes	FWUP	FWUP	FWUP
HSMCI Data Size	8 bits	8 bits	8 bits	4 bits	4 bits	4 bits

Note: 1. The SRAM size takes into account the 4 Kbyte RAM buffer of the NAND Flash Controller (NFC) which can be used by the core if not used by the NFC.

2. Block Diagram

Figure 2-1. 144-pin SAM3U4/2/1E Block Diagram

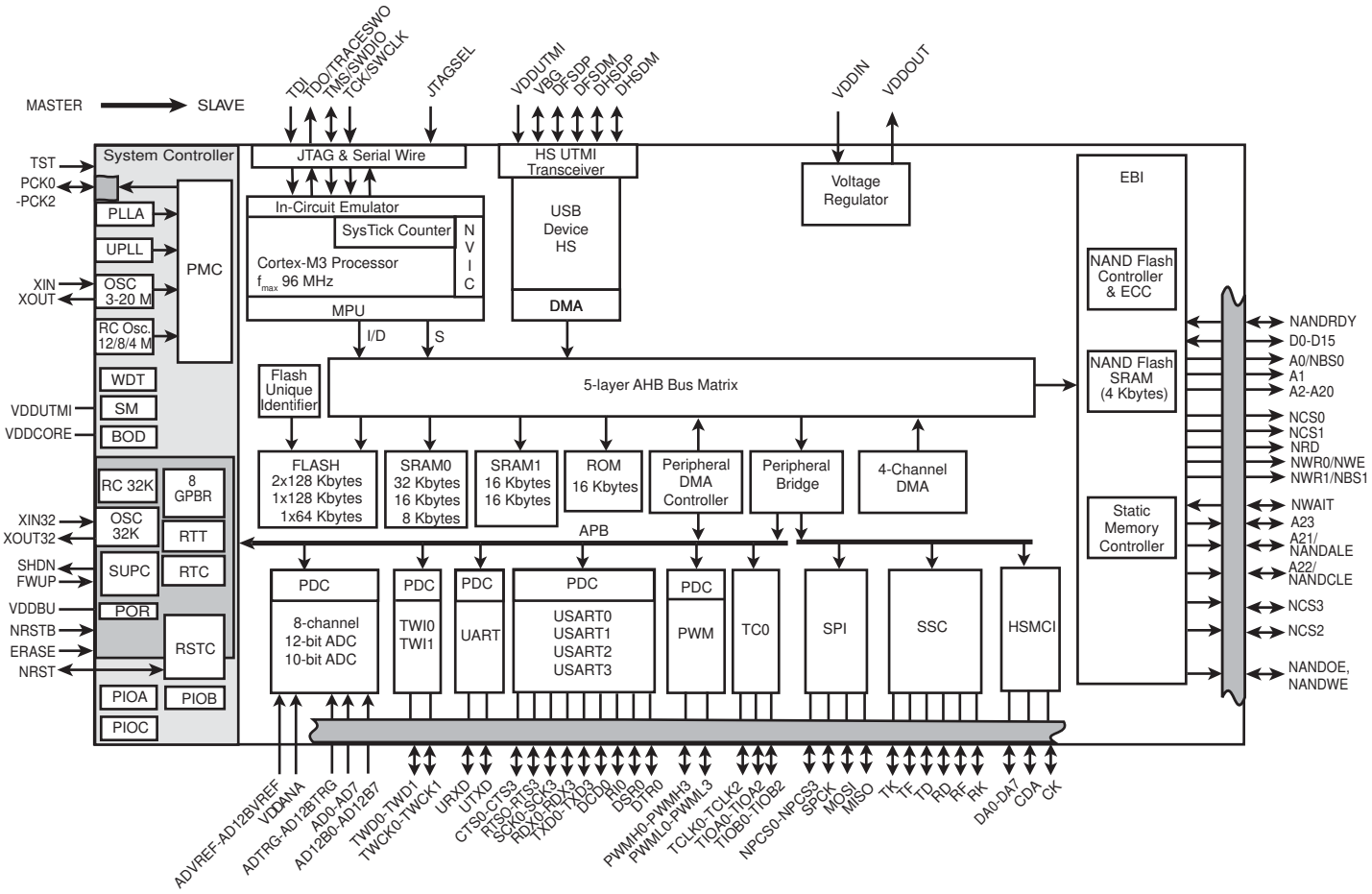
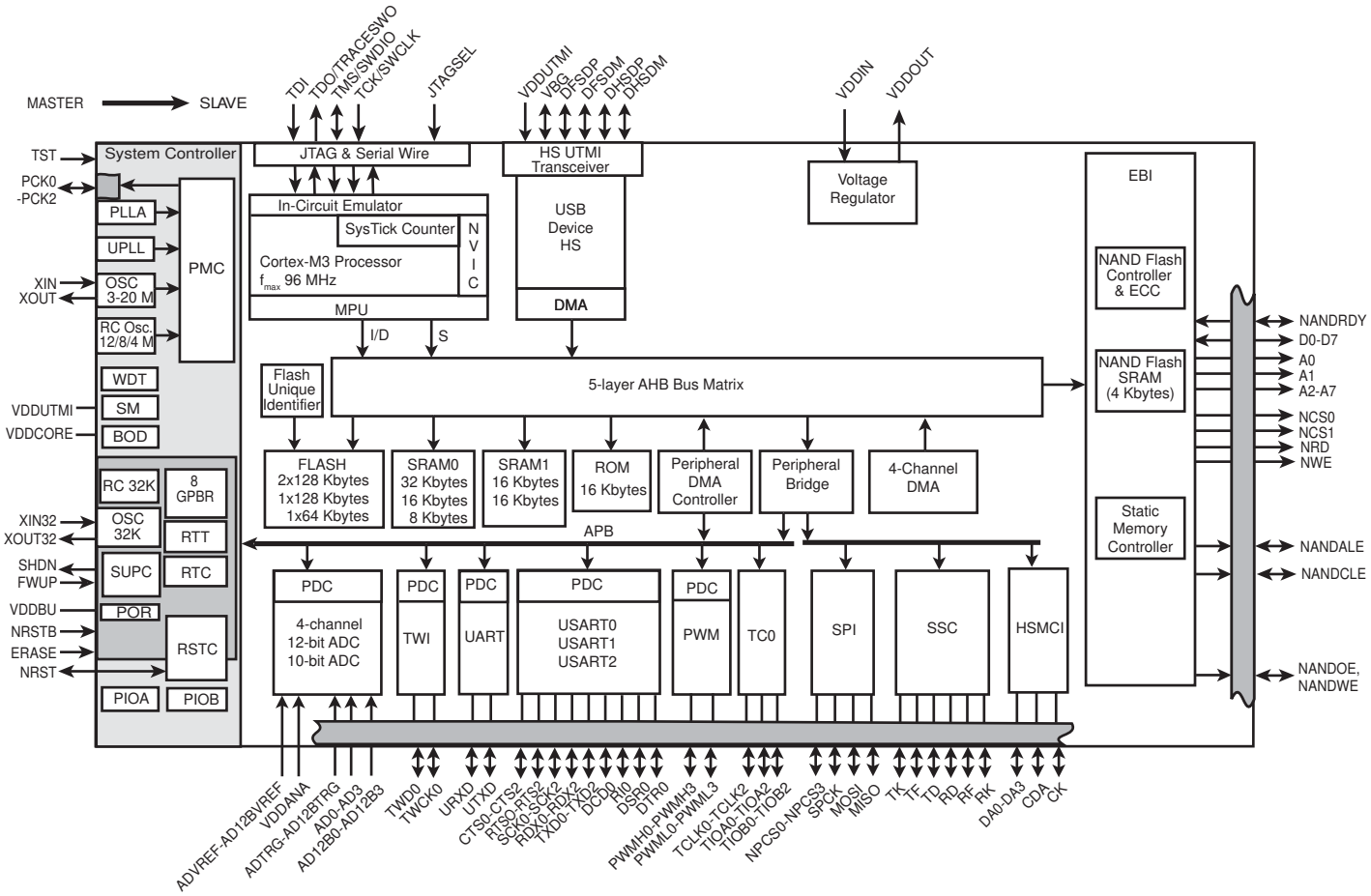


Figure 2-2. 100-pin SAM3U4/2/1C Block Diagram



3. Signal Description

Table 3-1 gives details on the signal names classified by peripheral.

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Power Supplies					
VDDIO	Peripherals I/O Lines Power Supply	Power			1.62V to 3.6V
VDDIN	Voltage Regulator Input	Power			1.8V to 3.6V
VDDOUT	Voltage Regulator Output	Power			1.8V
VDDUTMI	USB UTMI+ Interface Power Supply	Power			3.0V to 3.6V
GNDUTMII	USB UTMI+ Interface Ground	Ground			
VDDBU	Backup I/O Lines Power Supply	Power			1.62V to 3.6V
GNDBU	Backup Ground	Ground			
VDDPLL	PLL A, UPLL and Osc 3–20 MHz Power Supply	Power			1.62 V to 1.95V
GNDPLL	PLL A, UPLL and Osc 3–20 MHz Ground	Ground			
VDDANA	ADC Analog Power Supply	Power			2.0V to 3.6V
GNDANA	ADC Analog Ground	Ground			
VDDCORE	Core, Memories and Peripherals Chip Power Supply	Power			1.62V to 1.95V
GND	Ground	Ground			
Clocks, Oscillators and PLLs					
XIN	Main Oscillator Input	Input		VDDPLL	
XOUT	Main Oscillator Output	Output			
XIN32	Slow Clock Oscillator Input	Input		VDDBU	
XOUT32	Slow Clock Oscillator Output	Output			
VBG	Bias Voltage Reference	Analog			
PCK0–PCK2	Programmable Clock Output	Output		VDDIO	
Shutdown, Wakeup Logic					
SHDN	Shut-Down Control	Output		VDDBU	Push/pull 0: The device is in backup mode 1: The device is running (not in backup mode)
FWUP	Force Wake-Up Input	Input	Low		Needs external pull-up
Serial Wire/JTAG Debug Port (SWJ-DP)					
TCK/SWCLK	Test Clock/Serial Wire Clock	Input		VDDIO	No pull-up resistor
TDI	Test Data In	Input			No pull-up resistor
TDO/TRACESWO	Test Data Out/Trace Asynchronous Data Out	Output[4]			
TMS/SWDIO	Test Mode Select/Serial Wire Input/Output	Input			No pull-up resistor
JTAGSEL	JTAG Selection	Input	High	VDDBU	Internal permanent pull-down

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Flash Memory					
ERASE	Flash and NVM Configuration Bits Erase Command	Input	High	VDDBU	Internal permanent 15K pulldown
Reset/Test					
NRST	Microcontroller Reset	I/O	Low	VDDIO	Internal permanent pullup
NRSTB	Asynchronous Microcontroller Reset	Input	Low	VDDBU	Internal permanent pullup
TST	Test Select	Input			Internal permanent pulldown
Universal Asynchronous Receiver Transceiver - UART					
URXD	UART Receive Data	Input			
UTXD	UART Transmit Data	Output			
PIO Controller - PIOA - PIOB - PIOC					
PA0–PA31	Parallel IO Controller A	I/O		VDDIO	Schmitt Trigger (1) Reset State: - PIO Input - Internal pullup enabled
PB0–PB31	Parallel IO Controller B	I/O			Schmitt Trigger (2) Reset State: - PIO Input - Internal pullup enabled
PC0–PC31	Parallel IO Controller C	I/O			Schmitt Trigger(3) Reset State: - PIO Input - Internal pullup enabled
External Bus Interface					
D0–D15	Data Bus	I/O			
A0–A23	Address Bus	Output			
NWAIT	External Wait Signal	Input	Low		
Static Memory Controller - SMC					
NCS0–NCS3	Chip Select Lines	Output	Low		
NWR0–NWR1	Write Signal	Output	Low		
NRD	Read Signal	Output	Low		
NWE	Write Enable	Output	Low		
NBS0–NBS1	Byte Mask Signal	Output	Low		

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
NAND Flash Controller - NFC					
NANDOE	NAND Flash Output Enable	Output	Low		
NANDWE	NAND Flash Write Enable	Output	Low		
NANDRDY	NAND Ready	Input			
High Speed Multimedia Card Interface - HSMCI					
CK	Multimedia Card Clock	I/O			
CDA	Multimedia Card Slot A Command	I/O			
DA0–DA7	Multimedia Card Slot A Data	I/O			
Universal Synchronous Asynchronous Receiver Transmitter - USARTx					
SCKx	USARTx Serial Clock	I/O			
TXDx	USARTx Transmit Data	I/O			
RXDx	USARTx Receive Data	Input			
RTSx	USARTx Request To Send	Output			
CTSx	USARTx Clear To Send	Input			
DTR0	USART0 Data Terminal Ready	I/O			
DSR0	USART0 Data Set Ready	Input			
DCD0	USART0 Data Carrier Detect	Input			
RI0	USART0 Ring Indicator	Input			
Synchronous Serial Controller - SSC					
TD	SSC Transmit Data	Output			
RD	SSC Receive Data	Input			
TK	SSC Transmit Clock	I/O			
RK	SSC Receive Clock	I/O			
TF	SSC Transmit Frame Sync	I/O			
RF	SSC Receive Frame Sync	I/O			
Timer/Counter - TC					
TCLKx	TC Channel x External Clock Input	Input			
TIOAx	TC Channel x I/O Line A	I/O			
TIOBx	TC Channel x I/O Line B	I/O			
Pulse Width Modulation Controller - PWMC					
PWMHx	PWM Waveform Output High for channel x	Output			
PWMLx	PWM Waveform Output Low for channel x	Output			Only output in complementary mode when dead time insertion is enabled
PWMFI0–2	PWM Fault Input	Input			

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Serial Peripheral Interface - SPI					
MISO	Master In Slave Out	I/O			
MOSI	Master Out Slave In	I/O			
SPCK	SPI Serial Clock	I/O			
NPCS0	SPI Peripheral Chip Select 0	I/O	Low		
NPCS1–NPCS3	SPI Peripheral Chip Select	Output	Low		
Two-Wire Interface - TWI					
TWDx	TWIx Two-wire Serial Data	I/O			
TWCKx	TWIx Two-wire Serial Clock	I/O			
12-bit Analog-to-Digital Converter - ADC12B					
AD12Bx	Analog Inputs	Analog			
AD12BTRG	ADC Trigger	Input			
AD12BVREF	ADC Reference	Analog			
10-bit Analog-to-Digital Converter - ADC					
ADx	Analog Inputs	Analog			
ADTRG	ADC Trigger	Input			
ADVREF	ADC Reference	Analog			
Fast Flash Programming Interface - FFPI					
PGMEN0–PGMEN2	Programming Enabling	Input		VDDIO	
PGMM0–PGMM3	Programming Mode	Input			
PGMD0–PGMD15	Programming Data	I/O			
PGMRDY	Programming Ready	Output	High		
PGMNVALID	Data Direction	Output	Low		
PGMNOE	Programming Read	Input	Low		
PGMCK	Programming Clock	Input			
PGMNCMD	Programming Command	Input	Low		
USB High Speed Device - UDPHS					
DFSDM	USB Device Full Speed Data -	Analog		VDDUTMI	
DFSDP	USB Device Full Speed Data +	Analog			
DHSDM	USB Device High Speed Data -	Analog			
DHSDP	USB Device High Speed Data +	Analog			

Notes:
1. PIOA: Schmitt Trigger on all except PA14 on 100 and 144-pin packages.
2. PIOB: Schmitt Trigger on all except PB9 to PB16, PB25 to PB31 on 100 and 144-pin packages.
3. PIOC: Schmitt Trigger on all except PC20 to PC27 on 144-pin package.
4. TDO pin is set in input mode when the Cortex-M3 Core is not in debug mode. Thus an external pull-up (100 kΩ) must be added to avoid current consumption due to floating input.

3.1 Design Considerations

To facilitate schematic capture when using a SAM3U design, refer to the application note *SAM3U Microcontroller Series Schematic Check List* (Atmel literature No. 11006). This application note and additonal documenation are available on www.atmel.com.

4. Package and Pinout

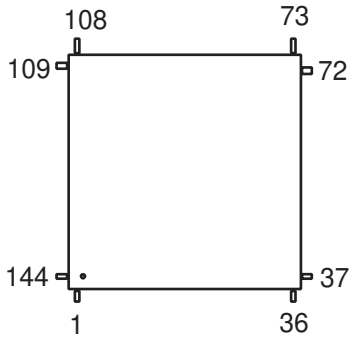
SAM3U4E / SAM3U2E / SAM3U1E devices are available in 144-lead LQFP and 144-ball LFBGA packages.

SAM3U4C / SAM3U2C / SAM3U1C devices are available in 100-lead LQFP and 100-ball TFBGA packages.

4.1 Package and Pinout (SAM3U4E / SAM3U2E / SAM3U1E Devices)

4.1.1 144-lead LQFP Package Outline

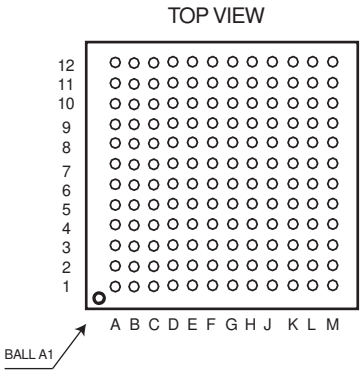
Figure 4-1. Orientation of the 144-lead LQFP Package



See Section 43.3 “144-lead LQFP Package” for mechanical drawings and specifications.

4.1.2 144-ball LFBGA Package Outline

Figure 4-2. Orientation of the 144-ball LFBGA Package



See Section 43.4 “144-ball LFBGA Package” for mechanical drawings and specifications.

4.1.3 144-lead LQFP Pinout

Table 4-1. 144-lead LQFP Pinout (SAM3U4E / SAM3U2E / SAM3U1E Devices)

1	TDI	37	DHSDP	73	VDDANA	109	PA0/PGMNCMD
2	VDDOUT	38	DHSDM	74	ADVREF	110	PC0
3	VDDIN	39	VBG	75	GNDANA	111	PA1/PGMRDY
4	TDO/TRACESWO	40	VDDUTMI	76	AD12BVREF	112	PC1
5	PB31	41	DFSDM	77	PA22/PGMD14	113	PA2/PGMNOE
6	PB30	42	DFSDP	78	PA30	114	PC2
7	TMS/SWDIO	43	GNDUTMI	79	PB3	115	PA3/PGMNVALID
8	PB29	44	VDDCORE	80	PB4	116	PC3
9	TCK/SWCLK	45	PA28	81	PC15	117	PA4/PGMM0
10	PB28	46	PA29	82	PC16	118	PC4
11	NRST	47	PC22	83	PC17	119	PA5/PGMM1
12	PB27	48	PA31	84	PC18	120	PC5
13	PB26	49	PC23	85	VDDIO	121	PA6/PGMM2
14	PB25	50	VDDCORE	86	VDDCORE	122	PC6
15	PB24	51	VDDIO	87	PA13/PGMD5	123	PA7/PGMM3
16	VDDCORE	52	GND	88	PA14/PGMD6	124	PC7
17	VDDIO	53	PB0	89	PC10	125	VDDCORE
18	GND	54	PC24	90	GND	126	GND
19	PB23	55	PB1	91	PA15/PGMD7	127	VDDIO
20	PB22	56	PC25	92	PC11	128	PA8/PGMD0
21	PB21	57	PB2	93	PA16/PGMD8	129	PC8
22	PC21	58	PC26	94	PC12	130	PA9/PGMD1
23	PB20	59	PB11	95	PA17/PGMD9	131	PC9
24	PB19	60	GND	96	PB16	132	PA10/PGMD2
25	PB18	61	PB12	97	PB15	133	PA11/PGMD3
26	PB17	62	PB13	98	PC13	134	PA12/PGMD4
27	VDDCORE	63	PC27	99	PA18/PGMD10	135	FWUP
28	PC14	64	PA27	100	PA19/PGMD11	136	SHDN
29	PB14	65	PB5	101	PA20/PGMD12	137	ERASE
30	PB10	66	PB6	102	PA21/PGMD13	138	TST
31	PB9	67	PB7	103	PA23/PGMD15	139	VDDBU
32	PC19	68	PB8	104	VDDIO	140	GNDBU
33	GNDPLL	69	PC28	105	PA24	141	NRSTB
34	VDDPLL	70	PC29	106	PA25	142	JTAGSEL
35	XOUT	71	PC30	107	PA26	143	XOUT32
36	XIN	72	PC31	108	PC20	144	XIN32

4.1.4 144-ball LFBGA Pinout

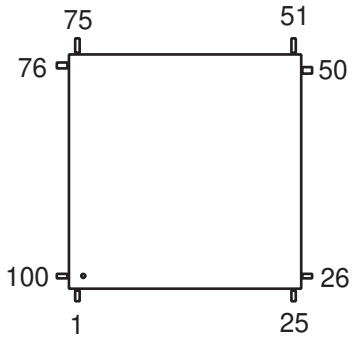
Table 4-2. 144-ball LFBGA Pinout (SAM3U4E / SAM3U2E / SAM3U1E Devices)

A1	VBG	D1	DFSDM	G1	PB0	K1	PB7
A2	VDDUTMI	D2	DHSDM	G2	PC26	K2	PC31
A3	PB9	D3	GNDPLL	G3	PB2	K3	PC29
A4	PB10	D4	PC14	G4	PC25	K4	PB3
A5	PB19	D5	PB21	G5	PB1	K5	PB4
A6	PC21	D6	PB23	G6	GND	K6	PA14/PGMD6
A7	PB26	D7	PB24	G7	GND	K7	PA16/PGMD8
A8	TCK/SWCLK	D8	PB28	G8	VDDCORE	K8	PA18/PGMD10
A9	PB30	D9	TDI	G9	PC4	K9	PC20
A10	TDO/TRACESWO	D10	VDDBU	G10	PA6/PGMM2	K10	PA1/PGMRDY
A11	XIN32	D11	PA10/PGMD2	G11	PA7/PGMM3	K11	PC1
A12	XOUT32	D12	PA11/PGMD3	G12	PC6	K12	PC2
B1	VDDCORE	E1	PC22	H1	PC24	L1	PC30
B2	GNDUTMI	E2	PA28	H2	PC27	L2	ADVREF
B3	XOUT	E3	PC19	H3	PA27	L3	AD12BVREF
B4	PB14	E4	VDDCORE	H4	PB12	L4	PA22/PGMD14
B5	PB17	E5	GND	H5	PB11	L5	PC17
B6	PB22	E6	VDDIO	H6	GND	L6	PC10
B7	PB25	E7	GNDBU	H7	VDDCORE	L7	PC12
B8	PB29	E8	NRST	H8	PB16	L8	PA19/PGMD11
B9	VDDIN	E9	PB31	H9	PB15	L9	PA23/PGMD15
B10	JTAGSEL	E10	PA12/PGMD4	H10	PC3	L10	PA0/PGMNCMD
B11	ERASE	E11	PA8/PGMD0	H11	PA5/PGMM1	L11	PA26
B12	SHDN	E12	PC8	H12	PC5	L12	PC0
C1	DFSDP	F1	PA31	J1	PB5	M1	VDDANA
C2	DHSDP	F2	PA29	J2	PB6	M2	GNDANA
C3	XIN	F3	PC23	J3	PC28	M3	PA30
C4	VDDPLL	F4	VDDCORE	J4	PB8	M4	PC15
C5	PB18	F5	VDDIO	J5	PB13	M5	PC16
C6	PB20	F6	GND	J6	VDDIO	M6	PC18
C7	PB27	F7	GND	J7	PA13/PGMD5	M7	PA15/PGMD7
C8	TMS/SWDIO	F8	VDDIO	J8	PA17/PGMD9	M8	PC11
C9	VDDOUT	F9	PC9	J9	PC13	M9	PA20/PGMD12
C10	NRSTB	F10	PA9/PGMD1	J10	PA2/PGMNOE	M10	PA21/PGMD13
C11	TST	F11	VDDCORE	J11	PA3/PGMNVALID	M11	PA24
C12	FWUP	F12	PC7	J12	PA4/PGMM0	M12	PA25

4.2 Package and Pinout (SAM3U4C / SAM3U2C / SAM3U1C Devices)

4.2.1 100-lead LQFP Package Outline

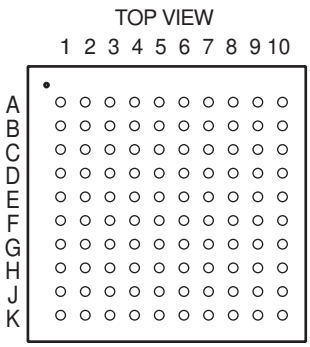
Figure 4-3. Orientation of the 100-lead LQFP Package



See Section 43.1 “100-lead LQFP Package” for mechanical drawings and specifications.

4.2.2 100-ball TFBGA Package Outline

Figure 4-4. Orientation of the 100-ball TFBGA Package



See Section 43.2 “100-ball TFBGA Package” for mechanical drawings and specifications.

4.2.3 100-lead LQFP Pinout

Table 4-3. 100-lead LQFP Pinout (SAM3U4C / SAM3U2C / SAM3U1C Devices)

1	VDDANA	26	PA0/PGMNCMD	51	TDI	76	DHSDP
2	ADVREF	27	PA1/PGMRDY	52	VDDOUT	77	DHSDM
3	GNDANA	28	PA2/PGMNOE	53	VDDIN	78	VBG
4	AD12BVREF	29	PA3/PGMNVALID	54	TDO/TRACESWO	79	VDDUTMI
5	PA22/PGMD14	30	PA4/PGMM0	55	TMS/SWDIO	80	DFSDM
6	PA30	31	PA5/PGMM1	56	TCK/SWCLK	81	DFSDP
7	PB3	32	PA6/PGMM2	57	NRST	82	GNDUTMI
8	PB4	33	PA7/PGMM3	58	PB24	83	VDDCORE
9	VDDCORE	34	VDDCORE	59	VDDCORE	84	PA28
10	PA13/PGMD5	35	GND	60	VDDIO	85	PA29
11	PA14/PGMD6	36	VDDIO	61	GND	86	PA31
12	PA15/PGMD7	37	PA8/PGMD0	62	PB23	87	VDDCORE
13	PA16/PGMD8	38	PA9/PGMD1	63	PB22	88	VDDIO
14	PA17/PGMD9	39	PA10/PGMD2	64	PB21	89	GND
15	PB16	40	PA11/PGMD3	65	PB20	90	PB0
16	PB15	41	PA12/PGMD4	66	PB19	91	PB1
17	PA18/PGMD10	42	FWUP	67	PB18	92	PB2
18	PA19/PGMD11	43	ERASE	68	PB17	93	PB11
19	PA20/PGMD12	44	TST	69	PB14	94	PB12
20	PA21/PGMD13	45	VDDBU	70	PB10	95	PB13
21	PA23/PGMD15	46	GNDBU	71	PB9	96	PA27
22	VDDIO	47	NRSTB	72	GNDPLL	97	PB5
23	PA24	48	JTAGSEL	73	VDDPLL	98	PB6
24	PA25	49	XOUT32	74	XOUT	99	PB7
25	PA26	50	XIN32	75	XIN	100	PB8

4.2.4 100-ball TFBGA Pinout

Table 4-4. 100-ball TFBGA Pinout (SAM3U4C / SAM3U2C / SAM3U1C Devices)

A1	VBG	C6	PB22	F1	PB1	H6	PA15/PGMD7
A2	XIN	C7	TMS/SWDIO	F2	PB12	H7	PA18/PGMD10
A3	XOUT	C8	NRSTB	F3	VDDIO	H8	PA24
A4	PB17	C9	JTAGSEL	F4	PA31	H9	PA1/PGMRDY
A5	PB21	C10	VDDBU	F5	VDDIO	H10	PA2/PGMNOE
A6	PB23	D1	DFSDM	F6	GND	J1	PB6
A7	TCK/SWCLK	D2	DHSDM	F7	PB16	J2	PB8
A8	VDDIN	D3	VDDPLL	F8	PA6/PGMM2	J3	ADVREF
A9	VDDOUT	D4	VDDCORE	F9	VDDCORE	J4	PA30
A10	XIN32	D5	PB20	F10	PA7/PGMM3	J5	PB3
B1	VDDCORE	D6	ERASE	G1	PB11	J6	PA16/PGMD8
B2	GNDUTMI	D7	TST	G2	PB2	J7	PA19/PGMD11
B3	VDDUTMI	D8	FWUP	G3	PB0	J8	PA21/PGMD13
B4	PB10	D9	PA11/PGMD3	G4	PB13	J9	PA26
B5	PB18	D10	PA12/PGMD4	G5	VDDCORE	J10	PA0/PGMNCMD
B6	PB24	E1	PA29	G6	GND	K1	PB7
B7	NRST	E2	GND	G7	PB15	K2	VDDANA
B8	TDO/TRACESWO	E3	PA28	G8	PA3/PGMNVALID	K3	GNDANA
B9	TDI	E4	PB9	G9	PA5/PGMM1	K4	AD12BVREF
B10	XOUT32	E5	GNDBU	G10	PA4/PGMM0	K5	PB4
C1	DFSDP	E6	VDDIO	H1	VDDCORE	K6	PA14/PGMD6
C2	DHSDP	E7	VDDCORE	H2	PB5	K7	PA17/PGMD9
C3	GNDPLL	E8	PA10/PGMD2	H3	PA27	K8	PA20/PGMD12
C4	PB14	E9	PA9/PGMD1	H4	PA22/PGMD14	K9	PA23/PGMD15
C5	PB19	E10	PA8/PGMD0	H5	PA13/PGMD5	K10	PA25

5. Power Considerations

5.1 Power Supplies

The SAM3U product power supply pins are the following:

- VDDCORE pins: Power the core, the embedded memories and the peripherals; voltage range 1.62–1.95 V
- VDDIO pins: Power the peripherals I/O lines; voltage range 1.62–3.6 V
- VDDIN pin: Powers the voltage regulator
- VDDOUT pin: Output of the voltage regulator
- VDDBU pin: Powers the Slow Clock oscillator and a part of the System Controller; voltage range 1.62– 3.6V. VDDBU must be supplied before or at the same time as VDDIO and VDDCORE.
- VDDPLL pin: Powers the PLL A, UPLL and 3–20 MHz Oscillator; voltage range 1.62–1.95 V
- VDDUTMI pin: Powers the UTMI+ interface; voltage range 3.0–3.6 V, 3.3V nominal
- VDDANA pin: Powers the ADC cells; voltage range 2.0–3.6 V

Ground pins GND are common to VDDCORE and VDDIO pins power supplies.

Separated ground pins are provided for VDDBU, VDDPLL, VDDUTMI and VDDANA. These ground pins are respectively GNDBU, GNDPLL, GNDUTMI and GNDANA.

5.2 Power-up Considerations

5.2.1 VDDIO Versus VDDCORE

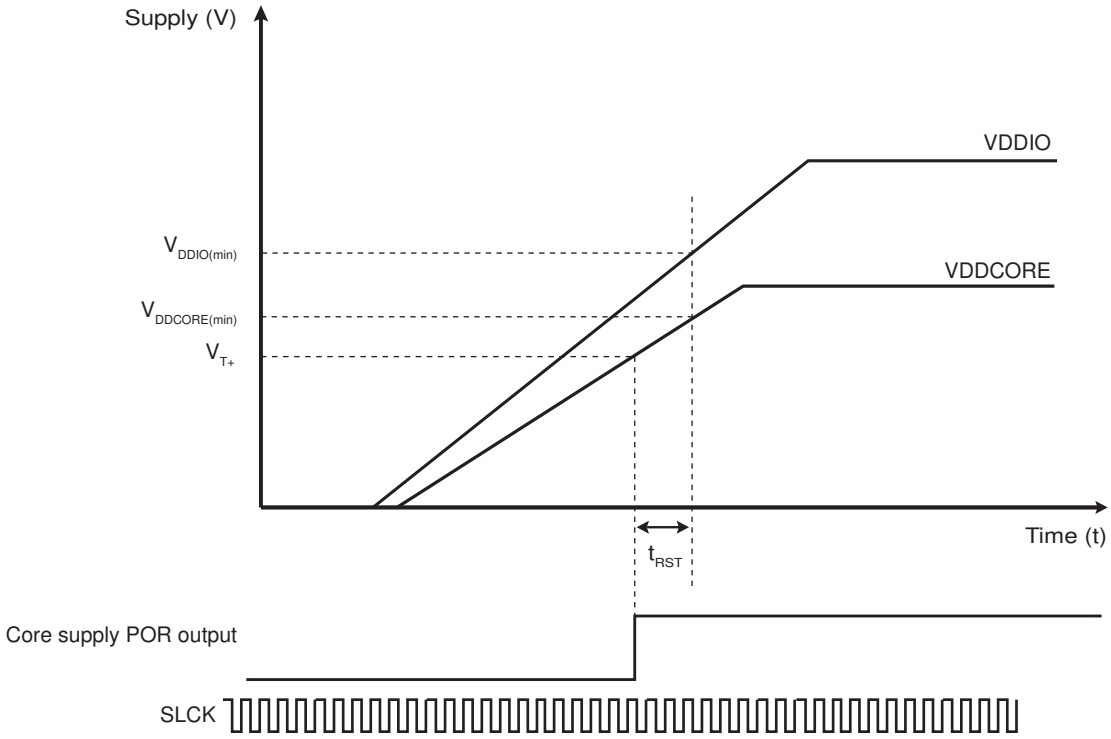
V_{DDIO} must always be higher or equal to V_{DDCORE}.

V_{DDIO} must reach its minimum operating voltage (1.60 V) before V_{DDCORE} has reached $V_{DDCORE(min)}$. The minimum slope for V_{DDCORE} is defined by $(V_{DDCORE(min)} - V_{T+}) / t_{RST}$.

If V_{DDCORE} rises at the same time as V_{DDIO}, the V_{DDIO} rising slope must be higher than or equal to 5V/ms.

If VDDCORE is powered by the internal regulator, all power-up considerations are met.

Figure 5-1. VDDCORE and VDDIO Constraints at Startup



5.2.2 VDDIO Versus VDDIN

At power-up, V_{DDIO} needs to reach 0.6 V before V_{DDIN} reaches 1.0 V.

VDDIO voltage needs to be equal to or below (VDDIN voltage + 0.5 V).

5.3 Voltage Regulator

The SAM3U embeds a voltage regulator that is managed by the Supply Controller.

This internal regulator is intended to supply the internal core of SAM3U but can be used to supply other parts in the application. It features two different operating modes:

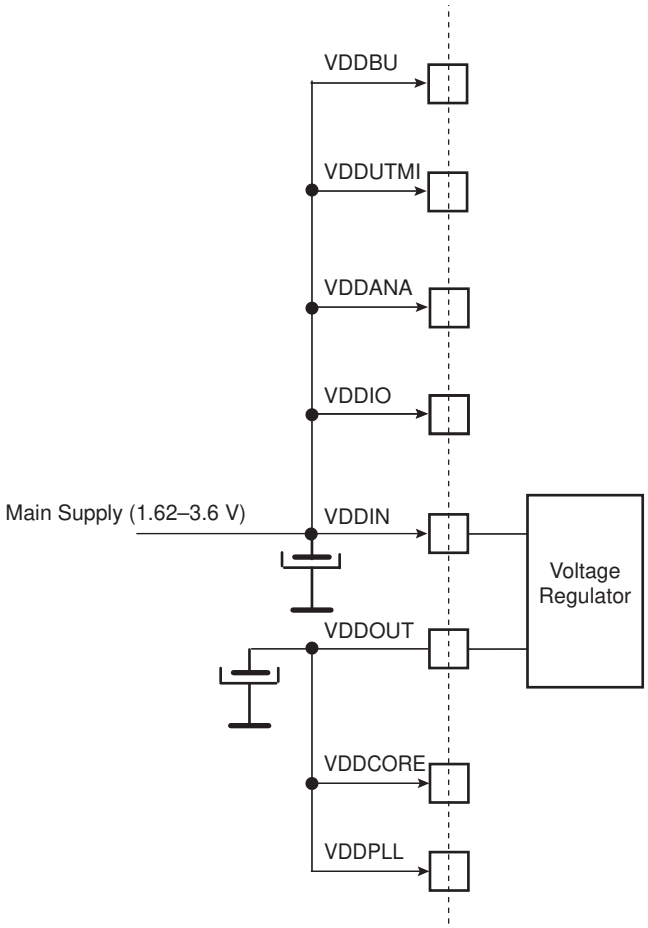
- In Normal mode, the voltage regulator consumes less than 700 µA static current and draws 150 mA of output current. Internal adaptive biasing adjusts the regulator quiescent current depending on the required load current. In Wait mode or when the output current is low, quiescent current is only 7 µA.
- In Shutdown mode, the voltage regulator consumes less than 1 µA while its output is driven internally to GND. The default output voltage is 1.80 V and the startup time to reach Normal mode is inferior to 400 µs.

For adequate input and output power supply decoupling/bypassing, refer to Table 42-3, “1.8V Voltage Regulator Characteristics,” on page 1089.

5.4 Typical Powering Schematics

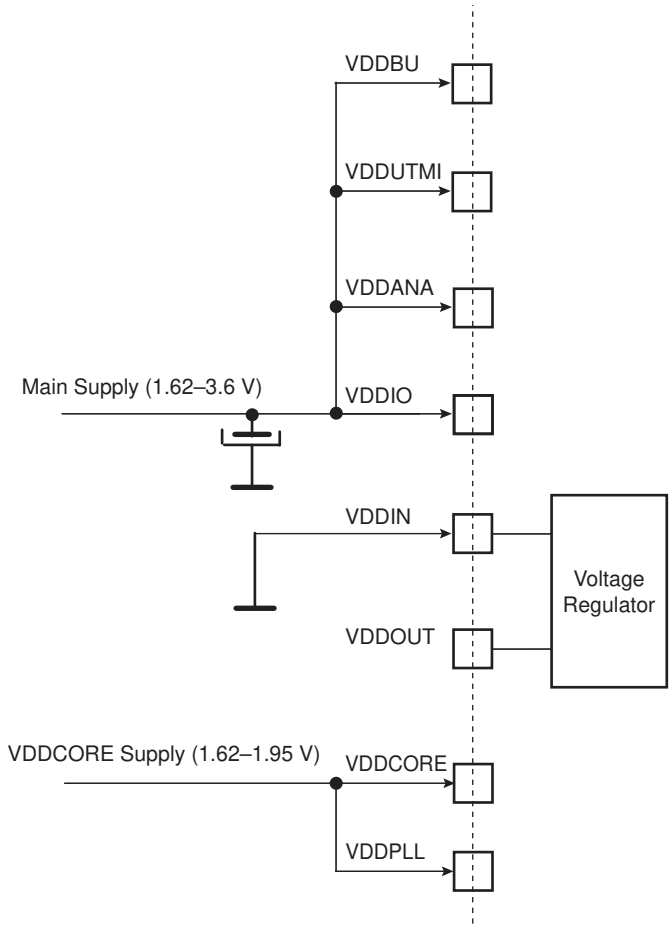
The SAM3U supports a 1.62–3.6 V single supply mode. The internal regulator input connected to the source and its output feed VDDCORE. Figure 5-2, Figure 5-3, and Figure 5-4 show the power schematics.

Figure 5-2. Single Supply



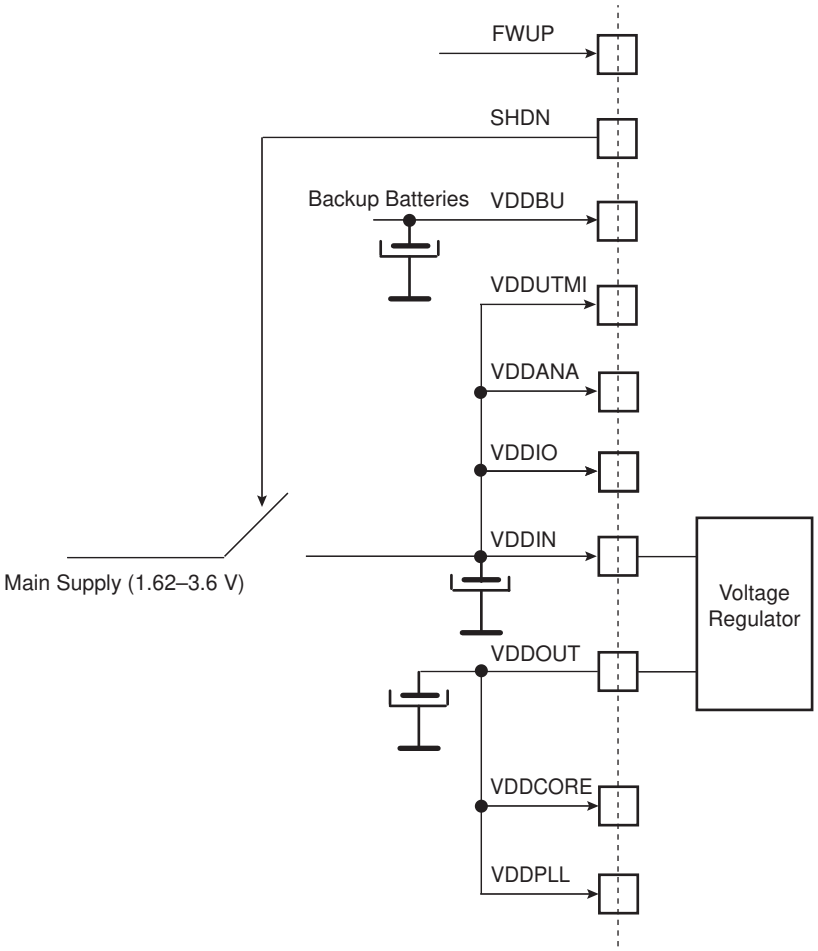
Note: Restrictions:
With Main Supply < 2.0 V, USB and ADC are not usable.
With Main Supply ≥ 2.4V and < 3V, USB is not usable.
With Main Supply ≥ 3V, all peripherals are usable.

Figure 5-3. Core Externally Supplied



Note: Restrictions:
With Main Supply < 2.0 V, USB and ADC are not usable.
With Main Supply ≥ 2.4V and < 3V, USB is not usable.
With Main Supply ≥ 3V, all peripherals are usable.

Figure 5-4. Backup Batteries Used



Note: Restrictions
With Main Supply < 2.0 V, USB and ADC are not usable.
With Main Supply ≥ 2.4V and < 3V, USB is not usable.
With Main Supply ≥ 3V, all peripherals are usable.

5.5 Active Mode

Active mode is the normal running mode with the core clock running from the fast RC oscillator, the main crystal oscillator or the PLLA. The power management controller can be used to adapt the frequency and to disable the peripheral clocks.

5.6 Low-power Modes

The SAM3U has the following low-power modes: Backup, Wait, and Sleep.

5.6.1 Backup Mode

The purpose of backup mode is to achieve the lowest power consumption possible in a system which is performing periodic wake-ups to perform tasks but not requiring fast startup time (< 0.5 ms).

The Supply Controller, zero-power power-on reset, RTT, RTC, backup registers and 32 kHz oscillator (RC or crystal oscillator selected by software in the Supply Controller) are running. The regulator and the core supply are off.

Backup mode is based on the Cortex-M3 deep-sleep mode with the voltage regulator disabled.

The SAM3U Series can be woken up from this mode through the Force Wake-Up (FWUP) pin, and Wake-Up input pins WKUP0–15, Supply Monitor, RTT or RTC wake-up event. Current consumption is 2.5 µA typical on VDDBU.

Backup mode can be entered by using the WFE instruction.

The procedure to enter Backup mode using the WFE instruction is the following:

1. Write a 1 to the SLEEPDEEP bit in the Cortex-M3 processor System Control Register (SCR) (refer to Section 12.20.7 ”System Control Register”).
2. Execute the WFE instruction of the processor.

Exit from Backup mode happens if one of the following enable wake-up events occurs:

- Low level, configurable debouncing on FWUP pin
- Level transition, configurable debouncing on pins WKUPEN0–15
- SM alarm
- RTC alarm
- RTT alarm

5.6.2 Wait Mode

The purpose of the Wait mode is to achieve very low power consumption while maintaining the whole device in a powered state for a startup time of less than 10 µs.

In this mode, the clocks of the core, peripherals and memories are stopped. However, the core, peripherals and memories power supplies are still powered. From this mode, a fast start up is available.

This mode is entered via Wait for Event (WFE) instructions with LPM = 1 (Low Power Mode bit in PMC_FSMR). The Cortex-M3 is able to handle external events or internal events in order to wake up the core (WFE). This is done by configuring the external lines WKUP0–15 as fast startup wake-up pins (refer to Section 5.8 “Fast Startup”). RTC or RTT Alarm and USB wake-up events can be used to wake up the CPU (exit from WFE).

Current Consumption in Wait mode is typically 15 µA on VDDIN if the internal voltage regulator is used or 8 µA on VDDCORE if an external regulator is used.

The procedure to enter Wait mode is the following:

1. Select the 4/8/12 MHz fast RC oscillator as Main Clock
2. Set the LPM bit in PMC_FSMR
3. Execute the WFE instruction of the processor

Note: Internal Main clock resynchronization cycles are necessary between the writing of MOSCRCEN bit and the effective entry in Wait mode. Depending on the user application, waiting for MOSCRCEN bit to be cleared is recommended to ensure that the core will not execute undesired instructions.

5.6.3 Sleep Mode

The purpose of sleep mode is to optimize power consumption of the device versus response time. In this mode, only the core clock is stopped. The peripheral clocks can be enabled. This mode is entered via Wait for Interrupt (WFI) or WFE instructions with LPM = 0 in PMC_FSMR.

The processor can be woken up from an interrupt if WFI instruction of the Cortex-M3 is used, or from an event if the WFE instruction is used to enter this mode.

5.6.4 Low-power Mode Summary Table

The modes detailed above are the main low-power modes. Each part can be set to on or off separately and wake up sources can be individually configured. Table 5-1 shows a summary of the configurations of the low-power modes.

Table 5-1. Low Power Mode Configuration Summary

Mode	SUPC, 32 kHz Osc., RTC, RTT, GPBR, POR (VDDBU Region)	Regulator	Core Memory Peripherals	Mode Entry	Potential Wake-up Sources	Core at Wake-up	PIO State While in Low Power Mode	PIO State at Wake-up	Consumption (2) (3)	Wake-up Time(1)
Backup Mode	ON	OFF SHDN = 0	OFF (Not powered)	WFE + SLEEPDEEP = 1	FWUP pin Pins WKUP0–15 SM alarm RTC alarm RTT alarm	Reset	Previous state saved	PIOA & PIOB & PIOC Inputs with pull-ups	2.5 µA typ(4)	< 0.5 ms
Wait Mode	ON	ON SHDN = 1	Powered (Not clocked)	WFE + SLEEPDEEP = 0 + LPM = 1	Any event from: - Fast startup through pins WKUP0–15 - RTC alarm - RTT alarm - USB wake-up	Clocked back	Previous state saved	Unchanged	13 µA/20 µA(5)	< 10 µs
Sleep Mode	ON	ON SHDN = 1	Powered(7) (Not clocked)	WFE or WFI + SLEEPDEEP = 0 + LPM = 0	Entry mode = WFI interrupt only; Entry mode = WFE any enabled interrupt and/or Any event from: - Fast startup through pins WKUP0–15 - RTC alarm - RTT alarm - USB wake-up	Clocked back	Previous state saved	Unchanged	(6)	(6)

Notes:
1. When considering wake-up time, the time required to start the PLL is not taken into account. Once started, the device works with the 4/8/12 MHz Fast RC oscillator. The user has to add the PLL startup time if it is needed in the system. The wake-up time is defined as the time taken for wake-up until the first instruction is fetched.
2. The external loads on PIOs are not taken into account in the calculation.
3. BOD current consumption is not included.
4. Current consumption on VDDBU.
5. 13 µA total current consumption - **without** using internal voltage regulator.
   20 µA total current consumption - **using** internal voltage regulator.
6. Depends on MCK frequency.
7. In this mode the core is supplied and not clocked but some peripherals can be clocked.

5.7 Wake-up Sources

The wake-up events allow the device to exit Backup mode. When a wake-up event is detected, the Supply Controller performs a sequence which automatically reenables the core power supply. See Figure 18-7 “Wake Up Sources” on page 273.

5.8 Fast Startup

The SAM3U device allows the processor to restart in a few microseconds while the processor is in Wait mode. A fast startup can occur upon detection of a low level on one of the 19 wake-up inputs (WKUP0 to 15 + RTC + RTT + USB).

The fast restart circuitry (shown in Figure 27-3 “Fast Startup Circuitry” on page 454) is fully asynchronous and provides a fast startup signal to the Power Management Controller. As soon as the fast startup signal is asserted, the PMC automatically restarts the embedded 4/8/12 MHz fast RC oscillator, switches the master clock on this 4 MHz clock by default and reenables the processor clock.

6. Input/Output Lines

The SAM3U has different kinds of input/output (I/O) lines, such as general purpose I/Os (GPIO) and system I/Os. GPIOs can have alternate functions thanks to multiplexing capabilities of the PIO controllers. The same GPIO line can be used whether it is in IO mode or used by the multiplexed peripheral. System I/Os are pins such as test pin, oscillators, erase pin, analog inputs or debug pins.

With a few exceptions, the I/Os have input Schmitt triggers. Refer to the footnotes associated with “PIO Controller - PIOA - PIOB - PIOC” on page 7 within Table 3-1, “Signal Description List”.

6.1 General Purpose I/O Lines (GPIO)

GPIO Lines are managed by PIO controllers. All I/Os have several input or output modes such as, pull-up, input Schmitt triggers, multi-drive (open-drain), glitch filters, debouncing or input change interrupt. Programming of these modes is performed independently for each I/O line through the PIO controller user interface. For more details, refer to Section 29. ”Parallel Input/Output Controller (PIO)”.

The input output buffers of the PIO lines are supplied through VDDIO power supply rail.

The SAM3U embeds high-speed pads able to handle up to 65 MHz for HSMCI and SPI clock lines and 35 MHz on other lines. See Section 42.9 ”AC Characteristics” for more details. Typical pull-up value is 100 kΩ for all I/Os.

Each I/O line also embeds an ODT (On-Die Termination) (see Figure 6-1). ODT consists of an internal series resistor termination scheme for impedance matching between the driver output (SAM3) and the PCB track impedance preventing signal reflection. The series resistor helps to reduce I/Os switching current (di/dt) thereby reducing in turn, EMI. It also decreases overshoot and undershoot (ringing) due to inductance of interconnect between devices or between boards. In conclusion, ODT helps reducing signal integrity issues.

Figure 6-1. On-Die Termination Schematic