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SAM3X / SAM3A Series

Atmel | SMART ARM-based MCU

DATASHEET

Description

The Atmel® | SMART SAM3X/A series is a member of a family of Flash microcontrollers based on the high performance 32-bit ARM® Cortex®-M3 RISC processor. It operates at a maximum speed of 84 MHz and features up to 512 Kbytes of Flash and up to 100 Kbytes of SRAM. The peripheral set includes a High Speed USB Host and Device port with embedded transceiver, an Ethernet MAC, 2 CANs, a High Speed MCI for SDIO/SD/MMC, an External Bus Interface with NAND Flash Controller (NFC), 5 UARTs, 2 TWIs, 4 SPIs, as well as a PWM timer, three 3-channel general-purpose 32-bit timers, a low-power RTC, a low-power RTT, 256-bit General Purpose Backup Registers, a 12-bit ADC and a 12-bit DAC.

The SAM3X/A devices have three software-selectable low-power modes: Sleep, Wait and Backup. In Sleep mode, the processor is stopped while all other functions can be kept running. In Wait mode, all clocks and functions are stopped but some peripherals can be configured to wake up the system based on predefined conditions. In Backup mode, only the RTC, RTT, and wake-up logic are running.

The SAM3X/A series is ready for capacitive touch thanks to the QTouch library, offering an easy way to implement buttons, wheels and sliders.

The SAM3X/A architecture is specifically designed to sustain high-speed data transfers. It includes a multi-layer bus matrix as well as multiple SRAM banks, PDC and DMA channels that enable it to run tasks in parallel and maximize data throughput.

The device operates from 1.62V to 3.6V and is available in 100 and 144-lead LQFP, 100-ball TFBGA and 144-ball LFBGA packages.

The SAM3X/A devices are particularly well suited for networking applications: industrial and home/building automation, gateways.

1. Features

- Core
  - ARM Cortex-M3 revision 2.0 running at up to 84 MHz
  - Memory Protection Unit (MPU)
  - Thumb®-2 instruction set
  - 24-bit SysTick Counter
  - Nested Vector Interrupt Controller
- Memories
  - 256 to 512 Kbytes embedded Flash, 128-bit wide access, memory accelerator, dual bank
  - 32 to 100 Kbytes embedded SRAM with dual banks
  - 16 Kbytes ROM with embedded bootloader routines (UART, USB) and IAP routines
  - Static Memory Controller (SMC): SRAM, NOR, NAND support. NFC with 4 Kbyte RAM buffer and ECC
- System
  - Embedded voltage regulator for single supply operation
  - Power-on-Reset (POR), Brown-out Detector (BOD) and Watchdog for safe reset
  - Quartz or ceramic resonator oscillators: 3 to 20 MHz main and optional low power 32.768 kHz for RTC or device clock
  - High precision 8/12 MHz factory trimmed internal RC oscillator with 4 MHz default frequency for fast device startup
  - Slow Clock Internal RC oscillator as permanent clock for device clock in low-power mode
  - One PLL for device clock and one dedicated PLL for USB 2.0 High Speed Mini Host/Device
  - Temperature Sensor
  - Up to 17 peripheral DMA (PDC) channels and 6-channel central DMA plus dedicated DMA for High-Speed USB Mini Host/Device and Ethernet MAC
- Low-power Modes
  - Sleep, Wait and Backup modes, down to 2.5 µA in Backup mode with RTC, RTT, and GPBR
- Peripherals
  - USB 2.0 Device/Mini Host: 480 Mbps, 4 Kbyte FIFO, up to 10 bidirectional Endpoints, dedicated DMA
  - Up to 4 USARTs (ISO7816, IrDA®, Flow Control, SPI, Manchester and LIN support) and one UART
  - 2 TWI (I2C compatible), up to 6 SPIs, 1 SSC (I2S), 1 HSMCI (SDIO/SD/MMC) with up to 2 slots
  - 9-channel 32-bit Timer Counter (TC) for capture, compare and PWM mode, Quadrature Decoder Logic and 2-bit Gray Up/Down Counter for Stepper Motor
  - Up to 8-channel 16-bit PWM (PWMC) with Complementary Output, Fault Input, 12-bit Dead Time Generator Counter for Motor Control
  - 32-bit low-power Real-time Timer (RTT) and low-power Real-time Clock (RTC) with calendar and alarm features
  - 256-bit General Purpose Backup Registers (GPBR)
  - 16-channel 12-bit 1 msps ADC with differential input mode and programmable gain stage
  - 2-channel 12-bit 1 msps DAC
  - Ethernet MAC 10/100 (EMAC) with dedicated DMA
  - 2 CAN Controllers with 8 Mailboxes
  - True Random Number Generator (TRNG)
  - Register Write Protection
- I/O
  - Up to 103 I/O lines with external interrupt capability (edge or level sensitivity), debouncing, glitch filtering and on-die Series Resistor Termination
  - Up to six 32-bit Parallel Input/Outputs (PIO)

- Packages
  - 100-lead LQFP – 14 x 14 mm, pitch 0.5 mm
  - 100-ball TFBGA – 9 x 9 mm, pitch 0.8 mm
  - 144-lead LQFP – 20 x 20 mm, pitch 0.5 mm
  - 144-ball LFBGA – 10 x 10 mm, pitch 0.8 mm

1.1 Configuration Summary

The SAM3X/A series devices differ in memory sizes, package and features list. Table 1-1 summarizes the configurations.

Table 1-1. Configuration Summary

Feature	SAM3X8E	SAM3X8C	SAM3X4E	SAM3X4C	SAM3A8C	SAM3A4C
Flash	2 x 256 Kbytes	2 x 256 Kbytes	2 x 128 Kbytes	2 x 128 Kbytes	2 x 256 Kbytes	2 x 128 Kbytes
SRAM	64 + 32 Kbytes	64 + 32 Kbytes	32 + 32 Kbytes	32 + 32 Kbytes	64 + 32 Kbytes	32 + 32 Kbytes
NAND Flash Controller (NFC)	Yes	–	Yes	–	–	–
NFC SRAM(1)	4 Kbytes	–	4 Kbytes	–	–	–
Package	LQFP144 LFBGA144	LQFP100 TFBGA100	LQFP144 LFBGA144	LQFP100 TFBGA100	LQFP100 TFBGA100	LQFP100 TFBGA100
Number of PIOs	103	63	103	63	63	63
SHDN Pin	Yes	No	Yes	No	No	No
EMAC	MII/RMII	RMII	MII/RMII	RMII	–	–
External Bus Interface	16-bit data, 8 chip selects, 23-bit address	–	16-bit data, 8 chip selects, 23-bit address	–	–	–
SDRAM Controller(6)	–	–	–	–	–	–
Central DMA	6	4	6	4	4	4
12-bit ADC	16 ch.(2)	16 ch.(2)	16 ch.(2)	16 ch.(2)	16 ch.(2)	16 ch.(2)
12-bit DAC	2 ch.	2 ch.	2 ch.	2 ch.	2 ch.	2 ch.
32-bit Timer	9 ch.(3)	9 ch.(4)	9 ch.(3)	9 ch.(4)	9 ch.(3)	9 ch.(3)
PDC Channels	17	15	17	15	15	15
USART/UART	3/2(5)	3/1	3/2(5)	3/1	3/1	3/1
SPI	1 SPI controller, 4 chip selects + 3 USART with SPI mode	1 SPI controller, 4 chip selects + 3 USART with SPI mode	1 SPI controller, 4 chip selects + 3 USART with SPI mode	1 SPI controller, 4 chip selects + 3 USART with SPI mode	1 SPI controller, 4 chip selects + 3 USART with SPI mode	1 SPI controller, 4 chip selects + 3 USART with SPI mode
HSMCI	1 slot, 8 bits	1 slot, 4 bits	1 slot, 8 bits	1 slot, 4 bits	1 slot, 4 bits	1 slot, 4 bits

Notes:
1. 4 Kbytes RAM buffer of the NFC which can be used by the core if not used by the NFC
2. One channel is reserved for internal temperature sensor
3. Six TC channels are accessible through PIO
4. Three TC channels are accessible through PIO
5. USART3 in UART mode (RXD3 and TXD3 available)
6. Available only on SAM3X8H in LFBGA217 package, which is mounted on SAM3X-EK evaluation kit for SAM3X and SAM3A series. The SAM3X8H device is not commercially available.

2. SAM3X/A Block Diagram

Figure 2-1. SAM3A4/8C (100 pins) Block Diagram

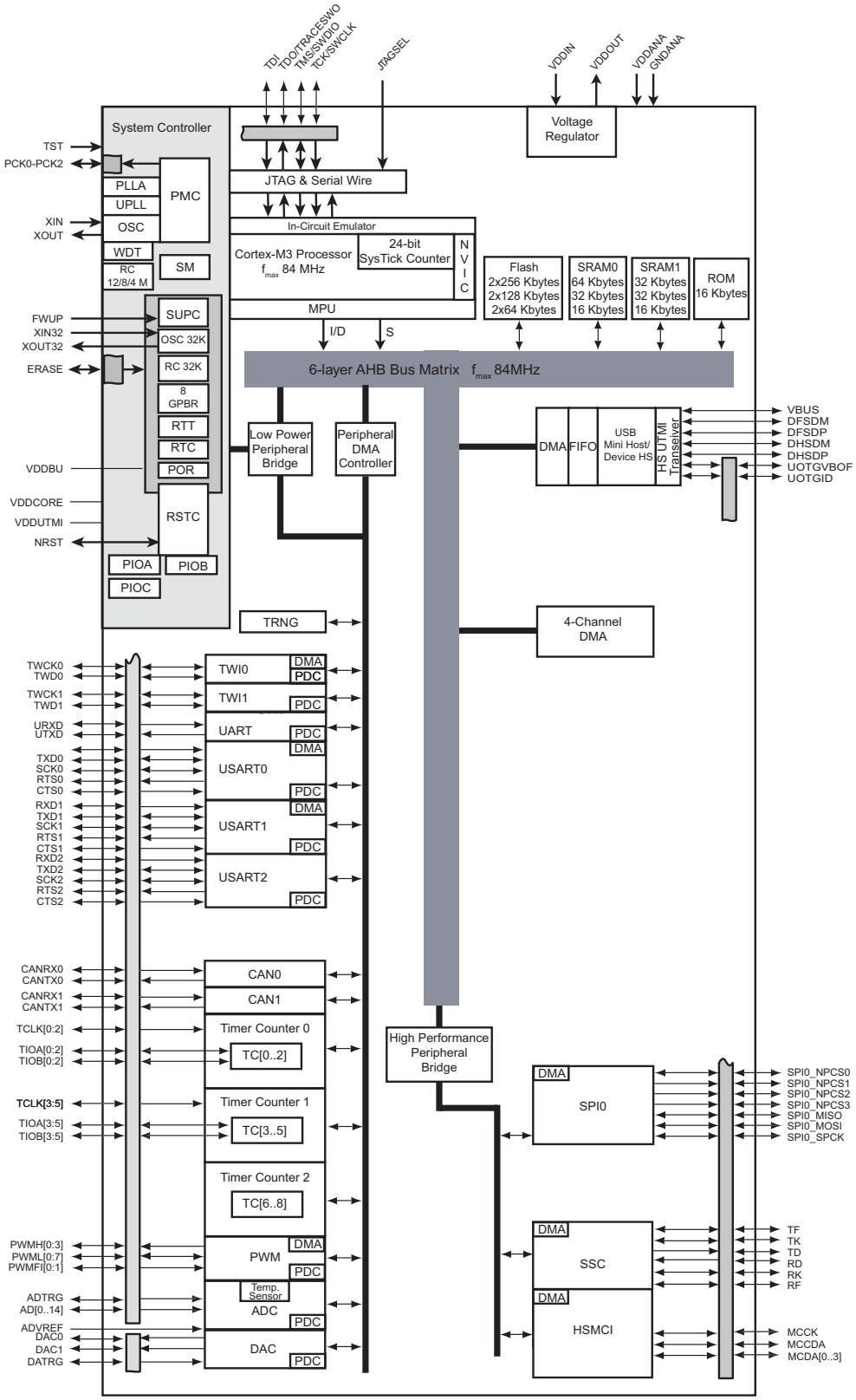


Figure 2-2. SAM3X4/8C (100 pins) Block Diagram

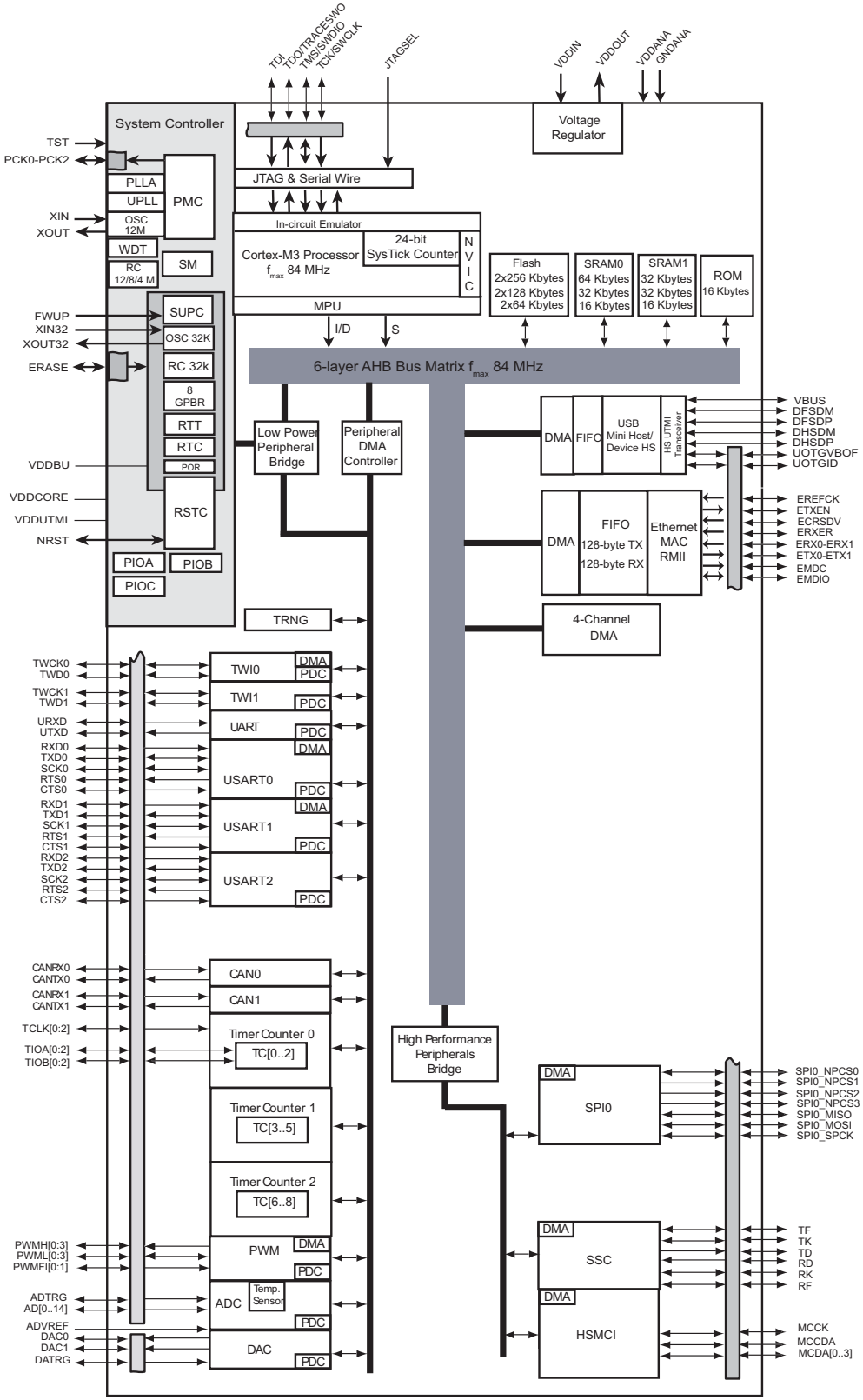


Figure 2-3. SAM3X4/8E (144 pins) Block Diagram

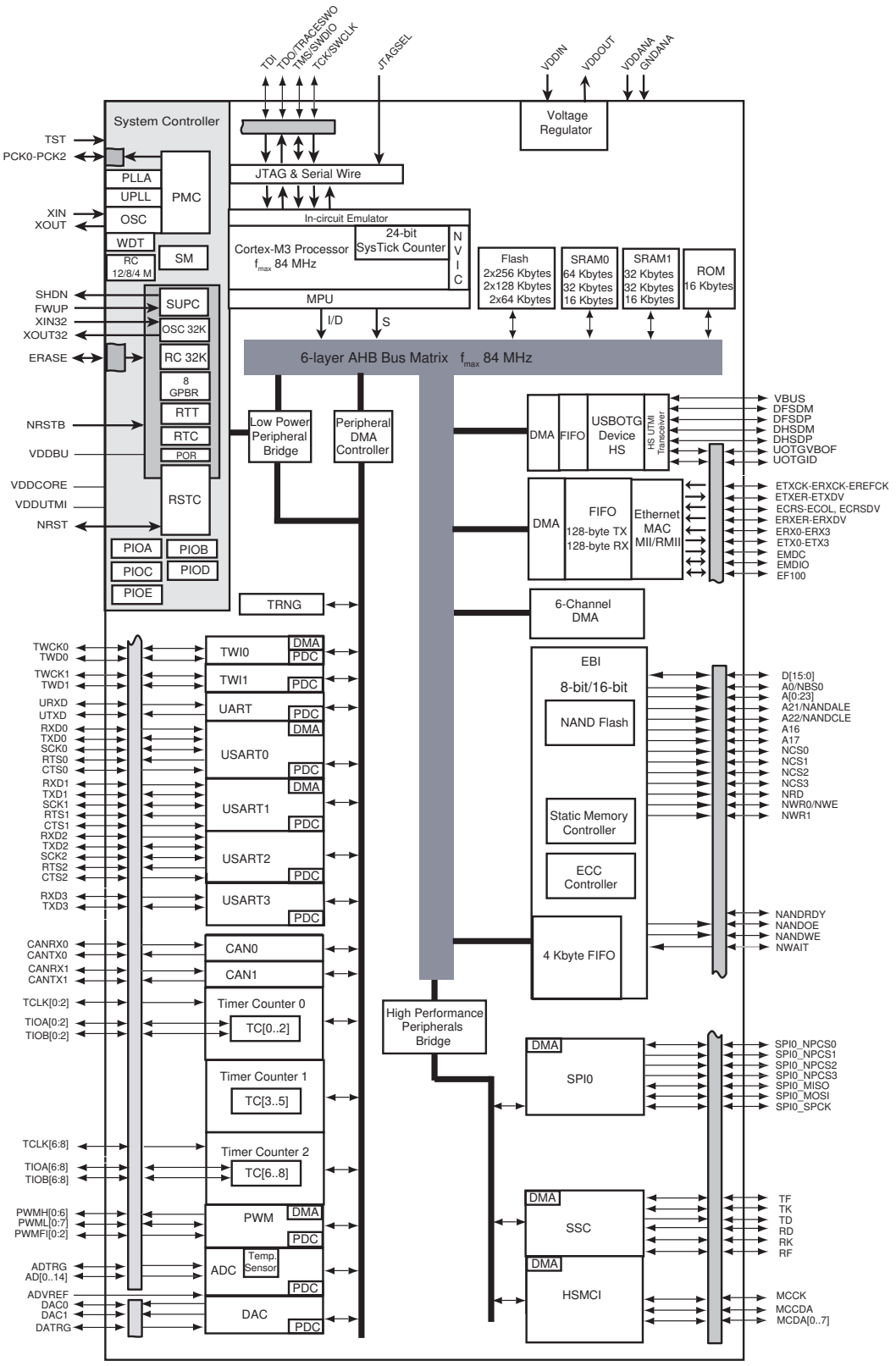
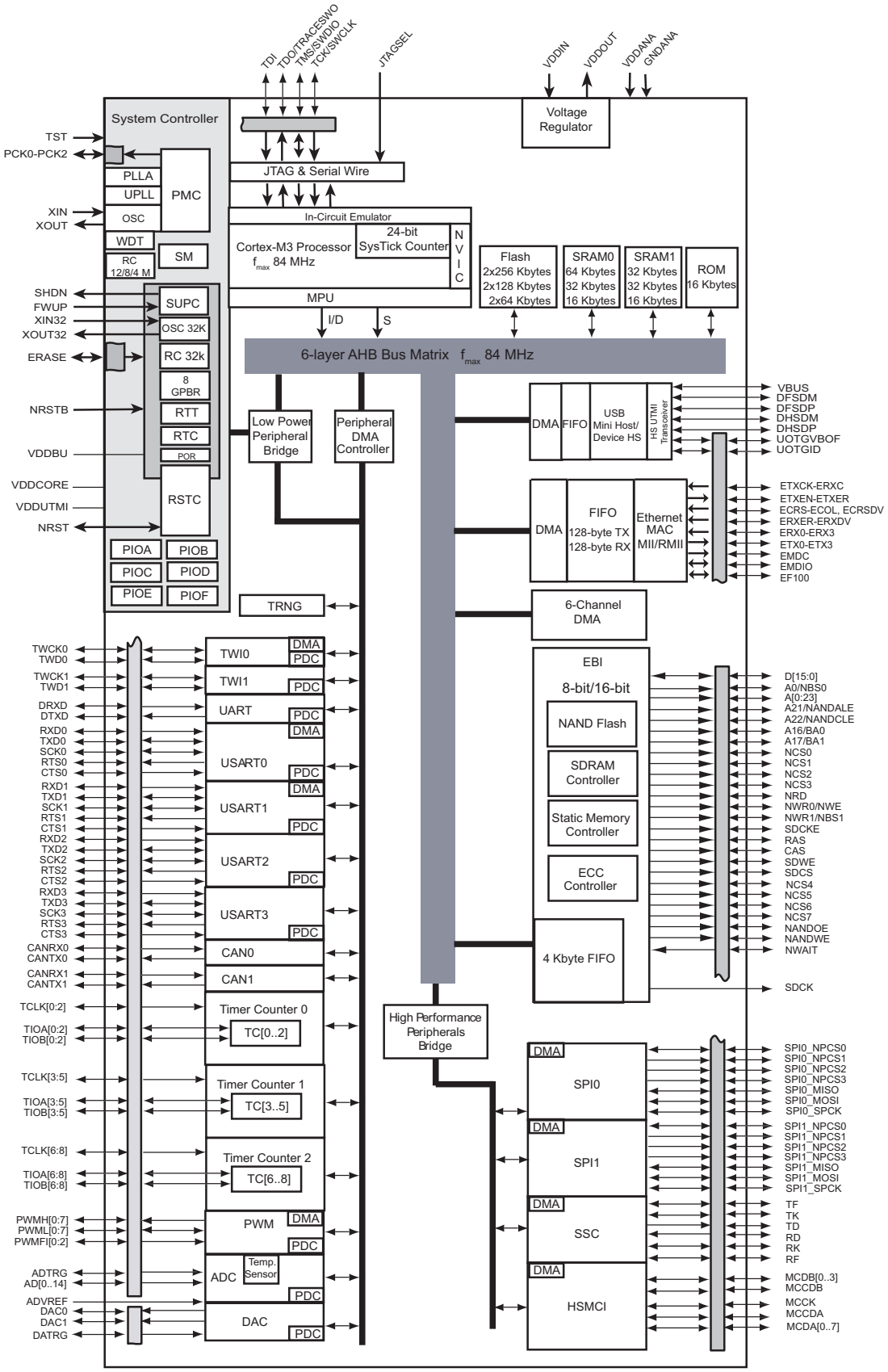


Figure 2-4. SAM3X8H (217 pins) Block Diagram (not commercially available)



3. Signal Description

Table 3-1 gives details on the signal names classified by peripheral.

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Power Supplies					
VDDIO	Peripherals I/O Lines Power Supply	Power			1.62V to 3.6V
VDDUTMI	USB UTMI+ Interface Power Supply	Power			3.0V to 3.6V
VDDOUT	Voltage Regulator Output	Power			
VDDIN	Voltage Regulator, ADC and DAC Power Supply	Power			
GNDUTMI	USB UTMI+ Interface Ground	Ground			
VDDBU	Backup I/O Lines Power Supply	Power			1.62V to 3.6V
GNDBU	Backup Ground	Ground			
VDDPLL	PLL A, UPLL and Oscillator Power Supply	Power			1.62 V to 1.95V
GNDPLL	PLL A, UPLL and Oscillator Ground	Ground			
VDDANA	ADC and DAC Analog Power Supply	Power			2.0V to 3.6V
GNDANA	ADC and DAC Analog Ground	Ground			
VDDCORE	Core Chip Power Supply	Power			1.62V to 1.95V
GND	Ground	Ground			
Clocks, Oscillators and PLLs					
XIN	Main Oscillator Input	Input		VDDPLL	
XOUT	Main Oscillator Output	Output			
XIN32	Slow Clock Oscillator Input	Input		VDDBU	
XOUT32	Slow Clock Oscillator Output	Output			
VBG	Bias Voltage Reference	Analog			
PCK0–PCK2	Programmable Clock Output	Output			
Shutdown, Wakeup Logic					
SHDN	Shut-Down Control	Output		VDDBU	0: Device is in backup mode 1: Device is running (not in backup mode)
FWUP	Force Wake-up Input	Input		VDDBU	Needs external pull-up

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
ICE and JTAG					
TCK/SWCLK	Test Clock/Serial Wire Clock	Input		VDDIO	Reset State: - SWJ-DP Mode - Internal pull-up disabled[1]
TDI	Test Data In	Input			
TDO/TRACESWO	Test Data Out / Trace Asynchronous Data Out	Output			
TMS/SWDIO	Test Mode Select /Serial Wire Input/Output	Input / I/O			
JTAGSEL	JTAG Selection	Input	High	VDDBU	Permanent Internal pull-down
Flash Memory					
ERASE	Flash and NVM Configuration Bits Erase Command	Input	High	VDDIO	Pull-down resistor
Reset/Test					
NRST	Microcontroller Reset	I/O	Low	VDDIO	Pull-up resistor
NRSTB	Asynchronous Microcontroller Reset	Input	Low	VDDBU	Pull-up resistor
TST	Test Mode Select	Input		VDDBU	Pull-down resistor
Universal Asynchronous Receiver Transceiver - UART					
URXD	UART Receive Data	Input			
UTXD	UART Transmit Data	Output			
PIO Controller - PIOA - PIOB - PIOC - PIOD - PIOE - PIOF					
PA0–PA31	Parallel IO Controller A	I/O		VDDIO	Schmitt Trigger[3] Reset State: - PIO Input - Internal pull-up enabled
PB0–PB31	Parallel IO Controller B	I/O			Schmitt Trigger[4] Reset State: - PIO Input - Internal pull-up enabled
PC0–PC30	Parallel IO Controller C	I/O			Schmitt Trigger[5] Reset State: - PIO Input - Internal pull-up enabled
PD0–PD30	Parallel IO Controller D	I/O			Schmitt Trigger[6] Reset State: - PIO Input - Internal pull-up enabled
PE0–PE31	Parallel IO Controller E	I/O			Schmitt Trigger[7] Reset State: - PIO Input - Internal pull-up enabled
PF0–PF6	Parallel IO Controller F	I/O			Schmitt Trigger[7] Reset State: - PIO Input - Internal pull-up enabled

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
External Memory Bus					
D0–D15	Data Bus	I/O			Pulled-up input at reset
A0–A23	Address Bus	Output			0 at reset
Static Memory Controller - SMC					
NCS0–NCS7	Chip Select Lines	Output	Low		
NWR0–NWR1	Write Signal	Output	Low		
NRD	Read Signal	Output	Low		
NWE	Write Enable	Output	Low		
NBS0–NBS1	Byte Mask Signal	Output	Low		
NWAIT	External Wait Signal	Input	Low		
NAND Flash Controller - NFC					
NANDOE	NAND Flash Output Enable	Output	Low		
NANDWE	NAND Flash Write Enable	Output	Low		
NANDRDY	NAND Ready	Input			
NANDCLE	NAND Flash Command Line Enable	Output	Low		
NANDALE	NAND Flash Address Line Enable	Output	Low		
SDRAM Controller - SDRAMC					
SDCK	SDRAM Clock	Output			Tied low after reset
SDCKE	SDRAM Clock Enable	Output	High		
SDCS	SDRAM Controller Chip Select Line	Output	Low		
BA[1:0]	Bank Select	Output			
SDWE	SDRAM Write Enable	Output	Low		
RAS - CAS	Row and Column Signal	Output	Low		
NBS[1:0]	Byte Mask Signals	Output	Low		
SDA10	SDRAM Address 10 Line	Output			
High Speed Multimedia Card Interface - HSMCI					
MCCK	Multimedia Card Clock	I/O			
MCCDA	Multimedia Card Slot A Command	I/O			
MCDA0–MCDA7	Multimedia Card Slot A Data	I/O			
MCCDB	Multimedia Card Slot B Command	I/O			
MCDB0–MCDB3	Multimedia Card Slot A Data	I/O			
Universal Synchronous Asynchronous Receiver Transmitter - USARTx					
SCKx	USARTx Serial Clock	I/O			
TXDx	USARTx Transmit Data	I/O			
RXDx	USARTx Receive Data	Input			
RTSx	USARTx Request To Send	Output			
CTSx	USARTx Clear To Send	Input			

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Ethernet MAC 10/100 - EMAC					
EREFCK	Reference Clock	Input		RMII only	
ETXCK	Transmit Clock	Input		MII only	
ERXCK	Receive Clock	Input		MII only	
ETXEN	Transmit Enable	Output			
ETX0–ETX3	Transmit Data	Output		ETX0–ETX1 only in RMII	
ETXER	Transmit Coding Error	Output		MII only	
ERXDV	Receive Data Valid	Input		MII only	
ECRSDV	Carrier Sense and Data Valid	Input		RMII only	
ERX0–ERX3	Receive Data	Input		ERX0–ERX1 only in RMII	
ERXER	Receive Error	Input			
ECRS	Carrier Sense	Input		MII only	
ECOL	Collision Detected	Input		MII only	
EMDC	Management Data Clock	Output			
EMDIO	Management Data Input/Output	I/O			
CAN Controller - CANx					
CANRXx	CAN Input	Input			
CANTXx	CAN Output	Output			
Synchronous Serial Controller - SSC					
TD	SSC Transmit Data	Output			
RD	SSC Receive Data	Input			
TK	SSC Transmit Clock	I/O			
RK	SSC Receive Clock	I/O			
TF	SSC Transmit Frame Sync	I/O			
RF	SSC Receive Frame Sync	I/O			
Timer/Counter - TC					
TCLKx	TC Channel x External Clock Input	Input			
TIOAx	TC Channel x I/O Line A	I/O			
TIOBx	TC Channel x I/O Line B	I/O			
Pulse Width Modulation Controller - PWMC					
PWMHx	PWM Waveform Output High for channel x	Output			
PWMLx	PWM Waveform Output Low for channel x	Output			Only output in complementary mode when dead time insertion is enabled
PWMFIx	PWM Fault Input for channel x	Input			

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Serial Peripheral Interface - SPIx					
SPIx_MISO	Master In Slave Out	I/O			
SPIx_MOSI	Master Out Slave In	I/O			
SPIx_SPCK	SPI Serial Clock	I/O			
SPIx_NPCS0	SPI Peripheral Chip Select 0	I/O	Low		
SPIx_NPCS1–SPIx_NPCS3	SPI Peripheral Chip Select	Output	Low		
Two-Wire Interface - TWIx					
TWDx	TWIx Two-wire Serial Data	I/O			
TWCKx	TWIx Two-wire Serial Clock	I/O			
Analog-to-Digital Converter - ADC					
AD0–AD14	Analog Inputs	Analog			
ADTRG	ADC Trigger	Input			
ADVREF	ADC and DAC Reference	Analog			
Digital-to-Analog Converter Controller - DACC					
DAC0	DAC channel 0 analog output	Analog			
DAC1	DAC channel 1 analog output	Analog			
DATRG	DAC Trigger				
Fast Flash Programming Interface - FFPI					
PGMEN0–PGMEN2	Programming Enabling	Input		VDDIO	
PGMM0–PGMM3	Programming Mode	Input		VDDIO	
PGMD0–PGMD15	Programming Data	I/O		VDDIO	
PGMRDY	Programming Ready	Output	High	VDDIO	
PGMNVALID	Data Direction	Output	Low	VDDIO	
PGMNOE	Programming Read	Input	Low	VDDIO	
PGMCK	Programming Clock	Input		VDDIO	
PGMNCMD	Programming Command	Input	Low	VDDIO	
USB High Speed Device					
VBUS	USB Bus Power Measurement Mini Host/Device	Analog			
DFSDM	USB Full Speed Data -	Analog		VDDUTMI	
DFSDP	USB Full Speed Data +	Analog		VDDUTMI	
DHSDM	USB High Speed Data -	Analog		VDDUTMI	
DHSDP	USB High Speed Data +	Analog		VDDUTMI	
UOTGVBOF	USB VBus On/Off: Bus Power Control Port			VDDIO	
UOTGID	USB Identification: Mini Connector Identification Port			VDDIO	

Notes:
1. TDO pin is set in input mode when the Cortex-M3 Core is not in debug mode. Thus the internal pull-up corresponding to this PIO line must be enabled to avoid current consumption due to floating input.
2. PIOA: Schmitt Trigger on all, except PA0, PA9, PA26, PA29, PA30, PA31
3. PIOB: Schmitt Trigger on all, except PB14 and PB22

4. PIOC: Schmitt Trigger on all, except PC2 to PC9, PC15 to PC24
5. PIOD: Schmitt Trigger on all, except PD10 to PD30
6. PIOE: Schmitt Trigger on all, except PE0 to PE4, PE15, PE17, PE19, PE21, PE23, PE25, PE29
7. PIOF: Schmitt Trigger on all PIOs

3.1 Design Considerations

To facilitate schematic capture when using a SAM3X/A design, refer to the application note *Atmel AT03462: ATSAM3X and ATSAM3A Series - Checklist* (literature No. 42187) available on www.atmel.com.

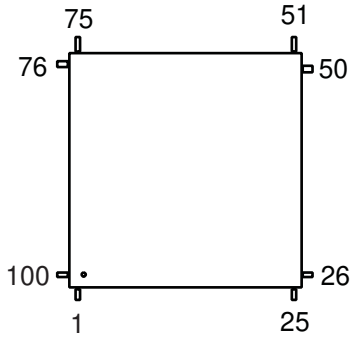
4. Package and Pinout

4.1 SAM3A4/8C and SAM3X4/8C Package and Pinout

The SAM3A4/8C and SAM3X4/8C are available in 100-lead LQFP and 100-ball TFBGA packages.

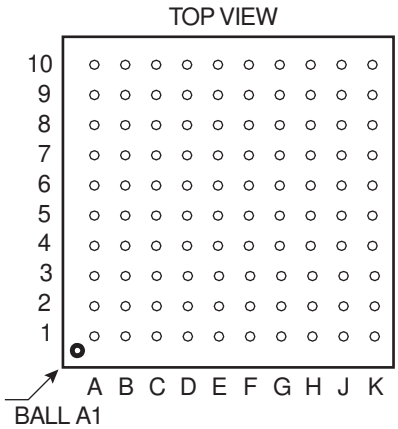
4.1.1 100-lead LQFP Package Outline

Figure 4-1. Orientation of the 100-lead LQFP Package



4.1.2 100-ball TFBGA Package Outline

Figure 4-2. Orientation of the 100-ball TFBGA Package



4.1.3 100-lead LQFP Pinout

Table 4-1. 100-lead LQFP SAM3A4/8C and SAM3X4/8C Pinout

1	PB26	26	DHSDP	51	VDDANA	76	PA26
2	PA9	27	DHSDM	52	GNDANA	77	PA27
3	PA10	28	VBUS	53	ADVREF	78	PA28
4	PA11	29	VBG	54	PB15	79	PA29
5	PA12	30	VDDUTMI	55	PB16	80	PB0
6	PA13	31	DFSDP	56	PA16	81	PB1
7	PA14	32	DFSDM	57	PA24	82	PB2
8	PA15	33	GNDUTMI	58	PA23	83	PB3
9	PA17	34	VDDCORE	59	PA22	84	PB4
10	VDDCORE	35	JTAGSEL	60	PA6	85	PB5
11	VDDIO	36	XIN32	61	PA4	86	PB6
12	GND	37	XOUT32	62	PA3	87	PB7
13	PA0	38	TST	63	PA2	88	PB8
14	PA1	39	VDDBU	64	PB12	89	VDDCORE
15	PA5	40	FWUP	65	PB13	90	VDDIO
16	PA7	41	GND	66	PB17	91	GND
17	PA8	42	VDDOUT	67	PB18	92	PB9
18	PB28	43	VDDIN	68	PB19	93	PB10
19	PB29	44	GND	69	PB20	94	PB11
20	PB30	45	VDDCORE	70	PB21	95	PC0
21	PB31	46	PB27	71	VDDCORE	96	PB14
22	GNDPLL	47	NRST	72	VDDIO	97	PB22
23	VDDPLL	48	PA18	73	GND	98	PB23
24	XOUT	49	PA19	74	PA21	99	PB24
25	XIN	50	PA20	75	PA25	100	PB25

4.1.4 100-ball TFBGA Pinout

Table 4-2. 100-ball TFBGA SAM3X4/8E Package and Pinout

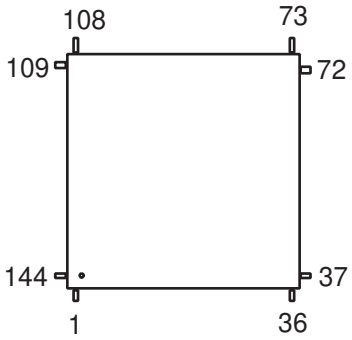
A1	PB26	C6	PB11	F1	VDDPLL	H6	NRST
A2	PB24	C7	PB8	F2	GNDPLL	H7	PA19
A3	PB22	C8	PB4	F3	PB30	H8	PA4
A4	PB14	C9	PB0	F4	PB29	H9	PA6
A5	PC0	C10	PA25	F5	GND	H10	PA22
A6	PB9	D1	PA5	F6	GND	J1	VBUS
A7	PB6	D2	PA0	F7	VDDIO	J2	DHSDP
A8	PB2	D3	PA1	F8	PB13	J3	DHSDM
A9	PA28	D4	VDDCORE	F9	PB17	J4	JTAGSEL
A10	PA26	D5	VDDIO	F10	PB18	J5	XIN32
B1	PA11	D6	VDDCORE	G1	XOUT	J6	VDDIN
B2	PB25	D7	VDDCORE	G2	VDDUTMI	J7	PA23
B3	PB23	D8	PB5	G3	PB31	J8	PA24
B4	PA10	D9	PB1	G4	GNDBU	J9	PB16
B5	PA9	D10	PA21	G5	PB27	J10	PA16
B6	PB10	E1	PB28	G6	PA18	K1	VBG
B7	PB7	E2	PA7	G7	PA20	K2	DFSDP
B8	PB3	E3	PA8	G8	PA3	K3	DFSDM
B9	PA29	E4	VDDCORE	G9	PA2	K4	VDDCORE
B10	PA27	E5	GND	G10	PB12	K5	XOUT32
C1	PA12	E6	GND	H1	XIN	K6	VDDOUT
C2	PA14	E7	VDDIO	H2	GNDUTMI	K7	VDDANA
C3	PA13	E8	PB19	H3	TST	K8	GNDANA
C4	PA17	E9	PB20	H4	VDDBU	K9	ADVREF
C5	PA15	E10	PB21	H5	FWUP	K10	PB15

4.2 SAM3X4/8E Package and Pinout

The SAM3X4/8E is available in 144-lead LQFP and 144-ball LFBGA packages.

4.2.1 144-lead LQFP Package Outline

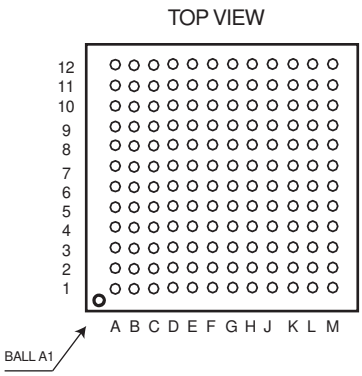
Figure 4-3. Orientation of the 144-lead LQFP Package



4.2.2 144-ball LFBGA Package Outline

The 144-ball LFBGA package has a 0.8 mm ball pitch and respects Green Standards. Its dimensions are 10 x 10 x 1.4 mm.

Figure 4-4. Orientation of the 144-ball LFBGA Package



4.2.3 144-lead LQFP Pinout

Table 4-3. 144-lead LQFP SAM3X4/8E Pinout

1	PB26	37	DHSDP	73	VDDANA	109	PA26
2	PA9	38	DHSDM	74	GNDANA	110	PA27
3	PA10	39	VBUS	75	ADVREF	111	PA28
4	PA11	40	VBG	76	PB15	112	PA29
5	PA12	41	VDDUTMI	77	PB16	113	PB0
6	PA13	42	DFSDP	78	PA16	114	PB1
7	PA14	43	DFSDM	79	PA24	115	PB2
8	PA15	44	GNDUTMI	80	PA23	116	PC4
9	PA17	45	VDDCORE	81	PA22	117	PC10
10	VDDCORE	46	JTAGSEL	82	PA6	118	PB3
11	VDDIO	47	NRSTB	83	PA4	119	PB4
12	GND	48	XIN32	84	PA3	120	PB5
13	PD0	49	XOUT32	85	PA2	121	PB6
14	PD1	50	SHDN	86	PB12	122	PB7
15	PD2	51	TST	87	PB13	123	PB8
16	PD3	52	VDDBU	88	PB17	124	VDDCORE
17	PD4	53	FWUP	89	PB18	125	VDDIO
18	PD5	54	GNDBU	90	PB19	126	GND
19	PD6	55	PC1	91	PB20	127	PB9
20	PD7	56	VDDOUT	92	PB21	128	PB10
21	PD8	57	VDDIN	93	PC11	129	PB11
22	PD9	58	GND	94	PC12	130	PC0
23	PA0	59	PC2	95	PC13	131	PC20
24	PA1	60	PC3	96	PC14	132	PC21
25	PA5	61	VDDCORE	97	PC15	133	PC22
26	PA7	62	VDDIO	98	PC16	134	PC23
27	PA8	63	PC5	99	PC17	135	PC24
28	PB28	64	PC6	100	PC18	136	PC25
29	PB29	65	PC7	101	PC19	137	PC26
30	PB30	66	PC8	102	PC29	138	PC27
31	PB31	67	PC9	103	PC30	139	PC28
32	PD10	68	PB27	104	VDDCORE	140	PB14
33	GNDPLL	69	NRST	105	VDDIO	141	PB22
34	VDDPLL	70	PA18	106	GND	142	PB23
35	XOUT	71	PA19	107	PA21	143	PB24
36	XIN	72	PA20	108	PA25	144	PB25

4.2.4 144-ball LFBGA Pinout

Table 4-4. 144-ball LFBGA SAM3X4/8E Pinout

A1	PA9	D1	PA17	G1	PA5	K1	VDDCORE
A2	PB23	D2	PD0	G2	PA7	K2	GNDUTMI
A3	PB14	D3	PA11	G3	PA8	K3	VDDPLL
A4	PC26	D4	PA15	G4	PA1	K4	NRSTB
A5	PC24	D5	PA14	G5	GND	K5	SHDN
A6	PC20	D6	PC27	G6	GND	K6	PC3
A7	PB10	D7	PC25	G7	GND	K7	PC6
A8	PB6	D8	VDDIO	G8	PC16	K8	PC7
A9	PB4	D9	PB5	G9	PC15	K9	PA18
A10	PC4	D10	PB0	G10	PC13	K10	PA23
A11	PA28	D11	PC30	G11	PB13	K11	PA16
A12	PA27	D12	PC19	G12	PB18	K12	PA24
B1	PA10	E1	PD1	H1	XOUT	L1	DHSDP
B2	PB26	E2	PD2	H2	PB30	L2	DHSDM
B3	PB24	E3	PD3	H3	PB28	L3	VDDUTMI
B4	PC28	E4	PD4	H4	PB29	L4	JTAGSEL
B5	PC23	E5	PD5	H5	VDDBU	L5	GNDBU
B6	PC0	E6	VDDCORE	H6	VDDCORE	L6	PC1
B7	PB9	E7	VDDCORE	H7	VDDIO	L7	PC2
B8	PB8	E8	VDDCORE	H8	PC12	L8	PC5
B9	PB3	E9	PB1	H9	PC11	L9	PC9
B10	PB2	E10	PC18	H10	PA3	L10	PA20
B11	PA26	E11	PB19	H11	PB12	L11	VDDANA
B12	PA25	E12	PB21	H12	PA2	L12	PB16
C1	PA13	F1	PD8	J1	XIN	M1	DFSDP
C2	PA12	F2	PD6	J2	GNDPLL	M2	DFSDM
C3	PB25	F3	PD9	J3	PD10	M3	VBG
C4	PB22	F4	PA0	J4	PB31	M4	VBUS
C5	PC22	F5	PD7	J5	TST	M5	XIN32
C6	PC21	F6	GND	J6	FWUP	M6	XOUT32
C7	PB11	F7	GND	J7	PB27	M7	VDDOUT
C8	PB7	F8	VDDIO	J8	NRST	M8	VDDIN
C9	PC10	F9	PC17	J9	PA19	M9	PC8
C10	PA29	F10	PC14	J10	PA22	M10	GNDANA
C11	PA21	F11	PB20	J11	PA4	M11	ADVREF
C12	PC29	F12	PB17	J12	PA6	M12	PB15

5. Power Considerations

5.1 Power Supplies

The SAM3X/A series product has several types of power supply pins:

- VDDCORE pins: Power the core, the embedded memories and the peripherals; voltage ranges from 1.62V to 1.95V.
- VDDIO pins: Power the peripherals I/O lines; voltage ranges from 1.62V to 3.6V.
- VDDIN pin: Powers the voltage regulator
- VDDOUT pin: Output of the voltage regulator
- VDDBU pin: Powers the Slow Clock oscillator and a part of the System Controller; voltage ranges from 1.62V to 3.6V. VDDBU must be supplied before or at the same time as VDDIO and VDDCORE.
- VDDPLL pin: Powers the PLL A, UPLL and 3–20 MHz Oscillator; voltage ranges from 1.62V to 1.95V.
- VDDUTMI pin: Powers the UTMI+ interface; voltage ranges from 3.0V to 3.6V, 3.3V nominal.
- VDDANA pin: Powers the ADC and DAC cells; voltage ranges from 2.0V to 3.6V.

Ground pins GND are common to VDDCORE and VDDIO pins power supplies.

Separated ground pins are provided for VDDBU, VDDPLL, VDDUTMI and VDDANA. These ground pins are respectively GNDBU, GNDPLL, GNDUTMI and GNDANA.

5.2 Power-up Considerations

5.2.1 VDDIO Versus VDDCORE

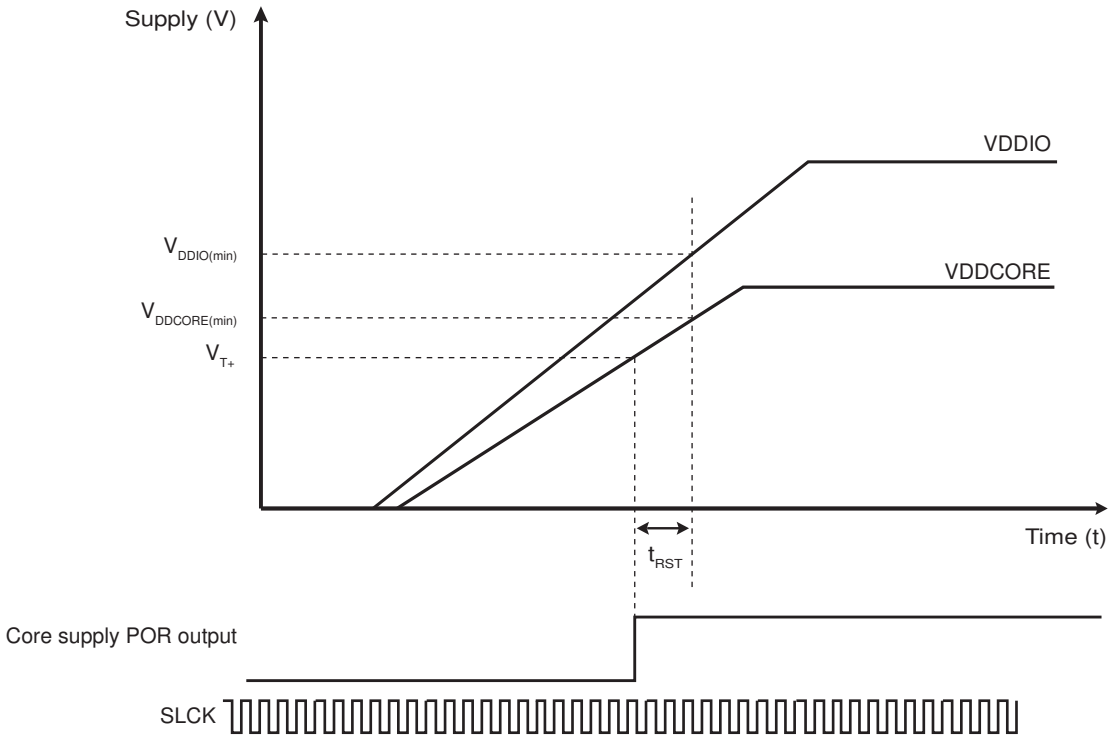
V_{DDIO} must always be higher than or equal to V_{DDCORE}.

V_{DDIO} must reach its minimum operating voltage (1.60 V) before V_{DDCORE} has reached $V_{DDCORE(min)}$. The minimum slope for V_{DDCORE} is defined by ($V_{DDCORE(min)}$ - V_{T+}) / t_{RST}.

If V_{DDCORE} rises at the same time as V_{DDIO}, the V_{DDIO} rising slope must be higher than or equal to 5 V/ms.

If VDDCORE is powered by the internal regulator, all power-up considerations are met.

Figure 5-1. VDDCORE and VDDIO Constraints at Startup



5.2.2 VDDIO Versus VDDIN

At power-up, V_{DDIO} needs to reach 0.6 V before V_{DDIN} reaches 1.0 V.

VDDIO voltage needs to be equal to or below (VDDIN voltage + 0.5 V).

5.3 Voltage Regulator

The SAM3X/A series embeds a voltage regulator that is managed by the Supply Controller.

This internal regulator is intended to supply the internal core of SAM3X/A series but can be used to supply other parts in the application. It features two different operating modes:

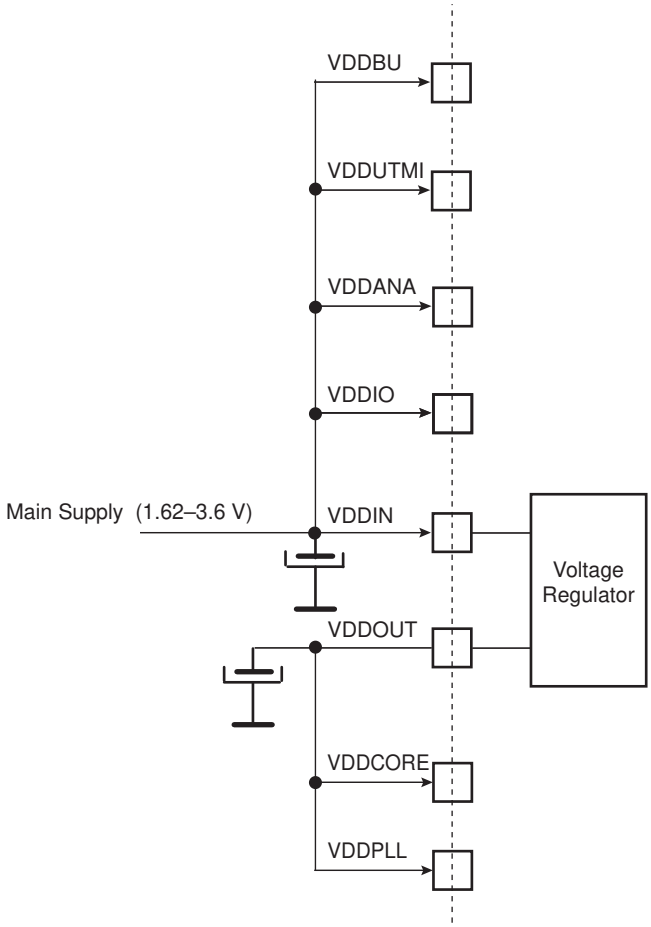
- In Normal mode, the voltage regulator consumes less than 700 µA static current and draws 150 mA of output current. Internal adaptive biasing adjusts the regulator quiescent current depending on the required load current. In Wait Mode or when the output current is low, quiescent current is only 7 µA.
- In Shutdown mode, the voltage regulator consumes less than 1 µA while its output is driven internally to GND. The default output voltage is 1.80V and the startup time to reach Normal mode is inferior to 400 µs.

For adequate input and output power supply decoupling/bypassing, refer to Table 45-3 ”1.8V Voltage Regulator Characteristics”.

5.4 Typical Powering Schematics

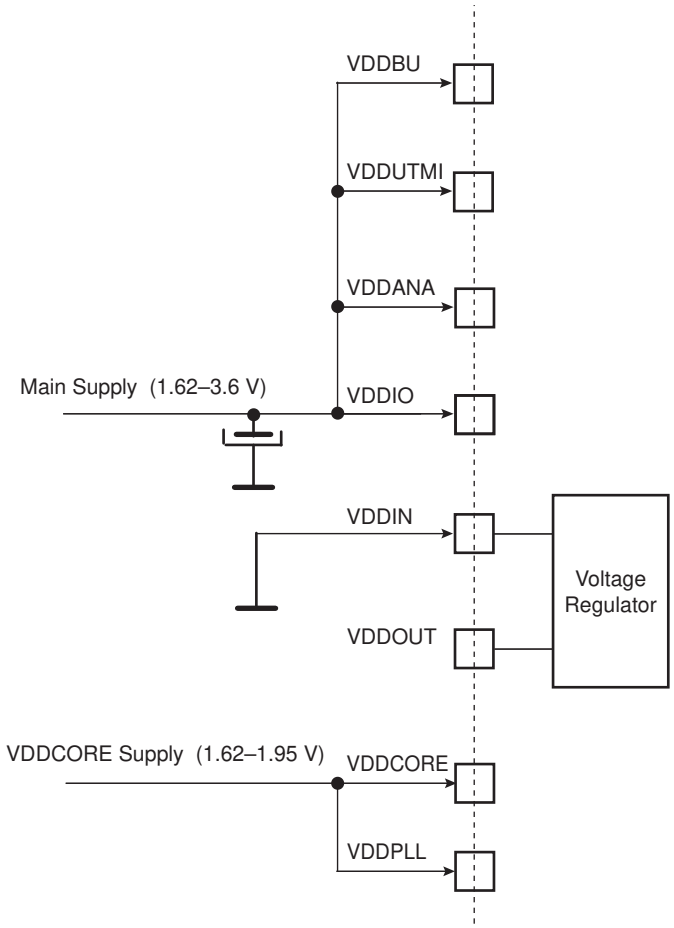
The SAM3X/A series supports a 1.62–3.6 V single supply mode. The internal regulator input connected to the source and its output feeds VDDCORE. Figure 5-2 shows the power schematics.

Figure 5-2. Single Supply



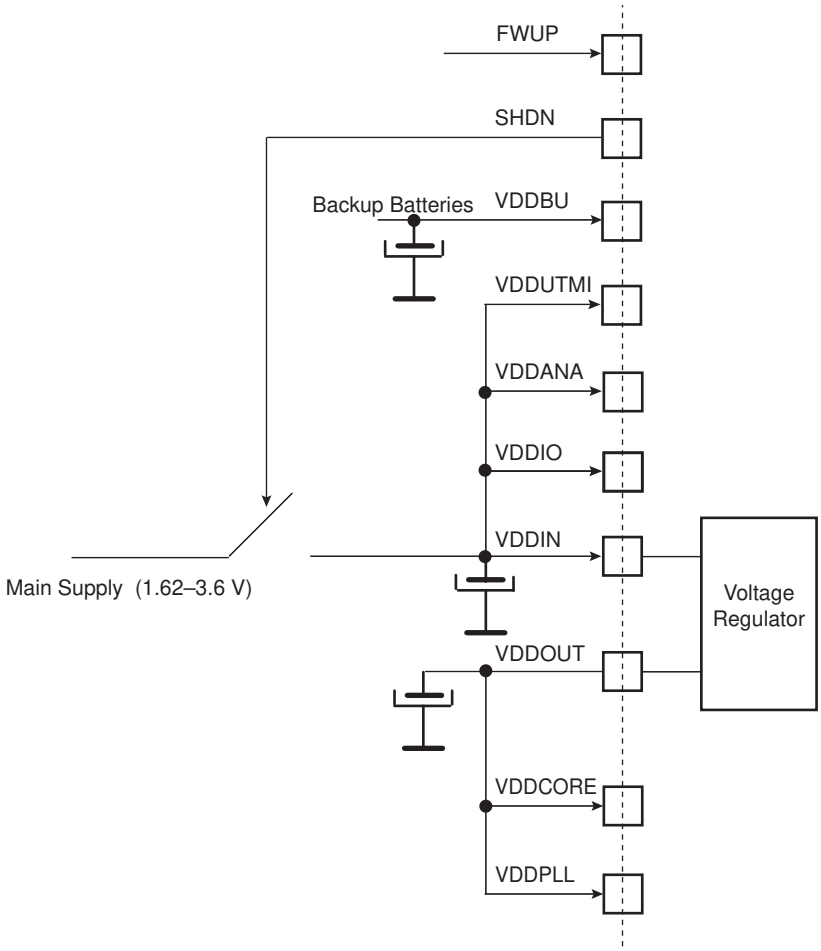
Note: Restrictions
For USB, VDDUTMI needs to be greater than 3.0V.
For ADC, VDDANA needs to be greater than 2.0V.
For DAC, VDDANA needs to be greater than 2.4V.

Figure 5-3. Core Externally Supplied



Note: Restrictions
For USB, VDDUTMI needs to be greater than 3.0V.
For ADC, VDDANA needs to be greater than 2.0V.
For DAC, VDDANA needs to be greater than 2.4V.

Figure 5-4. Backup Batteries Used



Note: 1. Restrictions
For USB, VDDUTMI needs to be greater than 3.0V.
For ADC, VDDANA needs to be greater than 2.0V.
For DAC, VDDANA needs to be greater than 2.4V.
2. VDDUTMI and VDDANA cannot be left unpowered.

5.5 Active Mode

Active mode is the normal running mode with the core clock running from the fast RC oscillator, the main crystal oscillator or the PLLA. The power management controller can be used to adapt the frequency and to disable the peripheral clocks.

5.6 Low Power Modes

The SAM3X/A devices provide the following low-power modes: Backup, Wait, and Sleep.

5.6.1 Backup Mode

The purpose of backup mode is to achieve the lowest power consumption possible in a system which is performing periodic wake-ups to perform tasks but not requiring fast startup time (< 0.5 ms).

The Supply Controller, zero-power power-on reset, RTT, RTC, backup registers and 32 kHz oscillator (RC or crystal oscillator selected by software in the Supply Controller) are running. The regulator and the core supply are off.

Backup mode is based on the Cortex-M3 deep-sleep mode with the voltage regulator disabled.

The SAM3X/A series can be awakened from this mode through the Force Wake-up pin (FWUP), and Wake-up input pins WKUP0–15, Supply Monitor, RTT or RTC wake-up event. Current consumption is 2.5 µA typical on VDDBU.

Backup mode can be entered by using the WFE instruction.

The procedure to enter Backup mode using the WFE instruction is the following:

1. Write a 1 to the SLEEPDEEP bit in the Cortex-M3 processor System Control Register (SCR) (refer to Section 10.21.7 “System Control Register”).
2. Execute the WFE instruction of the processor.

Exit from Backup mode happens if one of the following enable wake-up events occurs:

- Low level, configurable debouncing on FWUP pin
- Level transition, configurable debouncing on pins WKUPEN0–15
- SM alarm
- RTC alarm
- RTT alarm

5.6.2 Wait Mode

The purpose of the wait mode is to achieve very low power consumption while maintaining the whole device in a powered state for a startup time of less than 10 µs.

In this mode, the clocks of the core, peripherals and memories are stopped. However, the core, peripherals and memories power supplies are still powered. From this mode, a fast start up is available.

This mode is entered via Wait for Event (WFE) instructions with LPM = 1 (Low Power Mode bit in PMC_FSMR). The Cortex-M3 is able to handle external events or internal events in order to wake-up the core (WFE). This is done by configuring the external lines WKUP0–15 as fast startup wake-up pins (refer to Section 5.8 “Fast Startup”). RTC or RTT Alarm and USB wake-up events can be used to wake up the CPU (exit from WFE).

Current consumption in Wait mode is typically 23 µA for total current consumption if the internal voltage regulator is used or 15 µA if an external regulator is used.

The procedure to enter Wait mode is the following:

1. Select the 4/8/12 MHz Fast RC Oscillator as Main Clock.
2. Set the LPM bit in the PMC Fast Startup Mode Register (PMC_FSMR).
3. Execute the WFE instruction of the processor.