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Description

The Atmel® | SMART SAM4C microcontrollers are system-on-chip solutions for smart energy applications, built around two high-performance 32-bit ARM® Cortex®-M4 RISC processors.

These devices operate at a maximum speed of 120 MHz and feature up to 2 Mbytes of embedded Flash, up to 304 Kbytes of SRAM and on-chip cache for each core.

The dual ARM Cortex-M4 architecture allows for integration of an application layer, communications layers and security functions in a single device, with the ability to extend program and data memory via a 16-bit external bus interface.

The peripheral set includes advanced cryptographic engine, anti-tamper, floating point unit (FPU), USB Full-speed Host/Device port, five USARTs, two UARTs, two TWIs, up to seven SPIs, as well as a PWM timer, two 3-channel general-purpose 16-bit timers, calibrated low-power RTC running on the backup domain down to 0.5 µA, and a 50 × 6 segmented LCD controller.

The SAM4C series is a scalable platform providing, alongside Atmel's industry leading SAM4 standard microcontrollers, unprecedented cost structure, performance and flexibility to smart meter designers worldwide.

Features

- Application/Master Core
    – ARM Cortex-M4 running at up to 120 MHz[1]
    – Memory Protection Unit (MPU)
    – DSP Instruction
    – Thumb®-2 instruction set
    – Instruction and Data Cache Controller with 2 Kbytes Cache Memory
    – Memories
        - Up to 2 Mbytes of Embedded Flash for Program Code (I-Code bus) and Program Data (D-Code bus) with Built-in ECC (2-bit error detection and 1-bit correction per 128 bits)
        - Up to 256 Kbytes of Embedded SRAM (SRAM0) for Program Data (System bus)
        - 8 Kbytes of ROM with embedded bootloader routines (UART) and In-Application Programming (IAP) routines
- Coprocessor (provides ability to separate application, communication or metrology functions)
    – ARM Cortex-M4F running at up to 120 MHz[1]
    – IEEE® 754 Compliant, Single-precision Floating-Point Unit (FPU)
    – DSP Instruction
    – Thumb-2 instruction set
    – Instruction and Data Cache Controller with 2 Kbytes of Cache Memory
    – Memories
        - Up to 32 Kbytes of Embedded SRAM (SRAM1) for Program Code (I-Code bus) and Program Data (D-Code bus and System bus)
        - Up to 16 Kbytes of Embedded SRAM (SRAM2) for Program Data (System bus)
- Symmetrical/Asynchronous Dual Core Architecture
    – Interrupt-based Interprocessor Communication
    – Asynchronous Clocking
    – One Interrupt Controller (NVIC) for each core
    – Each Peripheral IRQ routed to each NVIC Input
- Cryptography
    – High-performance AES 128 to 256 with various modes (GCM, CBC, ECB, CFB, CBC-MAC, CTR)
    – TRNG (up to 38 Mbit/s stream, with tested Diehard and FIPS)
    – Public Key Crypto accelerator and associated ROM library for RSA, ECC, DSA, ECDSA
    – Integrity Check Module (ICM) based on Secure Hash Algorithm (SHA1, SHA224, SHA256), DMA-assisted
- Safety
    – Up to four physical Anti-tamper Detection I/Os with Time Stamping and Immediate Clear of General Backup Registers
    – Security Bit for Device Protection from JTAG Accesses
- Shared System Controller
    – Power Supply
        - Embedded core and LCD voltage regulator for single-supply operation
        - Power-on-Reset (POR), Brownout Detector (BOD) and Dual Watchdog for safe operation
        - Ultra-low-power Backup mode (< 0.5 µA Typical @ 25°C)

Atmel

- – Clock
  - 3 to 20 MHz oscillator supporting crystal, ceramic resonator or external clock signal. Also supports clock failure detection
  - Ultra-low power 32.768 kHz oscillator supporting crystal or external clock signal and frequency monitoring
  - High-precision 4/8/12 MHz factory-trimmed internal RC oscillator with on-the-fly trimming capability
  - One high-frequency PLL up to 240 MHz, one 8 MHz PLL with internal 32 kHz input, as source for high-frequency PLL
  - Low-power slow clock internal RC oscillator as permanent clock
  - – Ultra-low-power RTC with Gregorian and Persian Calendar, Waveform Generation in Backup mode and Clock Calibration Circuitry for 32.768 kHz Crystal Frequency Compensation Circuitry
  - – Up to 23 Peripheral DMA (PDC) Channels
- Shared Peripherals
  - – One Low-power Segmented LCD Controller
    - Display capacity of 50 segments and 6 common terminals
    - Software-selectable LCD output voltage (Contrast)
    - Low current consumption in Low-power mode
    - Can be used in Backup mode
  - – Up to five USARTs with ISO7816, IrDA®, RS-485, SPI and Manchester Mode
  - – Two 2-wire UARTs with one UART (UART1) supporting optical transceiver providing an electrically isolated serial communication with hand-held equipment, such as calibrators, compliant with ANSI-C12.18 or IEC62056-21 norms
  - – Full-speed USB Host and Device Port (available only for SAM4C32E in a 144-pin package)
  - – Up to two 400 kHz Master/Slave and Multi-Master Two-wire Interfaces (I^{2}C compatible)
  - – Up to seven Serial Peripheral Interfaces (SPI)
  - – Two 3-channel 16-bit Timer/Counters with Capture, Waveform, Compare and PWM modes
  - – Quadrature Decoder Logic and 2-bit Gray Up/Down Counter for Stepper Motor
  - – 4-channel 16-bit Pulse Width Modulator
  - – 32-bit Real-time Timer
- Analog Conversion Block
  - – 8-channel, 500 kS/s, Low-power 10-bit SAR ADC with Digital Averager providing 12-bit Resolution at 30 kS/s
  - – Software-controlled On-chip Reference ranging from 1.6V to 3.4V
  - – Temperature Sensor and Backup Battery Voltage Measurement Channel
- Debug
  - – Star Topology AHB-AP Debug Access Port Implementation with Common SW-DP / SWJ-DP Providing Higher Performance than Daisy-chain Topology
  - – Debug Synchronization between both Cores (cross triggering to/from each core for Halt and Run Mode)
- I/O
  - – Up to 106 I/O lines with External Interrupt Capability (edge or level sensitivity), Schmitt Trigger, Internal Pull-up/pull-down, Debouncing, Glitch Filtering and On-die Series Resistor Termination
- Package
  - – 100-lead LQFP, 14 x 14 mm, pitch 0.5 mm
  - – 144-lead LQFP, 20 x 20 mm, pitch 0.5 mm (SAM4C32E only)

Note: 1.   120 MHz: -40°C/+85°C, VDDCORE = 1.2V

1. Configuration Summary

The SAM4C devices differ in memory size, package and features. Table 1-1 summarizes the different device configurations.

Table 1-1. Configuration Summary

Feature	SAM4C32E	SAM4C32C	SAM4C16C	SAM4C8C	SAM4C4C
Flash	2048 Kbytes	2048 Kbytes	1024 Kbytes	512 Kbytes	256 Kbytes
SRAM	256 + 32 + 16 Kbytes		128 + 16 + 8 Kbytes		
Package	LQFP 144	LQFP 100			
Number of PIOs	106	74			
External Bus Interface	16-bit data				
16-bit Timer	6 channels				
16-bit PWM	4 channels				
UART/USART	2/5				
SPI [1]	2/5 + 5				
TWI	2				
10-bit ADC Channels[2]	8				
USB Full Speed	Host + Device	–			
Cryptography	AES, CPKCC, ICM (SHA), TRNG				
Segmented LCD	50 segments × 6 commons				
Anti-Tampering Inputs	4				
Flash Page Size	512 bytes				
Flash Pages	2 × 2048		2048	1024	512
Flash Lock Region Size	8 Kbytes				
Flash Lock Bits	256 (128 + 128)		128	64	32

Notes: 1. 2/5 + 5 = Number of SPI Controllers / Number of Chip Selects + Number of USARTs with SPI mode.
2. One channel is reserved for internal temperature sensor and one channel for VDDBU measurement.

2. Block Diagram

Figure 2-1. SAM4C Series Block Diagram
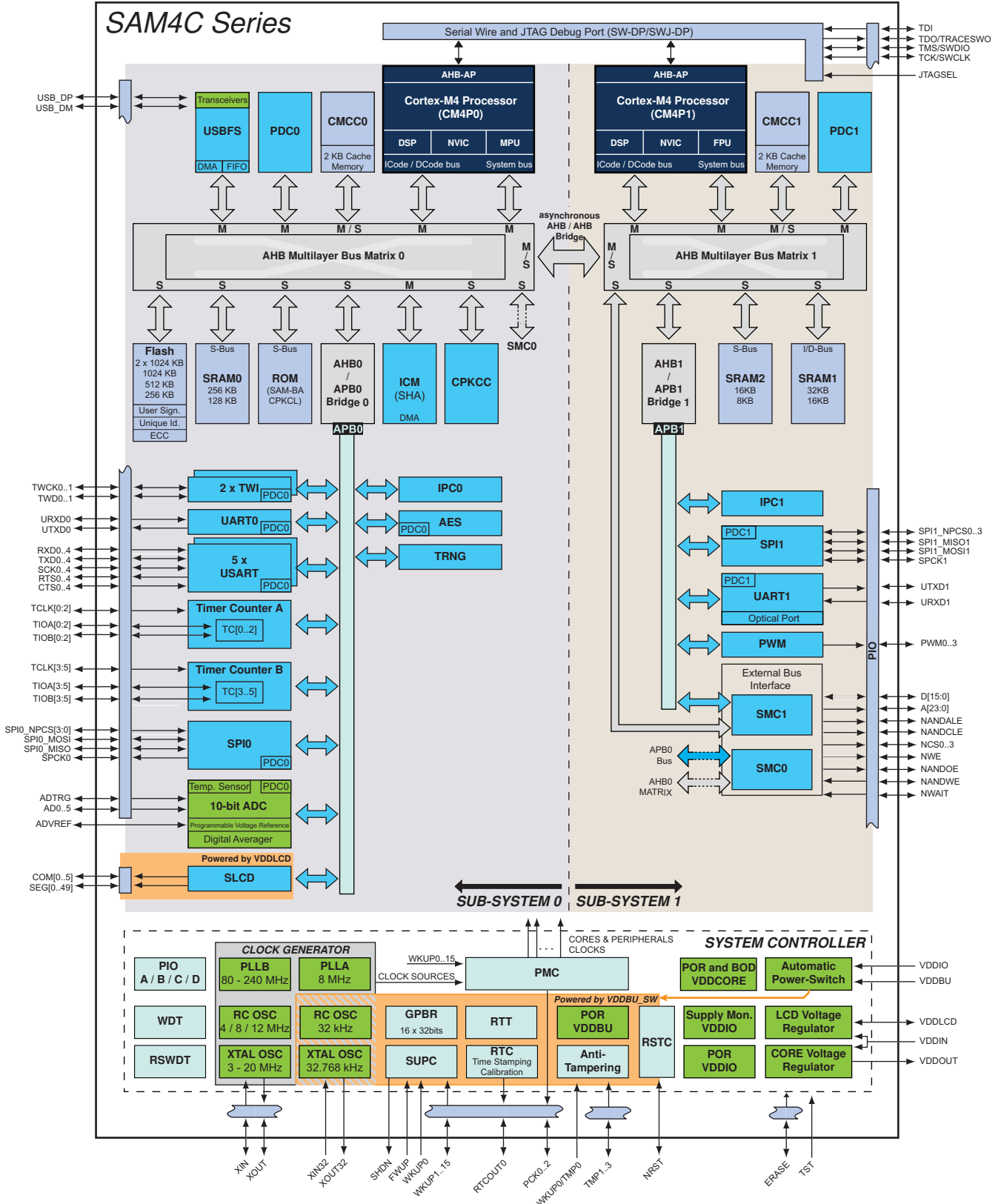
3. Signal Description

Table 3-1 provides details on signal names classified by peripheral.

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Power Supplies					
VDDIO	See Table 5-1	Power	–	–	–
VDDBU			–	–	–
VDDIN			–	–	–
VDDLCD			–	–	–
VDDOUT			–	–	–
VDDPLL			–	–	–
VDDCORE			–	–	–
GND		Ground	–	–	–
Clocks, Oscillators and PLLs					
XIN	Main Crystal Oscillator Input	Analog Digital	–	VDDIO	XIN is a clock input when the 3 to 20 MHz oscillator is in Bypass mode.
XOUT	Main Crystal Oscillator Output		–		
XIN32	Slow Clock Crystal Oscillator Input	Analog Digital	–	VDDBU	XIN32 is a clock input when the 32.768 kHz oscillator is in Bypass mode.
XOUT32	Slow Clock Crystal Oscillator Output		–		
PCK0–PCK2	Programmable Clock Output	Output	–	VDDIO	–
Real-Time Clock					
RTCOUT0	Programmable RTC Waveform Output	Digital Output	–	VDDIO	–
Supply Controller					
FWUP	Force Wake-up Input	Digital Input	Low	VDDBU	External Pull-up needed
TMP0	Anti-tampering Input 0	Digital Input	–	VDDBU	External Pull-up or Pull-down resistor needed
TMP1–TMP3	Anti-tampering Input 1 to 3	Digital Input	–	VDDIO	–
SHDN	Active Low Shutdown Control	Digital Output	–	VDDBU	0: The device is in Backup mode. 1: The device is running (not in Backup mode).
WKUP0	Wake-up Input 0	Digital Input	–	VDDBU	–
WKUP1–15	Wake-up Input 1 to 15	Digital Input	–	VDDIO	–

Table 3-1.   Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
**Serial Wire/JTAG Debug Port - SWJ-DP**				
TCK/SWCLK	Test Clock/Serial Wire Clock	Digital Input	–	VDDIO	–
TDI	Test Data In		–		
TDO/TRACESWO	Test Data Out / Trace Asynchronous Data Out	Digital Output	–	VDDIO	–
TMS/SWDIO	Test Mode Select input / Serial Wire Input/Output	Digital I/O	–		
JTAGSEL	JTAG Selection	Digital Input	High	VDDBU	Permanent Internal pull-down
**Flash Memory**				
ERASE	Flash and NVM Configuration Bits Erase Command	Digital Input	High	VDDIO	Permanent Internal pull-down
**Reset/Test**				
NRST	Synchronous Microcontroller Reset	Digital I/O	Low	VDDIO	Permanent Internal pull-up
TST	Test Select	Digital Input	–	VDDBU	Permanent Internal pull-down
**Universal Asynchronous Receiver Transceiver - UARTx**				
URXDx	UART Receive Data	Digital/ Analog Input	–	VDDIO	Analog mode for optical receiver
UTXDx	UART Transmit Data	Digital Output	–		–
**PIO Controller - PIOA - PIOB - PIOC**				
PA0–PA31	Parallel IO Controller A	Digital I/O	–	VDDIO	–
PB0–PB31	Parallel IO Controller B		–		–
PC0–PC9	Parallel IO Controller C		–		–
PD0–PD31	Parallel IO Controller D		–		
**External Bus Interface - EBI**				
D[15:0]	Data Bus	Digital I/O	–	VDDIO	–
A[23:0]	Address Bus	Digital Output	–		–
NWAIT	External Wait signal	Digital Input	Low		–

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
**Static Memory Controller - SMC**				
NCS0–NCS3	Chip Select Lines	Digital Output	Low	VDDIO	–
NRD	Read Signal				–
NWE	Write Enable				–
NBS0–NBS1	Byte Mask Signal				–
NWR0–NWR1	Write Signal				–
**NAND Flash Logic**				
NANDOE	NAND Flash Output Enable	Digital Output	Low	VDDIO	–
NANDWE	NAND Flash Write Enable				–
NANDCS	NAND Chip Select				SMC chip select used for Nand Flash Logic
**Universal Synchronous Asynchronous Receiver Transmitter - USARTx**				
SCKx	USARTx Serial Clock	Digital I/O	–	VDDIO	–
TXDx	USARTx Transmit Data	Digital Output	–		–
RXDx	USARTx Receive Data	Digital Input	–		–
RTSx	USARTx Request To Send	Digital Output	–		–
CTSx	USARTx Clear To Send	Digital Input	–		–
**Timer/Counter - TC**				
TCLKx	TC Channel x External Clock Input	Digital Input	–	VDDIO	–
TIOAx	TC Channel x I/O Line A	Digital I/O	–		–
TIOBx	TC Channel x I/O Line B		–		–
**Pulse Width Modulation Controller - PWMC**				
PWMx	PWM Waveform Output for channel x	Digital Output	–	VDDIO	–
**USB Host and Device Port - USB**				
USB_DP	USB Full-speed Data +	Analog Digital	–	VDDIO	Reset State: - USB Device mode - Internal Pull-down
USB_DM	USB Full-speed Data -				

Table 3-1.   Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Serial Peripheral Interface - SPI					
SPIx_MISOx	Master In Slave Out	Digital Input	–	VDDIO	–
SPIx_MOSIx	Master Out Slave In	Digital Output	–		–
SPCKx	SPI Serial Clock		–		–
SPIx_NPCS0	SPI Peripheral Chip Select 0		Low		NPCS0 is also NSS for Slave mode
SPIx_NPCS1–SPIx_NPCS3	SPI Peripheral Chip Select	Output	Low		–
Segmented LCD Controller - SLCDC					
COM0–COM5	Common Terminals	Output	–	VDDIO	–
SEG0–SEG49	Segment Terminals		–		–
Two-wire Interface - TWI					
TWDx	TWIx Two-wire Serial Data	Digital I/O	–	VDDIO	–
TWCKx	TWIx Two-wire Serial Clock	Digital Output	–		–
Analog					
ADVREF	External Voltage Reference for ADC	Analog Input	–	VDDIN	–
10-bit Analog-to-Digital Converter - ADC					
AD0–AD5	Analog Inputs	Analog, Digital	–	VDDIO	ADC input range limited to [0..ADVREF]
ADTRG	ADC Trigger	Input	–		–
Fast Flash Programming Interface - FFPI					
PGMEN0–PGMEN1	Programming Enabling	Digital Input	–	VDDIO	–
PGMM0–PGMM3	Programming Mode		–		–
PGMD0–PGMD15	Programming Data	Digital I/O	–		–
PGMRDY	Programming Ready	Digital Output	High		–
PGMNVALID	Data Direction		Low		–
PGMNOE	Programming Read	Digital Input	Low		–
PGMNCMD	Programming Command				–

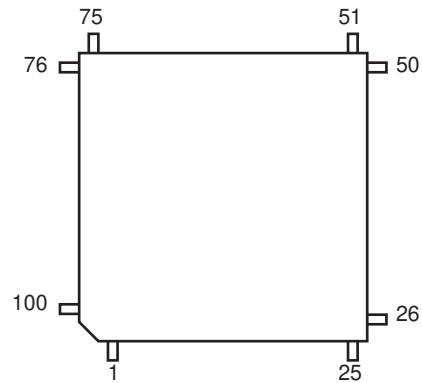# 4. Package and Pinout

4.1 100-lead LQFP Package and Pinout

4.1.1 100-lead LQFP Package Outline

The 100-lead LQFP package has a 0.5 mm ball pitch and respects Green standards.

Figure 4-1 shows the orientation of the 100-lead LQFP package. Refer to Figure 47-1 "100-lead LQFP Package Drawing".

Figure 4-1.   Orientation of the 100-lead LQFP Package

4.1.2 100-lead LQFP Pinout

Table 4-1. SAM4C32C/16C/8C/4C 100-lead LQFP Pinout

|							
1	PB6	26	TDI/PB0	51	PA31	76	VDDIO
2	PB7	27	TCK/SWCLK/PB3	52	GND	77	ADVREF
3	PB18	28	TMS/SWDIO/PB2	53	VDDPLL	78	GND
4	GND	29	ERASE/PC9	54	PC8	79	PB31/AD5
5	PB19	30	TDO/TRACESWO/PB1/RTCOUT0	55	PC5	80	PB23/AD4
6	PB8	31	PC1	56	PC4	81	PB13/AD3
7	PB22	32	PC6	57	PC3	82	PA5/AD2/PGMRDY
8	PB30	33	VDDIO	58	PC2	83	PA4/AD1/PGMNCMD
9	PB25	34	VDDBU	59	PA29	84	PA12/AD0/PGMD0
10	PB24	35	FWUP	60	PA28	85	VDDIN
11	VDDCORE	36	JTAGSEL	61	PA27/PGMD15	86	VDDOUT
12	PB29	37	SHDN	62	PA6/PGMNOE	87	PB21
13	PB9	38	TST	63	VDDCORE	88	PB20
14	PB10	39	WKUP0/TMP0	64	PA3	89	VDDCORE
15	PB11	40	XIN32	65	PA21/PGMD9	90	PA0/PGMEN0
16	PB12	41	XOUT32	66	PA22/PGMD10	91	PB27/TMP2
17	PB14	42	GND	67	PA23/PGMD11	92	VDDLCD
18	PB15	43	PB4	68	PA9/PGMM1	93	PB26
19	PA26/PGMD14	44	VDDCORE	69	PA10/PGMM2	94	PB28/TMP3
20	PA25/PGMD13	45	PB5	70	PA11/PGMM3	95	PB16/TMP1
21	PA24/PGMD12	46	PC7	71	PA13/PGMD1	96	PA1/PGMEN1
22	PA20/PGMD8	47	PC0	72	PA14/PGMD2	97	PB17
23	PA19/PGMD7	48	NRST	73	PA15/PGMD3	98	PA7/PGMNVALID
24	PA18/PGMD6	49	VDDIO	74	PA16/PGMD4	99	VDDIO
25	PA8/PGMM0	50	PA30	75	PA17/PGMD5	100	PA2

4.2   144-lead LQFP Package and Pinout

4.2.1   144-lead LQFP Package Outline

The 144-lead LQFP package has a 0.5 mm ball pitch and respects Green Standards.

Figure 4-2 shows the orientation of the 144-lead LQFP package. Refer to Figure 47-2 "144-lead LQFP Package Mechanical Drawing".

Figure 4-2.   Orientation of the 144-lead LQFP Package
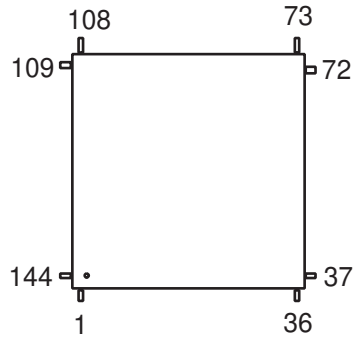
4.2.2 144-lead LQFP Pinout

Table 4-2. SAM4C32E 144-lead LQFP Pinout

1	PB6	37	PB0	73	PA31	109	VDDIO
2	PB7	38	PB3	74	GND	110	ADVREF
3	PB18	39	PB2	75	VDDPLL	111	GND
4	GND	40	PC9	76	PC8	112	PB31
5	PB19	41	PB1	77	PC5	113	PB23
6	PB8	42	PC1	78	PC4	114	PB13
7	PD23	43	NC	79	PC3	115	PA5/AD2/PGMRDY
8	PD24	44	NC	80	PC2	116	PA4/AD1/PGMNCMD
9	PD25	45	NC	81	PA29	117	PA12/AD0/PGMD0
10	VDDIO	46	PC6	82	PA28	118	VDDIN
11	PD26	47	VDDIO	83	PA27/PGMD15	119	VDDOUT
12	PD27	48	PD2	84	PA6/PGMNOE	120	PB21
13	PD28	49	PD3	85	VDDCORE	121	PB20
14	GND	50	GND	86	PA3	122	GND
15	PD29	51	PD0	87	PA21/PGMD9	123	VDDCORE
16	PD30	52	PD1	88	PA22/PGMD10	124	PD13
17	PD31	53	VDDIO	89	PD4	125	PD14
18	PB22	54	VDDBU	90	PD5	126	PA0/PGMEN0
19	PB30	55	FWUP	91	PD6	127	PD15
20	PB25	56	JTAGSEL	92	VDDIO	128	PD16
21	PB24	57	SHDN	93	PD7	129	PB27/TMP2
22	VDDCORE	58	TST	94	PD8	130	PD17
23	PB29	59	WKP0/TMP0	95	GND	131	PD18
24	PB9	60	XIN32	96	PD9	132	PD19
25	PB10	61	XOUT32	97	PD10	133	PD20
26	PB11	62	NC	98	PD11	134	VDDLCD
27	PB12	63	NC	99	PD12	135	PD21
28	PB14	64	GND	100	PA23/PGMD11	136	PD22
29	PB15	65	PB4	101	PA9/PGMM1	137	PB26
30	PA26/PGMD14	66	VDDCORE	102	PA10/PGMM2	138	PB28/TMP3
31	PA25/PGMD13	67	PB5	103	PA11/PGMM3	139	PB16/TMP1
32	PA24/PGMD12	68	PC7	104	PA13/PGMD1	140	PA1/PGMEN1
33	PA20/PGMD8	69	PC0	105	PA14/PGMD2	141	PB17
34	PA19/PGMD7	70	NRST	106	PA15/PGMD3	142	PA7/PGMNVALID
35	PA18/PGMD6	71	VDDIO	107	PA16/PGMD4	143	VDDIO
36	PA8/PGMM0	72	PA30	108	PA17/PGMD5	144	PA2

5. Power Supply and Power Control

5.1 Power Supplies

The SAM4C has several types of power supply pins. In most cases, a single supply scheme for all power supplies (except VDDBU) is possible. Figure 5-1 shows power domains according to the different power supply pins.
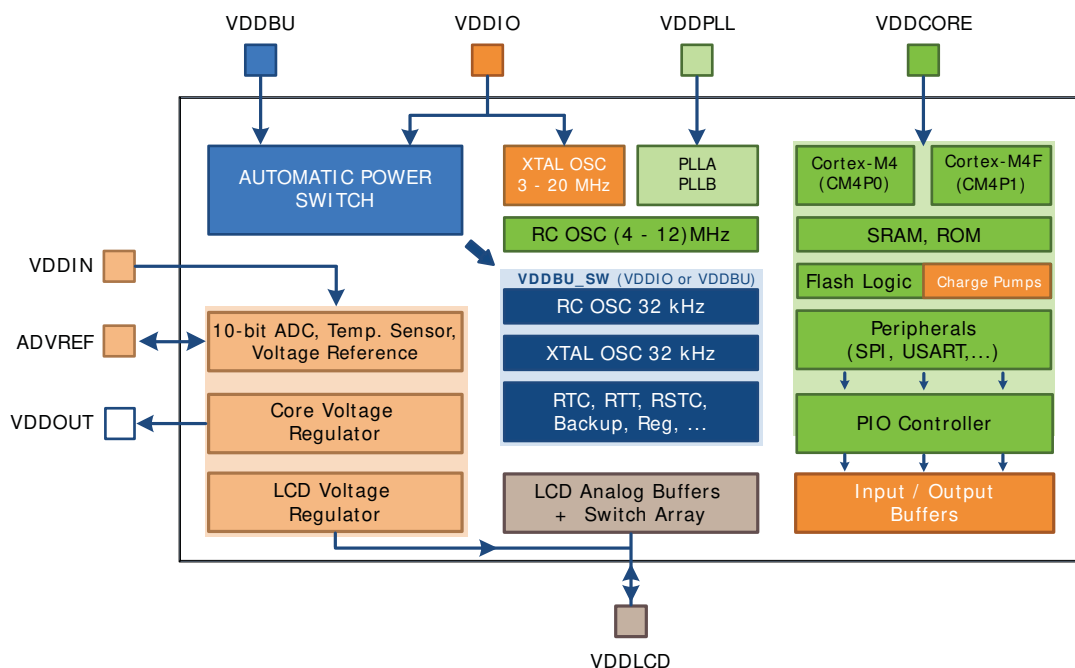
Figure 5-1. Power Domains

Table 5-1. Power Supply Voltage Ranges[1]

Power Supply	Range	Comments
VDDIO	1.6V to 3.6V	Flash memory charge pumps supply for erase and program operations, and read operation. Input/Output buffers supply. USB transceiver power supply. Restrictions on range may apply. Refer to Section 46. "Electrical Characteristics".
VDDBU[2]	1.6V to 3.6V	Backup area power supply. VDDBU is automatically disconnected when VDDIO is present (> 1.9V).
VDDIN	1.6V to 3.6V	Core voltage regulator supply, LCD voltage regulator supply, ADC and programmable voltage reference supply. Restrictions on range may apply. Refer to Section 46. "Electrical Characteristics".
VDDLCD	2.5V to 3.6V	LCD voltage regulator output. External LCD power supply input (LCD regulator not used). VDDIO/VDDIN must be supplied when the LCD Controller is used.

Table 5-1. Power Supply Voltage Ranges[(1)] (Continued)

Power Supply	Range	Comments
VDDPLL	1.08V to 1.32V	PLLA and PLLB supply.
VDDCORE	1.08V to 1.32V	Core logic, processors, memories and analog peripherals supply.

Notes: 1. In all power modes except Backup mode, all power supply inputs must be powered.

2. VDDBU must be powered from an external source to ensure proper start-up. The external source must meet the timing and voltage level requirements described in Section 46.2.2 "Recommended Power Supply Conditions at Powerup".

5.1.1 Core Voltage Regulator

The core voltage regulator is managed by the Supply Controller.

It features two operating modes:

- In Normal mode, the quiescent current of the voltage regulator is less than 500 µA when sourcing maximum load current, i.e. 120 mA. Internal adaptive biasing adjusts the regulator quiescent current depending on the required load current. In Wait Mode, quiescent current is only 5 µA.
- In Backup mode, the voltage regulator consumes less than 100 nA while its output (VDDOUT) is driven internally to GND.

The default output voltage is 1.20V and the start-up time to reach Normal mode is less than 500 µs.

For further information, refer to Table 46-16 "Core Voltage Regulator Characteristics".

5.1.2 LCD Voltage Regulator

The SAM4C embeds an adjustable LCD voltage regulator that is managed by the Supply Controller.

This internal regulator is designed to supply the Segment LCD outputs. The LCD regulator output voltage is software selectable with 16 levels to adjust the display contrast.

If not used, its output (VDDLCD) can be bypassed (Hi-z mode) and an external power supply can be provided onto the VDDLCD pin. In this case, VDDIO still needs to be supplied.

The LCD voltage regulator can be used in all power modes (Backup, Wait, Sleep and Active).

For further information, refer to Table 46-18 "LCD Voltage Regulator Characteristics".

5.1.3 Automatic Power Switch

The SAM4C features an automatic power switch between VDDBU and VDDIO. When VDDIO is present, the backup zone power supply is powered by VDDIO and current consumption on VDDBU is about zero (around 100 nA, typ.). When VDDIO is removed, the backup area of the device is supplied from VDDBU. Switching between VDDIO and VDDBU is transparent to the user.

5.1.4 Typical Powering Schematics

The SAM4C series supports 1.6V to 3.6V single-supply operation. Restrictions on this range may apply depending on enabled features. Refer to Section 46. "Electrical Characteristics".

Note: Figure 5-2, Figure 5-3 and Figure 5-4 show simplified schematics of the power section.

5.1.4.1 Single Supply Operation

Figure 5-2 below shows a typical power supply scheme with a single power source. VDDIO, VDDIN, and VDDBU are derived from the main power source (typically a 3.3V regulator output) while VDDCORE, VDDPLL, and VDDLCD are fed by the embedded regulator outputs.

Figure 5-2.   Single Supply Operation
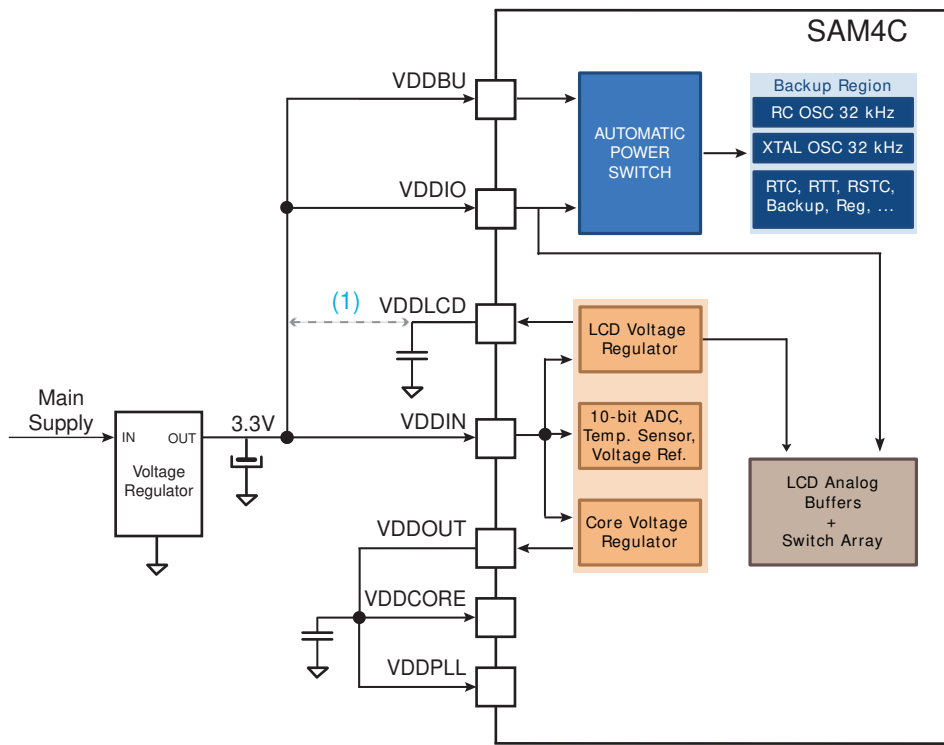
Note: 1.   Internal LCD Voltage Regulator can be disabled to save its operating current. VDDLCD must then be provided
externally.

5.1.4.2 Single Supply Operation with Backup Battery

Figure 5-3 shows the single-supply operation schematic from Figure 5-2, improved by adding a backup capability. VDDBU is supplied with a separate backup battery while VDDIO and VDDIN are still connected to the main power source. Note that the TMP1 to TMP3 and RTCOUT0 pins cannot be used in Backup mode as they are referred to VDDIO, which is not powered in this application case.

Figure 5-3. Single Supply Operation with Backup Battery
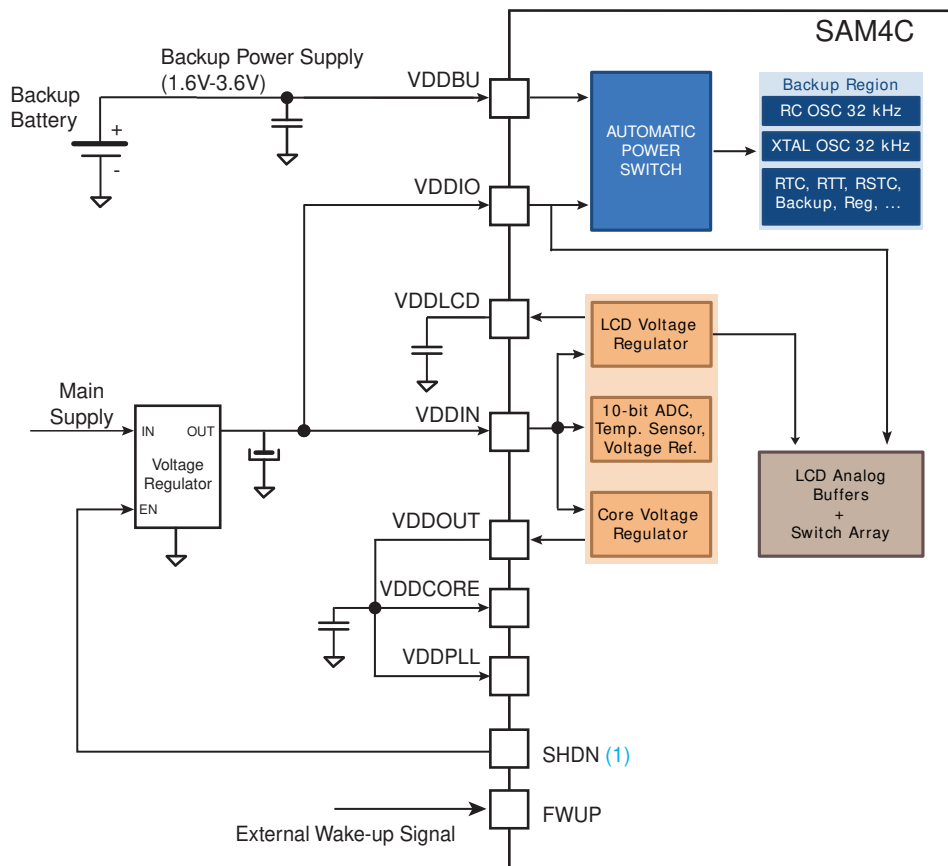
Note: 1. Example with the SHDN pin used to control the main regulator enable pin. SHDN defaults to VDDBU at startup and when the device wakes up from a wake-up event (external pin, RTC alarm, etc.). When the device is in Backup mode, SHDN defaults to 0.

5.1.4.3 Single Power Supply using One Main Battery and LCD Controller in Backup Mode

Figure 5-4 below shows a typical power supply scheme that maintains VDDBU, VDDIO, and VDDLCD when entering Backup mode. This is useful to enable the display and/or some supplementary wake-up sources in Backup mode when the main voltage is not present.

In this power supply scheme, the SAM4C can wake up both from an internal wake-up source, such as RTT, RTC and VDDIO Supply Monitor, and from an external source, such as generic wake-up pins (WKUPx), anti-tamper inputs (TMPx) or force wake-up (FWUP).

Note: The VDDIO supply monitor only wakes up the device from Backup mode on a negative-going VDDIO supply (as system alert). As a result, the supply monitor cannot be used to wake up the device when the VDDIO supply is rising at power cycle. Refer to Section 20. "Supply Controller (SUPC)" for more information on the VDDIO supply monitor.

Figure 5-4. Single Power Supply using Battery and LCD Controller in Backup Mode
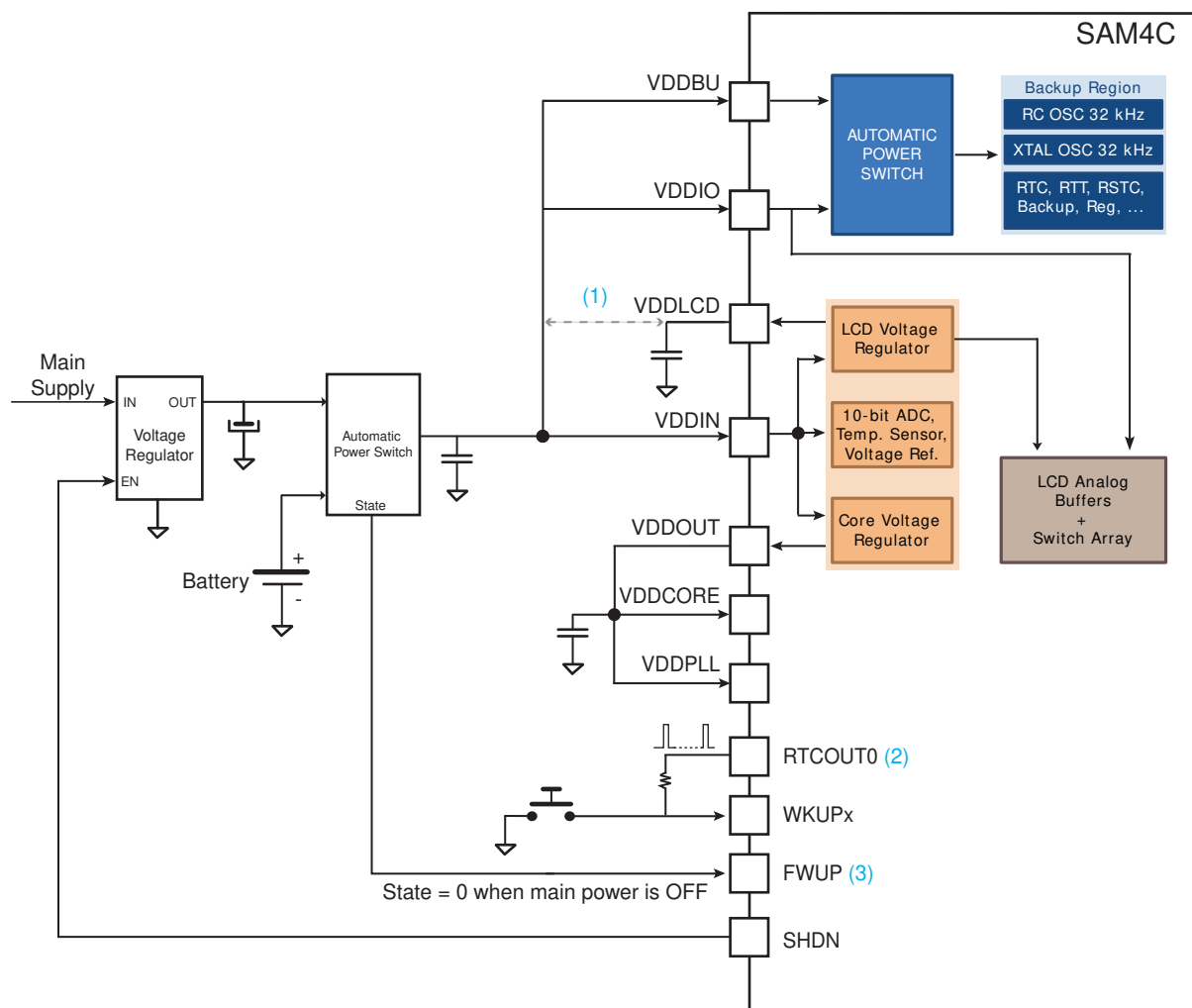
Notes: 1. Internal LCD Voltage Regulator can be disabled to save its operating current. VDDLCD must then be provided externally.
2. RTCOUT0 signal is used to make a dynamic wake-up. WKUPx pin is pulled-up with a low duty cycle to avoid battery discharge by permanent activation of the switch.
3. The State output of the automatic power switch indicates to the device that the main power is back and forces its wake-up.

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5.1.4.4 Wake-up, Anti-tamper and RTCOUT0 Pins

In all power supply figures shown above, if generic wake-up pins other than WKUP0/TMP0 are used either as a wake-up or a fast startup input, or as anti-tamper inputs, VDDIO must be present. This also applies to the RTCOUT0 pin.

5.1.4.5 General-purpose IO (GPIO) State in Low-power Modes

In dual-power supply schemes shown in Figure 5-3 and Figure 5-4, where Backup or Wait mode must be used, configuration of the GPIO lines is maintained in the same state as before entering Backup or Wait mode. Thus, to avoid extra current consumption on the VDDIO power rail, the user must configure the GPIOs either as an input with pull-up or pull-down enabled, or as an output with low or high level to comply with external components.

5.1.4.6 Default General-purpose IOs (GPIO) State after Reset

The reset state of the GPIO lines after reset is given in Table 11-5 "Multiplexing on PIO Controller A (PIOA)", Section 11-6 "Multiplexing on PIO Controller B (PIOB)" and Table 11-7 "Multiplexing on PIO Controller C (PIOC)". For further details about the GPIO and system lines, wake-up sources and wake-up time, and typical power consumption in different low-power modes, refer to Table 5-2 "Low-power Mode Configuration Summary".

5.2 Clock System Overview

Figure 5-5 and Figure 5-6 illustrate the typical operation of the whole SAM4C clock system in case of single crystal (32.768 kHz) applications. Note:

- The 32 kHz crystal oscillator can be the source clock of the 8 MHz digital PLL (PLLA).
- The 8 MHz clock can feed the high frequency PLL (PLLB) input.
- The output of the PLLB can be used as a main clock for both cores and the peripherals.

Full details of the clock system are provided in Section 29. "Clock Generator" and Section 30. "Power Management Controller (PMC)".

Figure 5-5. SAM4C16/8/4 Global Clock System
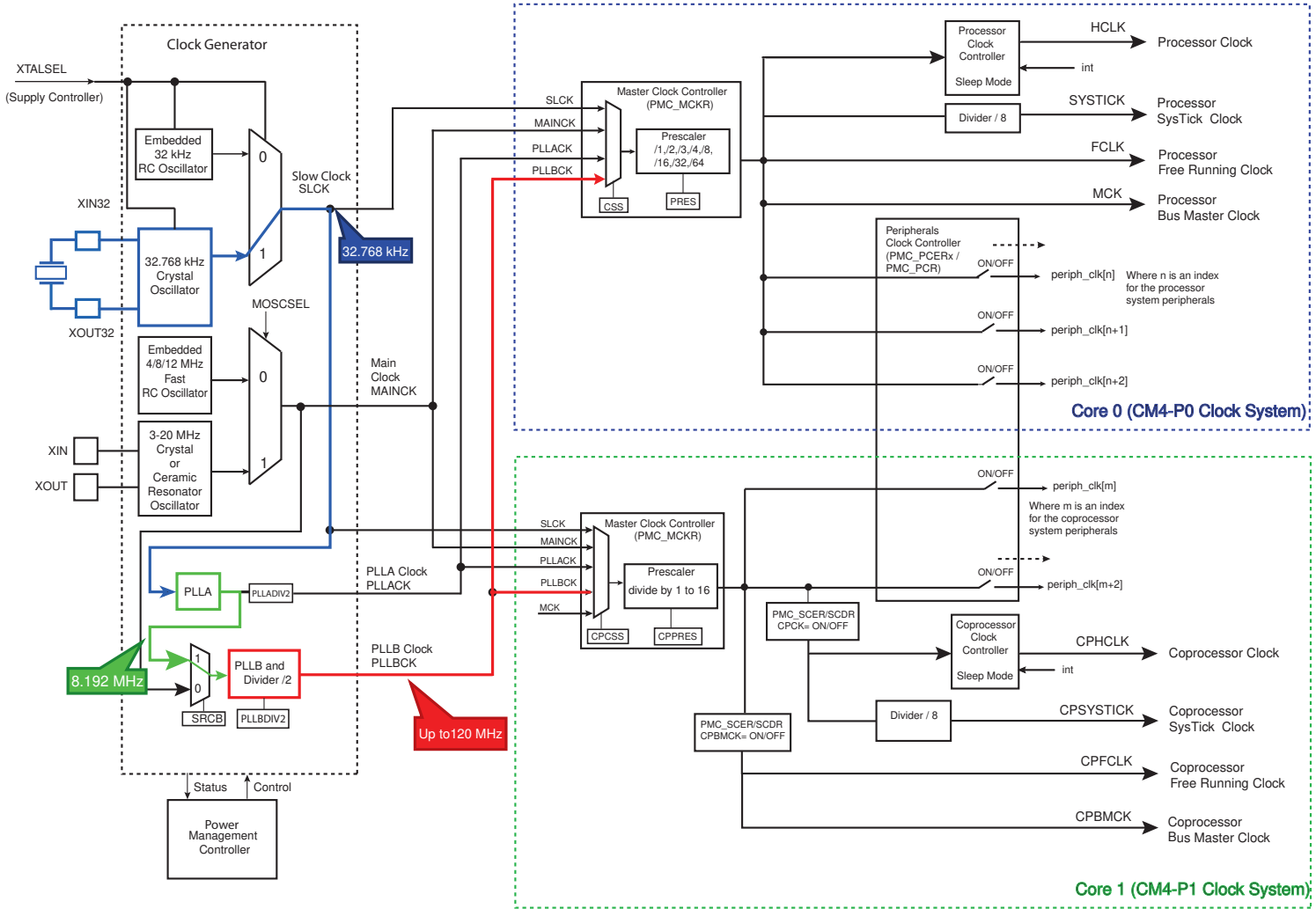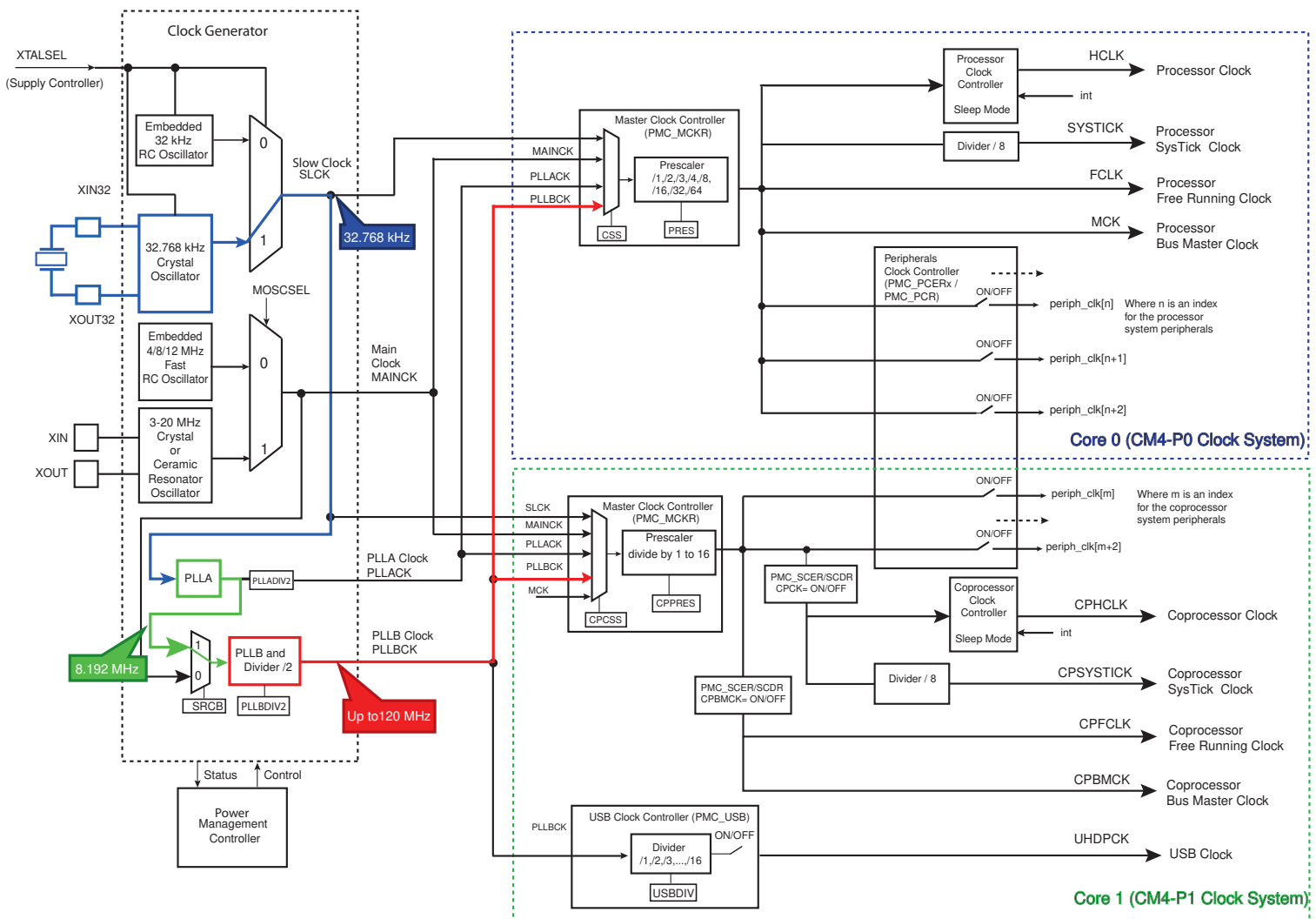
Figure 5-6. SAM4C32 Global Clock System

Figure 5-6. SAM4C32 Global Clock System

5.3 System State at Power-up

5.3.1 Device Configuration after the First Power-up

At the first power-up, the SAM4C boots from the ROM. The device configuration is defined by the SAM-BA boot program.

5.3.2 Device Configuration after a Power Cycle when Booting from Flash Memory

After a power cycle of all the power supply rails, the system peripherals, such as the Flash Controller, the Clock Generator, the Power Management Controller and the Supply Controller, are in the following states:

- Slow Clock (SLCK) source is the internal 32 kHz RC Oscillator (32 kHz crystal oscillator is disabled)
- Main Clock (MAINCK) source is set to the 4 MHz internal RC Oscillator
- 3–20 MHz crystal oscillator and PLLs are disabled
- Core Brownout Detector and Core Reset are enabled
- Backup Power-on-reset is enabled
- VDDIO Supply Monitor is disabled
- Flash Wait State (FWS) bit in the EEFC Flash Mode Register is set to 0
- Core 0 Cache Controller (CMCC0) is enabled (only used if the application link address for the Core 0 is 0x11000000)
- Sub-system 1 is in the reset state and not clocked

5.3.3 Device Configuration after a Reset

After a reset or a wake-up from Backup mode, the following system peripherals default to the same state as after a power cycle:

- Main Clock (MAINCK) source is set to the 4 MHz internal RC oscillator
- 3–20 MHz crystal oscillator and PLLs are disabled
- Flash Wait State (FWS) bit in the EEFC Flash Mode Register is set to 0
- Core 0 Cache Controller (CMCC0) is enabled (only used if the application link address for the Core 0 is 0x11000000)
- Sub-system 1 is in the reset state and not clocked

The states of the other peripherals are saved in the backup area managed by the Supply Controller as long as VDDBU is maintained during device reset:

- Slow Clock (SLCK) source selection is written in SUPC_ CR.XTALSEL.
- Core Brownout Detector enable/disable is written in SUPC_MR.BODDIS.
- Backup Power-on-reset enable/disable is written in the SUPC_MR.BUPPOREN.
- VDDIO Supply Monitor mode is written in the SUPC_SMMR.

5.4 Active Mode

Active mode is the normal running mode, with the single core or the dual cores executing code. The system clock can be the fast RC oscillator, the main crystal oscillator or the PLLs. The Power Management Controller (PMC) can be used to adapt the frequency and to disable the peripheral clocks when unused.

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5.5 Low-power Modes

The various low-power modes (Backup, Wait and Sleep modes) of the SAM4C are described below. Note that the Segmented LCD Controller can be used in all low-power modes.

Note: The Wait For Event instruction (WFE) of the Cortex-M4 core can be used to enter any of the low-power modes, however this may add complexity to the design of application state machines. This is due to the fact that the WFE instruction is associated with an event flag of the Cortex core that cannot be managed by the software application. The event flag can be set by interrupts, a debug event or an event signal from another processor. When an event occurs just before WFE execution, the processor takes it into account and does not enter Low-power mode. Atmel has made provision to avoid using the WFE instruction. The workarounds to ease application design, including the use of the WFE instruction, are given in the following description of the low-power mode sequences.

5.5.1 Backup Mode

The purpose of Backup mode is to achieve the lowest possible power consumption in a system that executes periodic wake-ups to perform tasks but which does not require fast start-up time. The total current consumption is 0.5 µA typical on VDDBU.

The Supply Controller, power-on reset, RTT, RTC, backup registers and the 32 kHz oscillator (RC or crystal oscillator selected by software in the Supply Controller) are running. The regulator and the core supplies are off. The power-on-reset on VDDBU can be deactivated by software.

Wake-up from Backup mode can be done through the Force Wake-up (FWUP) pin, WKUP0, WKUP1 to WKUP15 pins, the VDDIO Supply Monitor (SM) if VDDIO is supplied, or through an RTT or RTC wake-up event. Wake-up pins multiplexed with anti-tampering functions are additional possible sources of a wake-up if an anti-tampering event is detected. The TMP0 pad is supplied by the backup power supply (VDDBU). Other anti-tamper input pads are supplied by VDDIO.

The LCD Controller can be used in Backup mode. The purpose is to maintain the displayed message on the LCD display after entering Backup mode. The current consumption on VDDIN to maintain the LCD is 10 µA typical. Refer to Section 46. "Electrical Characteristics".

In case the VDDIO power supply is maintained with VDDBU when entering Backup mode, it is up to the application to configure all PIO lines in a stable and known state to avoid extra power consumption or possible current path with the input/output lines of the external on-board devices.

5.5.1.1 Entering and Exiting Backup Mode

To enter Backup mode, follow the steps in the sequence below:

1. Depending on the application, set the PIO lines in the correct mode and configuration (input pull-up or pull-down, output low or high levels).
2. Disable the Main Crystal Oscillator (enabled by SAM-BA boot if the device is booting from ROM).
3. Configure PA30/PA31 (XIN/XOUT) into PIO mode depending on their use.
4. Disable the JTAG lines using the SFR1 register in Matrix 0 (by default, internal pull-up or pull-down is disabled on JTAG lines).
5. Disable the USB pads and transceiver using the SFR1 register in Matrix 0 (SAM4C32E only).
6. Enable the RTT in 1 Hz mode.
7. Disable Normal mode of the RTT (RTT will run in 1 Hz mode).
8. To reduce power consumption, disable the POR backup if not needed.

Note: The POR BU provides critical functionality to ensure the MCU backup logic will be properly reset in the event VDDBU drops below the minimum specification. If this protection is not necessary, the backup POR may be disabled to reduce power consumption.

9. Disable the Core brownout detector.

10. Select one of the following methods to complete the sequence:
   a. To enter Backup mode using the VROFF bit:
      - Write a 1 to the VROFF bit of SUPC_CR.
   b. To enter Backup mode using the WFE instruction:
      - Write a 1 to the SLEEPDEEP bit of the Cortex-M4 processor.
      - Execute the WFE instruction of the processor.

After this step, the core voltage regulator is shut down and the SHDN pin goes low. The digital internal logic (cores, peripherals and memories) is not powered. The LCD controller can be enabled if needed before entering Backup mode.

Whether the VROFF bit or the WFE instruction was used to enter Backup mode, the system exits Backup mode if one of the following enabled wake-up events occurs:

- WKUP[0–15] pins
- Force Wake-up pin
- VDDIO Supply Monitor (if VDDIO is present, and VDDIO supply falling)
- Anti-tamper event detection
- RTC alarm
- RTT alarm

After exiting Backup mode, the device is in the reset state. Only the configuration of the backup area peripherals remains unchanged.

Note that the device does not automatically enter Backup mode if VDDIN is disconnected, or if it falls below minimum voltage. The Shutdown pin (SHDN) remains high in this case.

For current consumption in Backup mode, refer to Section 46. "Electrical Characteristics".

5.5.2 Wait Mode

The purpose of Wait mode is to achieve very low power consumption while maintaining the whole device in a powered state for a start-up time of a few µs. For current consumption in Wait mode, refer to Section 46. "Electrical Characteristics".

In Wait mode, the bus and peripheral clocks of Sub-system 0 and Sub-system 1 (MCK/CPBMCK), the clocks of Core 0 and Core 1 (HCLK/CPHCLK) are stopped when Wait mode is entered (refer to Section 5.5.2.1 "Entering and Exiting Wait Mode"). However, the power supply of core, peripherals and memories are maintained using Standby mode of the core voltage regulator.

The SAM4C is able to handle external and internal events in order to perform a wake-up. This is done by configuring the external WKUPx lines as fast startup wake-up pins (refer to Section 5.7 "Fast Start-up"). RTC alarm, RTT alarm and anti-tamper events can also wake up the device.

Wait mode can be used together with Flash in Read-Idle mode, Standby mode or Deep Power-down mode to further reduce the current consumption. Flash in Read-Idle mode provides a faster start-up; Standby mode offers lower power consumption.

5.5.2.1 Entering and Exiting Wait Mode
1. Stop Sub-system 1.
2. Select the 4/8/12 MHz fast RC Oscillator as Main Clock[1].
3. Disable the PLL if enabled.
4. Clear the internal wake-up sources.
5. Depending on the application, set the PIO lines in the correct mode and configuration (input pull-up or pull-down, output low or high level).
6. Disable the Main Crystal Oscillator (enabled by SAM-BA boot if device is booting from ROM).

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7. Configure PA30/PA31 (XIN/XOUT) into PIO mode according to their use.

8. Disable the JTAG lines using the SFR1 register in Matrix 0 (by default, internal pull-up or pull-down is disabled on JTAG lines).

9. Disable the USB pads and transceiver using the SFR1 register in Matrix 0.

10. Set the FLPM field in the PMC Fast Startup Mode Register (PMC_FSMR)[2].

11. Set the Flash Wait State (FWS) bit in the EEFC Flash Mode Register to 0.

12. Select one of the following methods to complete the sequence:

  a. To enter Wait mode using the WAITMODE bit:

  - Set the WAITMODE bit to 1 in the PMC Main Oscillator Register (CKGR_MOR).
  - Wait for Master Clock Ready MCKRDY = 1 in the PMC Status Register (PMC_SR).

  b. To enter Wait mode using the WFE instruction:

  - Select the 4/8/12 MHz fast RC Oscillator as Main Clock.
  - Set the FLPM field in the PMC Fast Startup Mode Register (PMC_FSMR).
  - Set Flash Wait State at 0.
  - Set the LPM bit in the PMC Fast Startup Mode Register (PMC_FSMR).
  - Write a 0 to the SLEEPDEEP bit of the Cortex-M4 processor.
  - Execute the Wait-For-Event (WFE) instruction of the processor.

Notes: 1. Any frequency can be chosen. The 12 MHz frequency will provide a faster start-up compared to the 4 MHz, but with the increased current consumption (in the µA range). Refer to Section 46. "Electrical Characteristics".
2. Depending on the Flash Low-power Mode (FLPM) value, the Flash enters three different modes:
  - If FLPM = 0, the Flash enters Stand-by mode (Low consumption)
  - If FLPM = 1, the Flash enters Deep Power-down mode (Extra low consumption)
  - If FLPM = 2, the Flash enters Idle mode. Memory is ready for Read access

Whether the WAITMODE bit or the WFE instruction was used to enter Wait mode, the system exits Wait mode if one of the following enabled wake-up events occurs:

- WKUP[0–15] pins in Fast wake-up mode
- Anti-tamper event detection
- RTC alarm
- RTT alarm

After exiting Wait mode, the PIO controller has the same configuration state as before entering Wait mode. The SAM4C is clocked back to the RC oscillator frequency which was used before entering Wait mode. The core will start fetching from Flash at this frequency. Depending on the configuration of the Flash Low-power Mode (FLPM) bits used to enter Wait mode, the application has to reconfigure it back to Read-idle mode.

5.5.3 Sleep Mode

The purpose of Sleep mode is to optimize power consumption of the device versus response time. In this mode, only the core clocks of CM4P0 and/or CM4P1 are stopped. Some of the peripheral clocks can be enabled depending on the application needs. The current consumption in this mode is application dependent. This mode is entered using Wait for Interrupt (WFI) or Wait for Event (WFE) instructions of the Cortex-M4.

The processor can be awakened from an interrupt if the WFI instruction of the Cortex-M4 is used to enter Sleep mode, or from a wake-up event if the WFE instruction is used. The WFI instruction can also be used to enter Sleep mode with the SLEEPONEXIT bit set to 1 in the System Control Register (SCB_SCR) of the Cortex-M. If the SLEEPONEXIT bit of the SCB_SCR is set to 1, when the processor completes the execution of an exception handler, it returns to Thread mode and immediately enters Sleep mode. This mechanism can be used in applications that require the processor to run only when an exception occurs. Setting the SLEEPONEXIT bit to 1 enables an interrupt-driven application in order to avoid returning to an empty main application.