Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

SAM4CM Series

Atmel | SMART ARM-based Flash MCU

DATASHEET

Description

The Atmel® | SMART SAM4CM series represents a family of system-on-chip solutions for residential and polyphase metering applications. The devices offer up to class 0.2 metrology accuracy over a dynamic range of 3000:1 within the industrial temperature range and are compliant with ANSI C12.20-2002 and IEC 62053-22 standards.

A seamless extension of Atmel's SAM4, SAM4CP and SAM4C family of microcontrollers and solutions for smart grid security and communications applications, these metrology-enabled devices offer an unprecedented level of integration and flexibility with dual 32-bit ARM® Cortex®-M4 RISC processors running at a maximum speed of 120 MHz each(1), up to 2 Mbytes of embedded Flash, 304 Kbytes of SRAM and on-chip cache.

The unique dual ARM Cortex-M4 architecture supports implementation of signal processing, application and communications firmware in independent partitions, and offers the ability to extend program and data memory via parallel external bus interface (EBI) to ensure scalability of the design to meet future requirements.

The peripheral set includes metrology-specific precision voltage reference, up to seven (7) simultaneously sampled Sigma-Delta ADC subsystems supporting three (3) voltage and four (4) current measurement channels (polyphase versions only), an extensive set of embedded cryptographic features, anti-tamper, Floating Point Unit (FPU), four USARTs, two UARTs, two TWIs, four SPIs, three 16-bit PWMs, two 3-channel general-purpose 16-bit timers, 6-channel 10-bit ADC, battery-backed RTC with <1 µA consumption and a 38 x 6 segmented LCD controller.

To ensure the distinct separation of metrology and application or communication functions, the SAM4CM integrates a dedicated Cortex-M4F core that manages all necessary metrology resources and memory.

Features

- Application/Master Core
  - ARM Cortex-M4 running at up to 120 MHz[1]
  - Memory Protection Unit (MPU)
  - DSP Instruction
  - Thumb®-2 instruction set
  - Instruction and Data Cache Controller with 2 Kbytes Cache Memory
  - Memories
    - Up to 2 Mbytes of Embedded Flash for Program Code (I-Code bus) and Program Data (D-Code bus) with Built-in ECC (2-bit error detection and 1-bit correction per 128 bits)
    - Up to 256 Kbytes of Embedded SRAM (SRAM0) for Program Data (System bus)
    - 8 Kbytes of ROM with embedded bootloader routines (UART) and In-Application Programming (IAP) routines
- Coprocessor (provides ability to separate application, communication or metrology functions)
  - ARM Cortex-M4F running at up to 120 MHz[1]
  - IEEE® 754 Compliant, Single-precision Floating-Point Unit (FPU)
  - DSP Instruction
  - Thumb-2 instruction set
  - Instruction and Data Cache Controller with 2 Kbytes of Cache Memory
  - Memories
    - Up to 32 Kbytes of Embedded SRAM (SRAM1) for Program Code (I-Code bus) and Program Data (D-Code bus and System bus)
    - Up to 16 Kbytes of Embedded SRAM (SRAM2) for Program Data (System bus)
- Symmetrical/Asynchronous Dual Core Architecture
  - Interrupt-based Interprocessor Communication
  - Asynchronous Clocking
  - One Interrupt Controller (NVIC) for each core
  - Each Peripheral IRQ routed to each NVIC Input
- Cryptography
  - High-performance AES 128 to 256 with various modes (GCM, CBC, ECB, CFB, CBC-MAC, CTR)
  - TRNG (up to 38 Mbit/s stream, with tested Diehard and FIPS)
  - Public Key Crypto accelerator and associated ROM library for RSA, ECC, DSA, ECDSA
  - Integrity Check Module (ICM) based on Secure Hash Algorithm (SHA1, SHA224, SHA256), DMA-assisted
- Safety
  - Up to two physical Anti-tamper Detection I/Os with Time Stamping and Immediate Clear of General Backup Registers
  - Security Bit for Device Protection from JTAG Accesses
- Shared System Controller
  - Power Supply
    - Embedded core and LCD voltage regulator for single-supply operation
    - Power-on-Reset (POR), Brownout Detector (BOD) and Dual Watchdog for safe operation
    - Ultra-low-power Backup mode (< 0.5 µA Typical @ 25°C)

- Clock
  - 3 to 20 MHz oscillator supporting crystal, ceramic resonator or external clock signal. Also supports clock failure detection
  - Ultra-low power 32.768 kHz oscillator supporting crystal or external clock signal and frequency monitoring
  - High-precision 4/8/12 MHz factory-trimmed internal RC oscillator with on-the-fly trimming capability
  - One high-frequency PLL up to 240 MHz, one 8 MHz PLL with internal 32 kHz input, as source for high-frequency PLL
  - Low-power slow clock internal RC oscillator as permanent clock
- Ultra-low-power RTC with Gregorian and Persian Calendar, Waveform Generation in Backup mode and Clock Calibration Circuitry for 32.768 kHz Crystal Frequency Compensation Circuitry
- Up to 23 Peripheral DMA (PDC) Channels

- Shared Peripherals
  - One Low-power Segmented LCD Controller
    - Display capacity of 38 segments and 6 common terminals
    - Software-selectable LCD output voltage (Contrast)
    - Low current consumption in Low-power mode
    - Can be used in Backup mode
  - Up to four USARTs with ISO7816, IrDA®, RS-485, SPI and Manchester Mode
  - Two 2-wire UARTs with one UART (UART1) supporting optical transceiver providing an electrically isolated serial communication with hand-held equipment, such as calibrators, compliant with ANSI-C12.18 or IEC62056-21 norms
  - Up to two 400 kHz Master/Slave and Multi-Master Two-wire Interfaces (I^2C compatible)
  - Up to four Serial Peripheral Interfaces (SPI)
  - Two 3-channel 16-bit Timer/Counters with Capture, Waveform, Compare and PWM modes
  - Quadrature Decoder Logic and 2-bit Gray Up/Down Counter for Stepper Motor
  - 3-channel 16-bit Pulse Width Modulator
  - 32-bit Real-time Timer
- Energy Metering Analog Front-End
  - Two-phase (SAM4CMS) or three-phase (SAM4CMP) Energy Metering Analog Front-End
  - Works with the Atmel MCU Metrology library
  - Compliant with Electricity Metering Standards up to Class 0.2 (ANSI C12.20-2002 and IEC 62053-22)
  - Four or seven Sigma-Delta ADC measurement channels, 20-bit resolution, 102 dB dynamic range
  - Current channels with Pre-gain (x1, x2, x4, x8) support directly connected Shunt, Current Transformer and Rogowsky Coils sensors without any active components
  - Dedicated current channel for neutral current measurement (anti-tamper)
  - 1.2V Precision Voltage Reference. Temperature drift: 10 ppm/C typical with software correction using factory-programmed calibration registers (SAM4CMx8C/16C/32C devices), 50 ppm typical (SAM4CMS4C devices)
  - Dedicated 2.8V LDO regulator to supply the Analog Front-End
  - 3.0V to 3.6V operation, ultra-low-power: < 2.5 mW / channel @ 3.3V
- Analog Conversion Block
  - 6-channel, 500 kS/s, Low-power 10-bit SAR ADC with Digital Averager providing 12-bit Resolution at 30 kS/s
  - Software-controlled On-chip Reference ranging from 1.6V to 3.4V
  - Temperature Sensor and Backup Battery Voltage Measurement Channel

- Debug
  - Star Topology AHB-AP Debug Access Port Implementation with Common SW-DP / SWJ-DP Providing Higher Performance than Daisy-chain Topology
  - Debug Synchronization between both Cores (cross triggering to/from each core for Halt and Run Mode)
- I/O
  - Up to 57 I/O lines with External Interrupt Capability (edge or level sensitivity), Schmitt Trigger, Internal Pull-up/pull-down, Debouncing, Glitch Filtering and On-die Series Resistor Termination
- Package
  - 100-lead LQFP, 14 x 14 mm, pitch 0.5 mm

Note: 1. 120 MHz: -40°C/+85°C, VDDCORE = 1.2V

1. Configuration Summary

The SAM4CM devices differ in memory size, package and features. Table 1-1 summarizes the different device configurations.

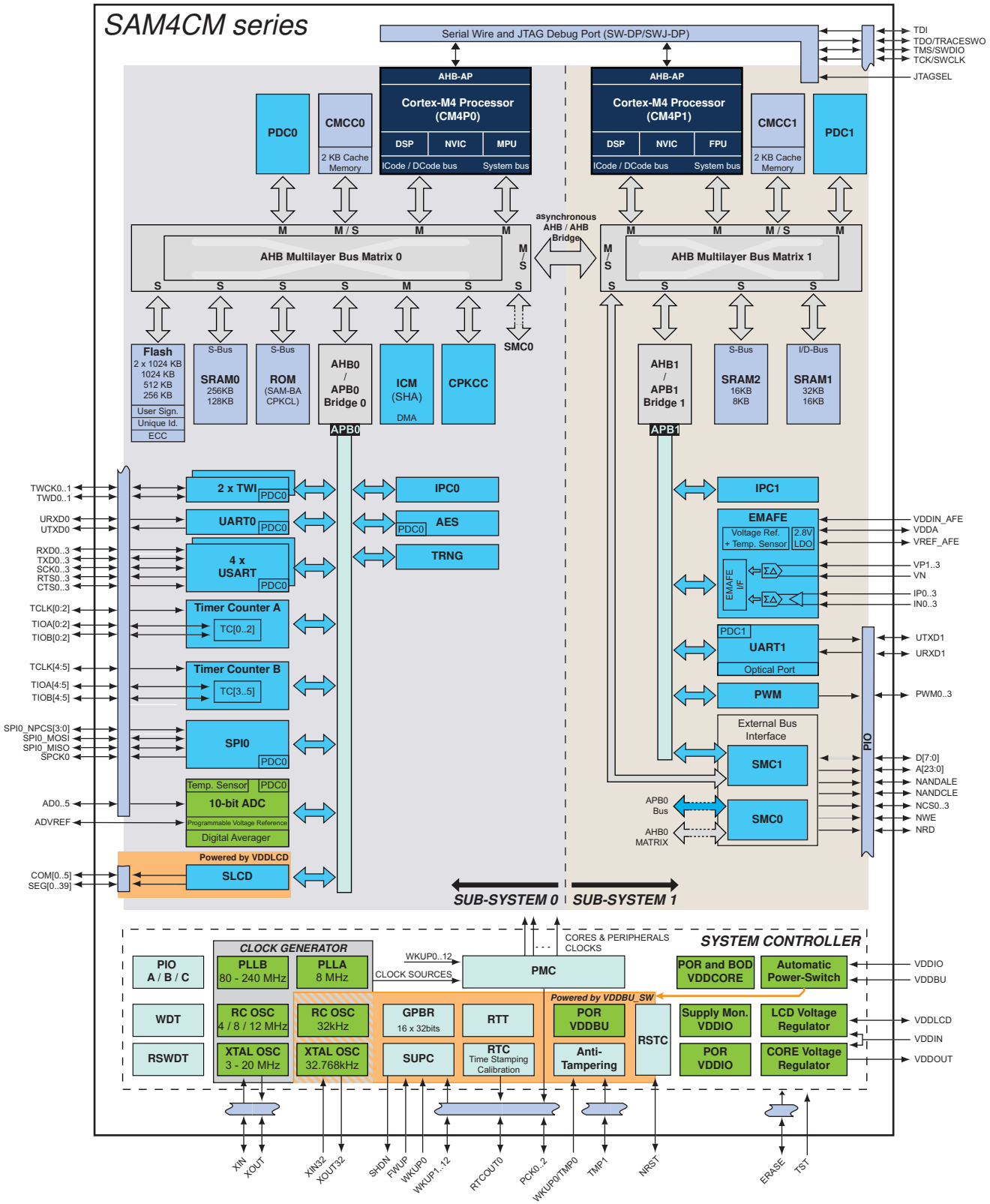
Table 1-1. Configuration Summary

Feature	SAM4CMP32C	SAM4CMP16C	SAM4CMP8C	SAM4CMS32C	SAM4CMS16C	SAM4CMS8C	SAM4CMS4C
Flash	2048 Kbytes	1024 Kbytes	512 Kbytes	2048 Kbytes	1024 Kbytes	512 Kbytes	256 Kbytes
SRAM	256 + 32 +16 Kbytes	128 + 16 + 8 Kbytes		256 + 32 +16 Kbytes	128 + 16 + 8 Kbytes		
Package	LQFP 100						
Number of PIOs	52			57			
External Bus Interface	8-bit data						
16-bit Timer	6 channels						
16-bit PWM	3 channels						
UART / USART	2/3			2/4			
SPI(1)	1/4 + 3			1/4 + 4			
TWI	2						
10-bit ADC Channels(2)	6						
Energy Metering Analog Front End	7 channels (3 voltages, 4 currents)			4 channels (2 voltages, 2 currents)			
Cryptography	AES, CPKCC, ICM (SHA), TRNG						
Segmented LCD	33 segments × 6 commons			38 segments × 6 commons			
Anti-Tampering Inputs	1			2			
Flash Page Size	512 bytes						
Flash Pages	2 × 2048	2048	1024	2 × 2048	2048	1024	512
Flash Lock Region Size	8 Kbytes						
Flash Lock Bits	2 × 128	128	64	2 × 128	128	64	32

Notes: 1. 1/4 + 3 = Number of SPI Controllers / Number of Chip Selects + Number of USARTs with SPI mode.
2. One channel is reserved for internal temperature sensor and one channel for VDDBU measurement.

2. Block Diagram

Figure 2-1. SAM4CM Series Block Diagram



3. Signal Description

Table 3-1 provides details on signal names classified by peripheral.

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Power Supplies					
VDDIO	See Table 5-1	Power	–	–	–
VDDBU			–	–	–
VDDIN			–	–	–
VDDLCD			–	–	–
VDDOUT			–	–	–
VDDPLL			–	–	–
VDDCORE			–	–	–
VDDIN_AFE			–	–	–
VDDA			–	–	–
GND		Ground	–	–	–
GNDA			–	–	–
GNDREF			–	–	–
Clocks, Oscillators and PLLs					
XIN	Main Crystal Oscillator Input	Analog Digital	–	VDDIO	XIN is a clock input when the 3 to 20 MHz oscillator is in Bypass mode.
XOUT	Main Crystal Oscillator Output		–		
XIN32	Slow Clock Crystal Oscillator Input	Analog Digital	–	VDDBU	XIN32 is a clock input when the 32.768 kHz oscillator is in Bypass mode.
XOUT32	Slow Clock Crystal Oscillator Output		–		
PCK0–PCK2	Programmable Clock Output	Output	–	VDDIO	–
Real-Time Clock					
RTCOUT0	Programmable RTC Waveform Output	Digital Output	–	VDDIO	–
Supply Controller					
FWUP	Force Wake-up Input	Digital Input	Low	VDDBU	External Pull-up needed
TMP0	Anti-tampering Input 0	Digital Input	–	VDDBU	External Pull-up or Pull-down resistor needed
TMP1	Anti-tampering Input 1	Digital Input	–	VDDIO	–
SHDN	Active Low Shutdown Control	Digital Output	–	VDDBU	0: The device is in Backup mode. 1: The device is running (not in Backup mode).
WKUP0	Wake-up Input 0	Digital Input	–	VDDBU	–

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
WKUP1–13	Wake-up Input 1 to 13	Digital Input	–	VDDIO	–
Serial Wire/JTAG Debug Port - SWJ-DP					
TCK/SWCLK	Test Clock/Serial Wire Clock	Digital Input	–	VDDIO	–
TDI	Test Data In		–		
TDO/TRACESWO	Test Data Out / Trace Asynchronous Data Out	Digital Output	–	VDDIO	–
TMS/SWDIO	Test Mode Select input / Serial Wire Input/Output	Digital I/O	–		
JTAGSEL	JTAG Selection	Digital Input	High	VDDBU	Permanent Internal pull-down
Flash Memory					
ERASE	Flash and NVM Configuration Bits Erase Command	Digital Input	High	VDDIO	Permanent Internal pull-down
Reset/Test					
NRST	Synchronous Microcontroller Reset	Digital I/O	Low	VDDIO	Permanent Internal pull-up
TST	Test Select	Digital Input	–	VDDBU	Permanent Internal pull-down
Universal Asynchronous Receiver Transceiver - UARTx					
URXDx	UART Receive Data	Digital/ Analog Input	–	VDDIO	Analog mode for optical receiver
UTXDx	UART Transmit Data	Digital Output	–		–
PIO Controller - PIOA - PIOB - PIOC					
PA0–PA31	Parallel IO Controller A	Digital I/O	–	VDDIO	–
PB0–PB21	Parallel IO Controller B		–		–
PC0–PC9	Parallel IO Controller C		–		–
External Bus Interface - EBI					
D[7:0]	Data Bus	Digital I/O	–	VDDIO	–
A[23:0]	Address Bus	Digital Output	–		–
Static Memory Controller - SMC					
NCS0–NCS3	Chip Select Lines	Digital Output	Low	VDDIO	–
NRD	Read Signal				–
NWE	Write Enable				–
NBS0–NBS1	Byte Mask Signal				–
NWR0–NWR1	Write Signal				–

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Universal Synchronous Asynchronous Receiver Transmitter - USARTx					
SCKx	USARTx Serial Clock	Digital I/O	–	VDDIO	–
TXDx	USARTx Transmit Data	Digital Output	–		–
RXDx	USARTx Receive Data	Digital Input	–		–
RTSx	USARTx Request To Send	Digital Output	–		–
CTSx	USARTx Clear To Send	Digital Input	–		–
Timer/Counter - TC					
TCLKx	TC Channel x External Clock Input	Digital Input	–	VDDIO	–
TIOAx	TC Channel x I/O Line A	Digital I/O	–		–
TIOBx	TC Channel x I/O Line B		–		–
Pulse Width Modulation Controller - PWMC					
PWMx	PWM Waveform Output for channel x	Digital Output	–	VDDIO	–
Serial Peripheral Interface - SPI					
SPI0_MISO	Master In Slave Out	Digital Input	–	VDDIO	–
SPI0_MOSI	Master Out Slave In	Digital Output	–		–
SPCK0	SPI Serial Clock		–		–
SPI0_NPCS0	SPI Peripheral Chip Select 0		Low		NPCS0 is also NSS for Slave mode
SPI0_NPCS1–SPI0_NPCS3	SPI Peripheral Chip Select	Output	Low		–
Segmented LCD Controller - SLCDC					
COM0–COM5	Common Terminals	Output	–	VDDIO	–
SEG0–SEG39	Segment Terminals		–		–
Two-wire Interface - TWI					
TWDx	TWIx Two-wire Serial Data	Digital I/O	–	VDDIO	–
TWCKx	TWIx Two-wire Serial Clock	Digital Output	–		–
Analog					
ADVREF	External Voltage Reference for ADC	Analog Input	–	VDDIN	–

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
10-bit Analog-to-Digital Converter - ADC					
AD0–AD3	Analog Inputs	Analog, Digital	–	VDDIO	ADC input range limited to [0..ADVREF]
Fast Flash Programming Interface - FFPI					
PGMEN0–PGMEN1	Programming Enabling	Digital Input	–	VDDIO	–
PGMM0–PGMM3	Programming Mode		–		–
PGMD0–PGMD15	Programming Data	Digital I/O	–		–
PGMRDY	Programming Ready	Digital Output	High		–
PGMNVALID	Data Direction		Low		–
PGMNOE	Programming Read	Digital Input	Low		–
PGMNCMD	Programming Command				–
Energy Metering Analog Front End - EMAFE					
VREF_AFE	Precision 1.2V Voltage Reference Input and Output for EMAFE	Analog Input / Output	–	VDDA	–
VPx	Voltage Channel x, Positive Input	Analog Input	–		–
VN	Voltage Channels, Common Negative Input		–		–
IPx	Current Channel x, Positive Input		–		–
INx	Current Channel x, Negative Input		–		–

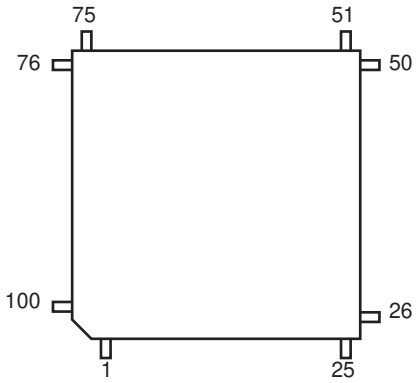
4. Package and Pinout

4.1 100-lead LQFP Package Outline

The 100-lead LQFP package has a 0.5 mm ball pitch and respects Green standards.

Figure 4-1 shows the orientation of the 100-lead LQFP package. Refer to Figure 47-1 “100-lead LQFP Package Drawing”.

Figure 4-1. Orientation of the 100-lead LQFP Package



4.2 100-lead LQFP Pinout

Table 4-1. SAM4CMP32C/16C/8C 100-lead LQFP Pinout

1	PB6	26	TDI/PB0	51	VDDIO	76	ADVREF
2	PB7	27	TCK/SWCLK/PB3	52	GND	77	GND
3	IN2	28	TMS/SWDIO/PB2	53	PA31	78	PB13/AD3
4	GND	29	ERASE/PC9	54	GND	79	PA5/AD2/PGMRDY
5	IP2	30	TDO/TRACESWO /PB1	55	VDDPLL	80	PA4/AD1/PGMNCMD
6	PB8	31	PC1	56	PA28	81	PA12/AD0/PGMD0
7	IN1	32	PC6	57	PA27/PGMD15	82	VDDIN
8	IP1	33	VDDIO	58	PA6/PGMNOE	83	VDDOUT
9	IN0	34	VDDBU	59	VDDCORE	84	VP3
10	IP0	35	FWUP	60	PA3	85	VP2
11	GND	36	JTAGSEL	61	PA21/PGMD9	86	VDDCORE
12	VDDCORE	37	SHDN	62	PA22/PGMD10	87	VP1
13	PB9	38	TST	63	VDDIO	88	PA0/PGMEN0
14	PB10	39	WKP0/TMP0	64	VDDIN_AFE	89	VN
15	PB11	40	XIN32	65	–	90	VREF_AFE
16	PB12	41	XOUT32	66	PA23/PGMD11	91	GNDREF
17	PB14	42	GND	67	PA9/PGMM1	92	VDDLCD
18	PB15	43	PB4	68	PA10/PGMM2	93	GNDA
19	PA26/PGMD14	44	VDDCORE	69	PA11/PGMM3	94	VDDA
20	PA25/PGMD13	45	PB5	70	PA13/PGMD1	95	IN3
21	PA24/PGMD12	46	PC7	71	PA14/PGMD2	96	PA1/PGMEN1
22	PA20/PGMD8	47	PC0	72	PA15/PGMD3	97	IP3
23	PA19/PGMD7	48	NRST	73	PA16/PGMD4	98	PA7/PGMNVALID
24	PA18/PGMD6	49	VDDIO	74	PA17/PGMD5	99	VDDIO
25	PA8/PGMM0	50	PA30	75	VDDIO	100	PA2

Table 4-2. SAM4CMS32C/16C/8C/4C 100-lead LQFP Pinout

1	PB6	26	TDI/PB0	51	VDDIO	76	ADVREF
2	PB7	27	TCK/SWCLK/PB3	52	GND	77	GND
3	PB18	28	TMS/SWDIO/PB2	53	PA31	78	PB13/AD3
4	GND	29	ERASE/PC9	54	GND	79	PA5/AD2/PGMRDY
5	PB19	30	TDO/TRACESWO /PB1	55	VDDPLL	80	PA4/AD1/PGMNCMD
6	PB8	31	PC1	56	PA28	81	PA12/AD0/PGMD0
7	IN1	32	PC6	57	PA27/PGMD15	82	VDDIN
8	IP1	33	VDDIO	58	PA6/PGMNOE	83	VDDOUT
9	IN0	34	VDDBU	59	VDDCORE	84	PB21
10	IP0	35	FWUP	60	PA3	85	VP2
11	GND	36	JTAGSEL	61	PA21/PGMD9	86	VDDCORE
12	VDDCORE	37	SDHN	62	PA22/PGMD10	87	VP1
13	PB9	38	TST	63	VDDIO	88	PA0/PGMEN0
14	PB10	39	WKUP0/TMP0	64	VDDIN_AFE	89	VN
15	PB11	40	XIN32	65	–	90	VREF_AFE
16	PB12	41	XOUT32	66	PA23/PGMD11	91	GNDREF
17	PB14	42	GND	67	PA9/PGMM1	92	VDDLCD
18	PB15	43	PB4	68	PA10/PGMM2	93	GNDA
19	PA26/PGMD14	44	VDDCORE	69	PA11/PGMM3	94	VDDA
20	PA25/PGMD13	45	PB5	70	PA13/PGMD1	95	PB16/TMP1
21	PA24/PGMD12	46	PC7	71	PA14/PGMD2	96	PA1/PGMEN1
22	PA20/PGMD8	47	PC0	72	PA15/PGMD3	97	PB17
23	PA19/PGMD7	48	NRST	73	PA16/PGMD4	98	PA7/PGMNVALID
24	PA18/PGMD6	49	VDDIO	74	PA17/PGMD5	99	VDDIO
25	PA8/PGMM0	50	PA30	75	VDDIO	100	PA2

5. Power Supply and Power Control

5.1 Power Supplies

The SAM4CM has several types of power supply pins. In most cases, a single supply scheme for all power supplies (except VDDBU) is possible. Figure 5-1 shows power domains according to the different power supply pins.

Figure 5-1. Power Domains

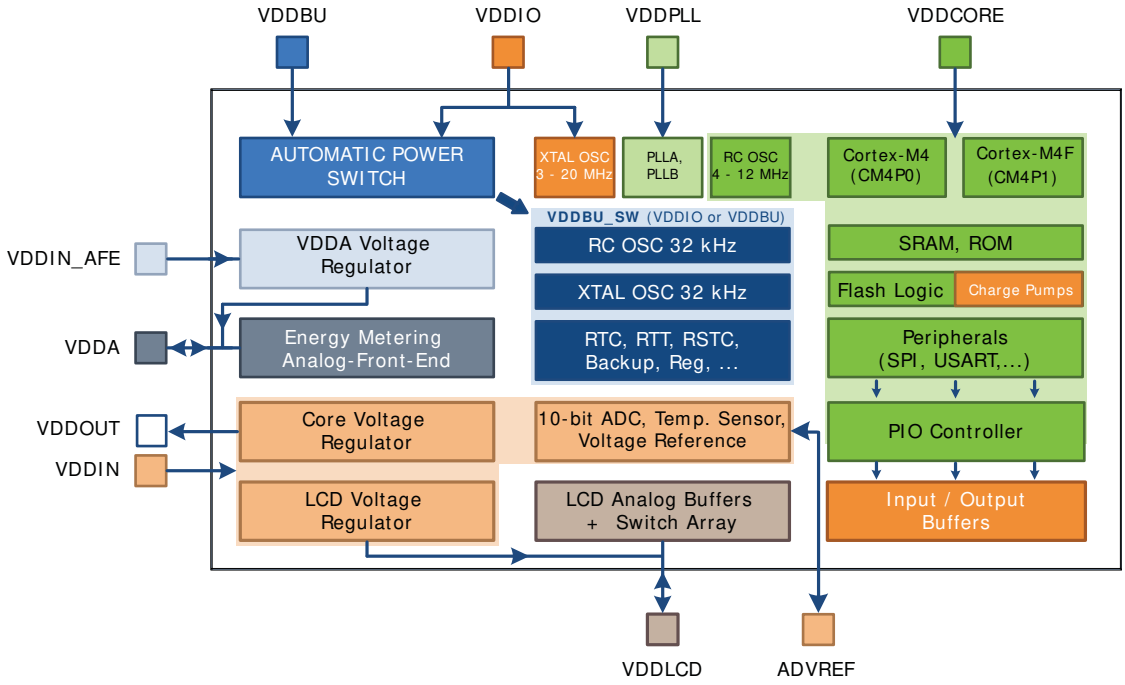


Table 5-1. Power Supply Voltage Ranges[1]

Power Supply	Range	Comments
VDDIO	1.6V to 3.6V	Flash memory charge pumps supply for erase and program operations, and read operation. Input/Output buffers supply. EMAFE digital functions supply. Restrictions on range may apply. Refer to Section 46. "Electrical Characteristics".
VDDBU[2]	1.6V to 3.6V	Backup area power supply. VDDBU is automatically disconnected when VDDIO is present (> 1.9V).
VDDIN	1.6V to 3.6V	Core voltage regulator supply, LCD voltage regulator supply, ADC and programmable voltage reference supply. Restrictions on range may apply. Refer to Section 46. "Electrical Characteristics".
VDDLCD	2.5V to 3.6V	LCD voltage regulator output. External LCD power supply input (LCD regulator not used). VDDIO/VDDIN must be supplied when the LCD Controller is used.

Table 5-1. Power Supply Voltage Ranges[1] (Continued)

Power Supply	Range	Comments
VDDPLL	1.08V to 1.32V	PLLA and PLLB supply.
VDDCORE	1.08V to 1.32V	Core logic, processors, memories and analog peripherals supply.
VDDIN_AFE	3.00V to 3.60V	EMAFE regulator input.
VDDA	2.70 to 2.90V	EMAFE regulator output (2.8V). EMAFE analog functions power supply input.

Notes: 1. In all power modes except Backup mode, all power supply inputs must be powered.
2. VDDBU must be powered from an external source to ensure proper start-up. The external source must meet the timing and voltage level requirements described in Section 46.2.2 “Recommended Power Supply Conditions at Powerup”.

5.1.1 Core Voltage Regulator

The core voltage regulator is managed by the Supply Controller.

It features two operating modes:

- In Normal mode, the quiescent current of the voltage regulator is less than 500 µA when sourcing maximum load current, i.e. 120 mA. Internal adaptive biasing adjusts the regulator quiescent current depending on the required load current. In Wait Mode, quiescent current is only 5 µA.
- In Backup mode, the voltage regulator consumes less than 100 nA while its output (VDDOUT) is driven internally to GND.

The default output voltage is 1.20V and the start-up time to reach Normal mode is less than 500 µs.

For further information, refer to Table 46-16 “Core Voltage Regulator Characteristics”.

5.1.2 LCD Voltage Regulator

The SAM4CM embeds an adjustable LCD voltage regulator that is managed by the Supply Controller.

This internal regulator is designed to supply the Segment LCD outputs. The LCD regulator output voltage is software selectable with 16 levels to adjust the display contrast.

If not used, its output (VDDLCD) can be bypassed (Hi-z mode) and an external power supply can be provided onto the VDDLCD pin. In this case, VDDIO still needs to be supplied.

The LCD voltage regulator can be used in all power modes (Backup, Wait, Sleep and Active).

For further information, refer to Table 46-18 “LCD Voltage Regulator Characteristics”.

5.1.3 Automatic Power Switch

The SAM4CM features an automatic power switch between VDDBU and VDDIO. When VDDIO is present, the backup zone power supply is powered by VDDIO and current consumption on VDDBU is about zero (around 100 nA, typ.). When VDDIO is removed, the backup area of the device is supplied from VDDBU. Switching between VDDIO and VDDBU is transparent to the user.

5.1.4 EMAFE Voltage Regulator

The SAM4CM series embeds a 2.8V voltage regulator to supply its Energy Metering Analog Front-End (the VDDA pin). This regulator is under software control. When the EMAFE voltage regulator is turned off, its output stage is placed in High-impedance mode and thus can be forced by an external voltage source.

5.1.5 Typical Powering Schematics

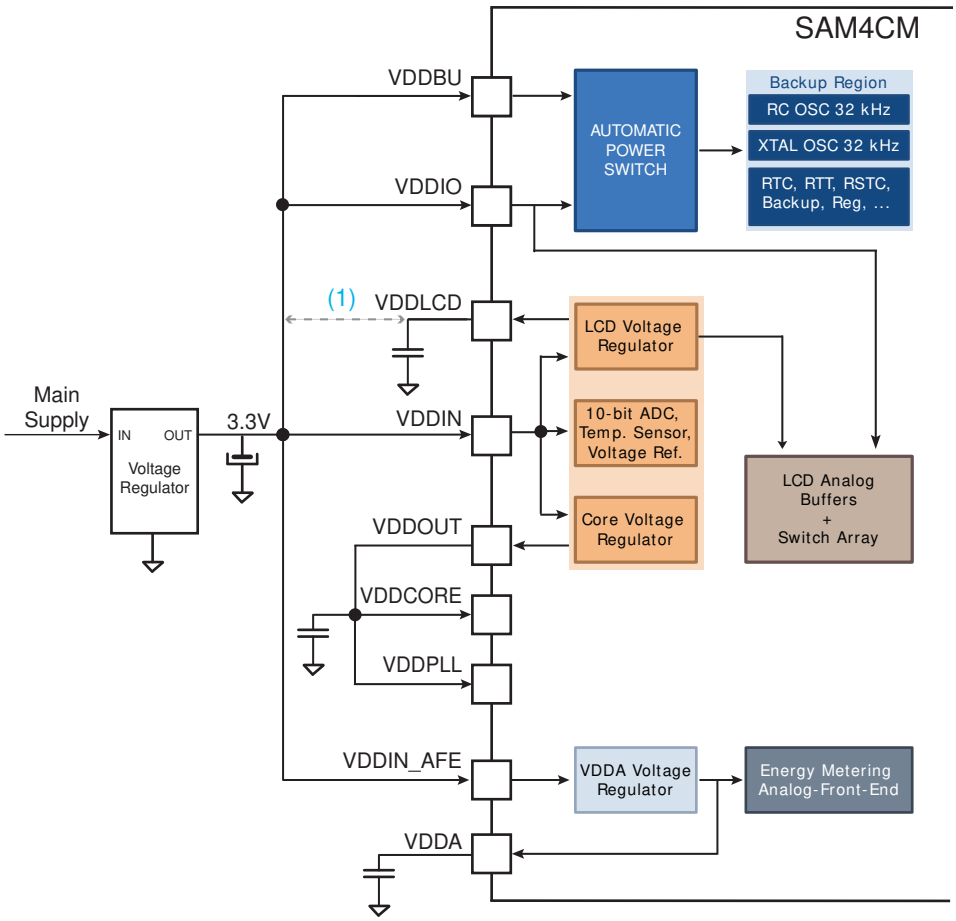
The SAM4CM series supports 1.6V to 3.6V single-supply operation. Restrictions on this range may apply depending on enabled features. Refer to Section 46. “Electrical Characteristics”.

Note: Figure 5-2, Figure 5-3 and Figure 5-4 show simplified schematics of the power section.

5.1.5.1 Single Supply Operation

Figure 5-2 below shows a typical power supply scheme with a single power source. VDDIO, VDDIN, VDDIN_AFE and VDDBU are derived from the main power source (typically a 3.3V regulator output) while VDDCORE, VDDPLL, VDDLCD, and VDDA are fed by the embedded regulator outputs.

Figure 5-2. Single Supply Operation

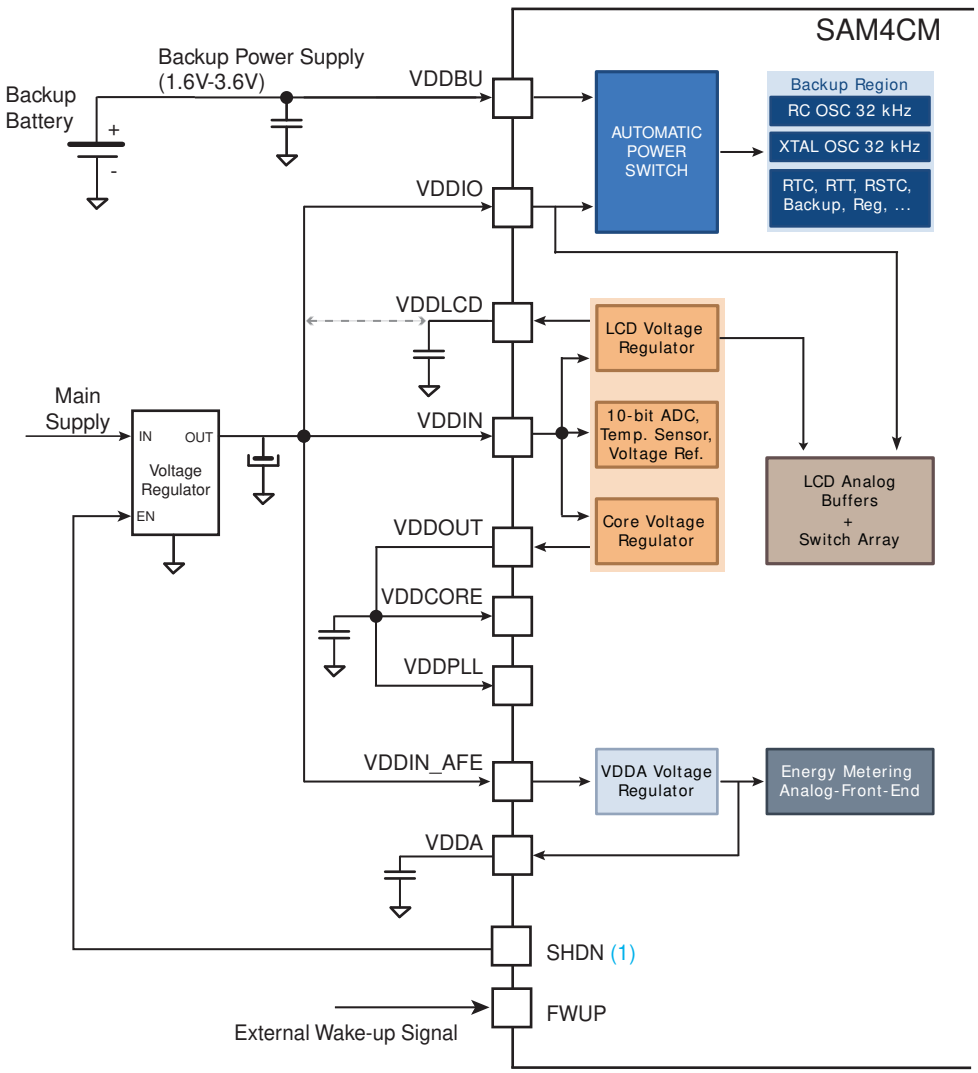


Note: 1. Internal LCD Voltage Regulator can be disabled to save its operating current. VDDLCD must then be provided externally.

5.1.5.2 Single Supply Operation with Backup Battery

Figure 5-3 shows the single-supply operation schematic from Figure 5-2, improved by adding a backup capability. VDDBU is supplied with a separate backup battery while VDDIO, VDDIN and VDDIN_AFE are still connected to the main power source. Note that the TMP1 and RTCOUT0 pins cannot be used in Backup mode as they are referred to VDDIO, which is not powered in this application case. To keep using these pins in Backup mode, VDDIO must be maintained.

Figure 5-3. Single Supply Operation with Backup Battery



Note: 1. Example with the SHDN pin used to control the main regulator enable pin. SHDN defaults to VDDBU at startup and when the device wakes up from a wake-up event (external pin, RTC alarm, etc.). When the device is in Backup mode, SHDN defaults to 0.

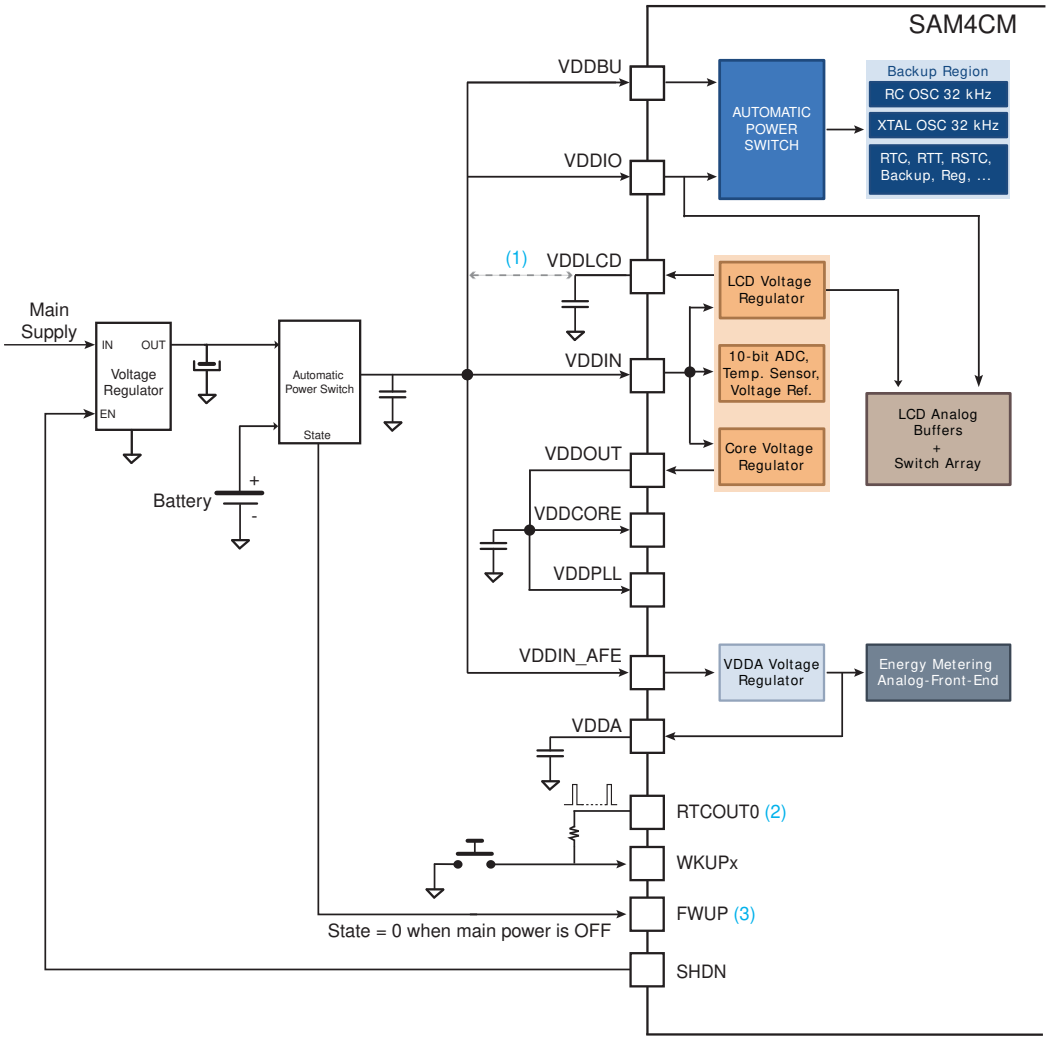
5.1.5.3 Single Power Supply using One Main Battery and LCD Controller in Backup Mode

Figure 5-4 below shows a typical power supply scheme that maintains VDDBU, VDDIO, and VDDLCD when entering Backup mode. This is useful to enable the display and/or some supplementary wake-up sources in Backup mode when the main voltage is not present.

In this power supply scheme, the SAM4CM can wake up both from an internal wake-up source, such as RTT, RTC and VDDIO Supply Monitor, and from an external source, such as generic wake-up pins (WKUPx), anti-tamper inputs (TMP0/1) or force wake-up (FWUP).

Note: The VDDIO supply monitor only wakes up the device from Backup mode on a negative-going VDDIO supply (as system alert). As a result, the supply monitor cannot be used to wake up the device when the VDDIO supply is rising at power cycle. Refer to Section 20. "Supply Controller (SUPC)" for more information on the VDDIO supply monitor.

Figure 5-4. Single Power Supply using Battery and LCD Controller in Backup Mode



Notes:
1. Internal LCD Voltage Regulator can be disabled to save its operating current. VDDLCD must then be provided externally.
2. RTCOUT0 signal is used to make a dynamic wake-up. WKUPx pin is pulled-up with a low duty cycle to avoid battery discharge by permanent activation of the switch.
3. The State output of the automatic power switch indicates to the device that the main power is back and forces its wake-up.

5.1.5.4 Wake-up, Anti-tamper and RTCOUT0 Pins

In all power supply figures shown above, if generic wake-up pins other than WKUP0/TMP0 are used either as a wake-up or a fast startup input, or as anti-tamper inputs, VDDIO must be present. This also applies to the RTCOUT0 pin.

5.1.5.5 General-purpose IO (GPIO) State in Low-power Modes

In dual-power supply schemes shown in Figure 5-3 and Figure 5-4, where Backup or Wait mode must be used, configuration of the GPIO lines is maintained in the same state as before entering Backup or Wait mode. Thus, to avoid extra current consumption on the VDDIO power rail, the user must configure the GPIOs either as an input with pull-up or pull-down enabled, or as an output with low or high level to comply with external components.

5.1.5.6 Default General-purpose IOs (GPIO) State after Reset

The reset state of the GPIO lines after reset is given in Table 11-5 “Multiplexing on PIO Controller A (PIOA)”, Section 11-6 “Multiplexing on PIO Controller B (PIOB)” and Table 11-7 “Multiplexing on PIO Controller C (PIOC)”. For further details about the GPIO and system lines, wake-up sources and wake-up time, and typical power consumption in different low-power modes, refer to Table 5-2 “Low-power Mode Configuration Summary”.

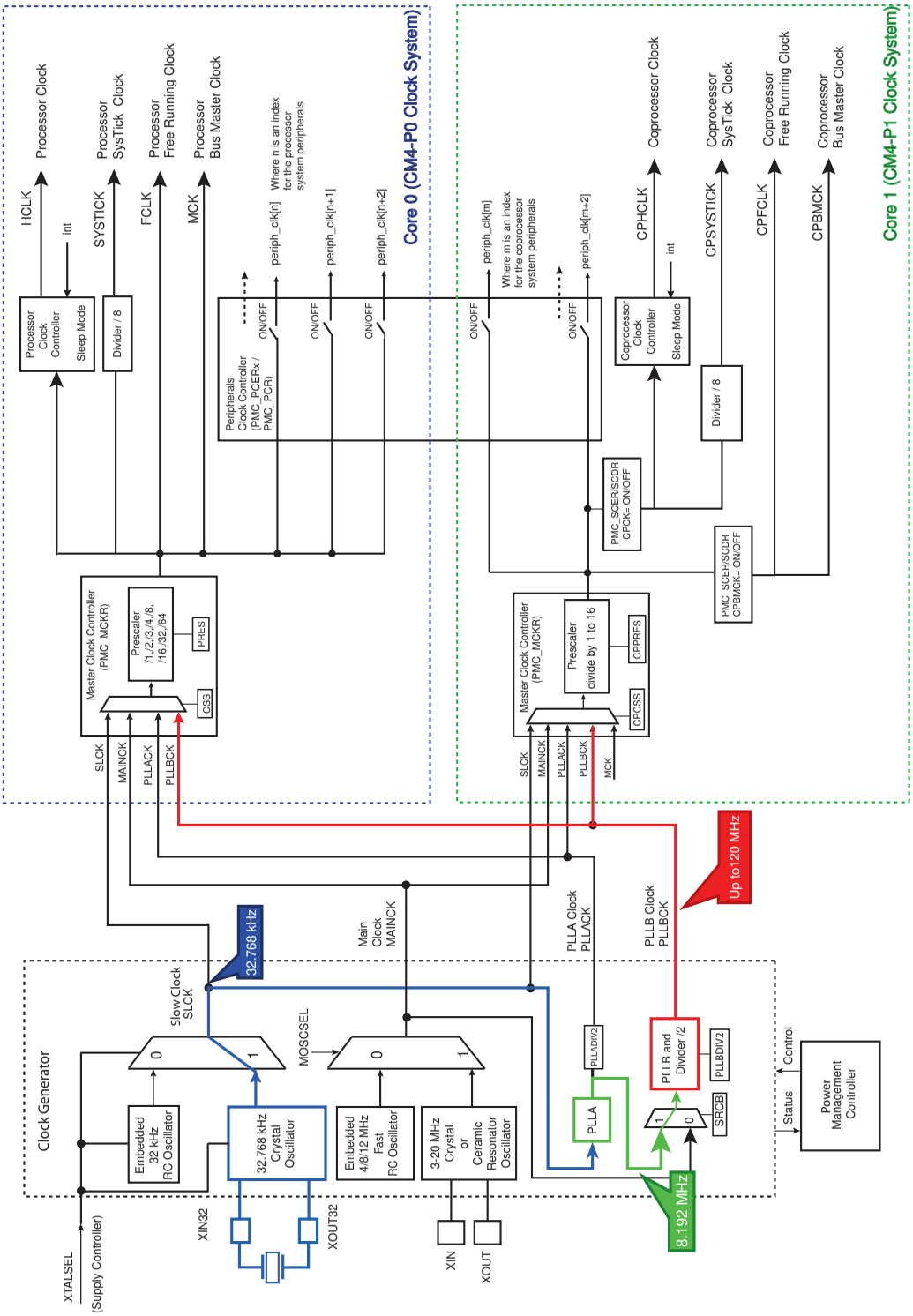
5.2 Clock System Overview

Figure 5-5 illustrates the typical operation of the whole SAM4CM clock system in case of single crystal (32.768 kHz) applications. Note:

- The 32 kHz crystal oscillator can be the source clock of the 8 MHz digital PLL (PLLA).
- The 8 MHz clock can feed the high frequency PLL (PLLB) input.
- The output of the PLLB can be used as a main clock for both cores and the peripherals.

Full details of the clock system are provided in Section 29. “Clock Generator” and Section 30. “Power Management Controller (PMC)”.

Figure 5-5. Global Clock System



5.3 System State at Power-up

5.3.1 Device Configuration after the First Power-up

At the first power-up, the SAM4CM boots from the ROM. The device configuration is defined by the SAM-BA boot program.

5.3.2 Device Configuration after a Power Cycle when Booting from Flash Memory

After a power cycle of all the power supply rails, the system peripherals, such as the Flash Controller, the Clock Generator, the Power Management Controller and the Supply Controller, are in the following states:

- Slow Clock (SLCK) source is the internal 32 kHz RC Oscillator (32 kHz crystal oscillator is disabled)
- Main Clock (MAINCK) source is set to the 4 MHz internal RC Oscillator
- 3–20 MHz crystal oscillator and PLLs are disabled
- Core Brownout Detector and Core Reset are enabled
- Backup Power-on-reset is enabled
- VDDIO Supply Monitor is disabled
- Flash Wait State (FWS) bit in the EEFC Flash Mode Register is set to 0
- Core 0 Cache Controller (CMCC0) is enabled (only used if the application link address for the Core 0 is 0x11000000)
- Sub-system 1 is in the reset state and not clocked

5.3.3 Device Configuration after a Reset

After a reset or a wake-up from Backup mode, the following system peripherals default to the same state as after a power cycle:

- Main Clock (MAINCK) source is set to the 4 MHz internal RC oscillator
- 3–20 MHz crystal oscillator and PLLs are disabled
- Flash Wait State (FWS) bit in the EEFC Flash Mode Register is set to 0
- Core 0 Cache Controller (CMCC0) is enabled (only used if the application link address for the Core 0 is 0x11000000)
- Sub-system 1 is in the reset state and not clocked

The states of the other peripherals are saved in the backup area managed by the Supply Controller as long as VDDBU is maintained during device reset:

- Slow Clock (SLCK) source selection is written in SUPC_ CR.XTALSEL.
- Core Brownout Detector enable/disable is written in SUPC_MR.BODDIS.
- Backup Power-on-reset enable/disable is written in the SUPC_MR.BUPPOREN.
- VDDIO Supply Monitor mode is written in the SUPC_SMMR.

5.4 Active Mode

Active mode is the normal running mode, with the single core or the dual cores executing code. The system clock can be the fast RC oscillator, the main crystal oscillator or the PLLs. The Power Management Controller (PMC) can be used to adapt the frequency and to disable the peripheral clocks when unused.

5.5 Low-power Modes

The various low-power modes (Backup, Wait and Sleep modes) of the SAM4CM are described below. Note that the Segmented LCD Controller can be used in all low-power modes.

Note: The Wait For Event instruction (WFE) of the Cortex-M4 core can be used to enter any of the low-power modes, however this may add complexity to the design of application state machines. This is due to the fact that the WFE instruction is associated with an event flag of the Cortex core that cannot be managed by the software application. The event flag can be set by interrupts, a debug event or an event signal from another processor. When an event occurs just before WFE execution, the processor takes it into account and does not enter Low-power mode. Atmel has made provision to avoid using the WFE instruction. The workarounds to ease application design, including the use of the WFE instruction, are given in the following description of the low-power mode sequences.

5.5.1 Backup Mode

The purpose of Backup mode is to achieve the lowest possible power consumption in a system that executes periodic wake-ups to perform tasks but which does not require fast start-up time. The total current consumption is 0.5 µA typical on VDDBU.

The Supply Controller, power-on reset, RTT, RTC, backup registers and the 32 kHz oscillator (RC or crystal oscillator selected by software in the Supply Controller) are running. The regulator and the core supplies are off. The power-on-reset on VDDBU can be deactivated by software.

Wake-up from Backup mode can be done through the Force Wake-up (FWUP) pin, WKUP0, WKUP1 to WKUP12 pins, the VDDIO Supply Monitor (SM) if VDDIO is supplied, or through an RTT or RTC wake-up event. Wake-up pins multiplexed with anti-tampering functions are additional possible sources of a wake-up if an anti-tampering event is detected. The TMP0 pad is supplied by the backup power supply (VDDBU). TMP1 is supplied by VDDIO.

The LCD Controller can be used in Backup mode. The purpose is to maintain the displayed message on the LCD display after entering Backup mode. The current consumption on VDDIN to maintain the LCD is 10 µA typical. Refer to Section 46. “Electrical Characteristics”.

In case the VDDIO power supply is maintained with VDDBU when entering Backup mode, it is up to the application to configure all PIO lines in a stable and known state to avoid extra power consumption or possible current path with the input/output lines of the external on-board devices.

5.5.1.1 Entering and Exiting Backup Mode

To enter Backup mode, follow the steps in the sequence below:

1. Depending on the application, set the PIO lines in the correct mode and configuration (input pull-up or pull-down, output low or high levels).
2. Disable the Main Crystal Oscillator (enabled by SAM-BA boot if the device is booting from ROM).
3. Configure PA30/PA31 (XIN/XOUT) into PIO mode depending on their use.
4. Disable the JTAG lines using the SFR1 register in Matrix 0 (by default, internal pull-up or pull-down is disabled on JTAG lines).
5. Enable the RTT in 1 Hz mode.
6. Disable Normal mode of the RTT (RTT will run in 1 Hz mode).
7. To reduce power consumption, disable the POR backup if not needed.

Note: The POR BU provides critical functionality to ensure the MCU backup logic will be properly reset in the event VDDBU drops below the minimum specification. If this protection is not necessary, the backup POR may be disabled to reduce power consumption.

8. Disable the Core brownout detector.

9. Select one of the following methods to complete the sequence:
    a. To enter Backup mode using the VROFF bit:
        - Write a 1 to the VROFF bit of SUPC_CR.
    b. To enter Backup mode using the WFE instruction:
        - Write a 1 to the SLEEPDEEP bit of the Cortex-M4 processor.
        - Execute the WFE instruction of the processor.

After this step, the core voltage regulator is shut down and the SHDN pin goes low. The digital internal logic (cores, peripherals and memories) is not powered. The LCD controller can be enabled if needed before entering Backup mode.

Whether the VROFF bit or the WFE instruction was used to enter Backup mode, the system exits Backup mode if one of the following enabled wake-up events occurs:

- WKUP[0–13] pins
- Force Wake-up pin
- VDDIO Supply Monitor (if VDDIO is present, and VDDIO supply falling)
- Anti-tamper event detection
- RTC alarm
- RTT alarm

After exiting Backup mode, the device is in the reset state. Only the configuration of the backup area peripherals remains unchanged.

Note that the device does not automatically enter Backup mode if VDDIN is disconnected, or if it falls below minimum voltage. The Shutdown pin (SHDN) remains high in this case.

For current consumption in Backup mode, refer to Section 46. “Electrical Characteristics”.

5.5.2 Wait Mode

The purpose of Wait mode is to achieve very low power consumption while maintaining the whole device in a powered state for a start-up time of a few µs. For current consumption in Wait mode, refer to Section 46. “Electrical Characteristics”.

In Wait mode, the bus and peripheral clocks of Sub-system 0 and Sub-system 1 (MCK/CPBMCK), the clocks of Core 0 and Core 1 (HCLK/CPHCLK) are stopped when Wait mode is entered (refer to Section 5.5.2.1 “Entering and Exiting Wait Mode”). However, the power supply of core, peripherals and memories are maintained using Standby mode of the core voltage regulator.

The SAM4CM is able to handle external and internal events in order to perform a wake-up. This is done by configuring the external WKUPx lines as fast startup wake-up pins (refer to Section 5.7 “Fast Start-up”). RTC alarm, RTT alarm and anti-tamper events can also wake up the device.

Wait mode can be used together with Flash in Read-Idle mode, Standby mode or Deep Power-down mode to further reduce the current consumption. Flash in Read-Idle mode provides a faster start-up; Standby mode offers lower power consumption.

5.5.2.1 Entering and Exiting Wait Mode

1. Stop Sub-system 1.
2. Select the 4/8/12 MHz fast RC Oscillator as Main Clock(1).
3. Disable the PLL if enabled.
4. Clear the internal wake-up sources.
5. Depending on the application, set the PIO lines in the correct mode and configuration (input pull-up or pull-down, output low or high level).
6. Disable the Main Crystal Oscillator (enabled by SAM-BA boot if device is booting from ROM).

7. Configure PA30/PA31 (XIN/XOUT) into PIO mode according to their use.
8. Disable the JTAG lines using the SFR1 register in Matrix 0 (by default, internal pull-up or pull-down is disabled on JTAG lines).
9. Set the FLPM field in the PMC Fast Startup Mode Register (PMC_FSMR)[(2)].
10. Set the Flash Wait State (FWS) bit in the EEFC Flash Mode Register to 0.
11. Select one of the following methods to complete the sequence:
    a. To enter Wait mode using the WAITMODE bit:
        - Set the WAITMODE bit to 1 in the PMC Main Oscillator Register (CKGR_MOR).
        - Wait for Master Clock Ready MCKRDY = 1 in the PMC Status Register (PMC_SR).
    b. To enter Wait mode using the WFE instruction:
        - Select the 4/8/12 MHz fast RC Oscillator as Main Clock.
        - Set the FLPM field in the PMC Fast Startup Mode Register (PMC_FSMR).
        - Set Flash Wait State at 0.
        - Set the LPM bit in the PMC Fast Startup Mode Register (PMC_FSMR).
        - Write a 0 to the SLEEPDEEP bit of the Cortex-M4 processor.
        - Execute the Wait-For-Event (WFE) instruction of the processor.

Notes:
1. Any frequency can be chosen. The 12 MHz frequency will provide a faster start-up compared to the 4 MHz, but with the increased current consumption (in the µA range). Refer to Section 46. “Electrical Characteristics”.
2. Depending on the Flash Low-power Mode (FLPM) value, the Flash enters three different modes:
    - If FLPM = 0, the Flash enters Stand-by mode (Low consumption)
    - If FLPM = 1, the Flash enters Deep Power-down mode (Extra low consumption)
    - If FLPM = 2, the Flash enters Idle mode. Memory is ready for Read access

Whether the WAITMODE bit or the WFE instruction was used to enter Wait mode, the system exits Wait mode if one of the following enabled wake-up events occurs:

- WKUP[0–13] pins in Fast wake-up mode
- Anti-tamper event detection
- RTC alarm
- RTT alarm

After exiting Wait mode, the PIO controller has the same configuration state as before entering Wait mode. The SAM4CM is clocked back to the RC oscillator frequency which was used before entering Wait mode. The core will start fetching from Flash at this frequency. Depending on the configuration of the Flash Low-power Mode (FLPM) bits used to enter Wait mode, the application has to reconfigure it back to Read-idle mode.

5.5.3 Sleep Mode

The purpose of Sleep mode is to optimize power consumption of the device versus response time. In this mode, only the core clocks of CM4P0 and/or CM4P1 are stopped. Some of the peripheral clocks can be enabled depending on the application needs. The current consumption in this mode is application dependent. This mode is entered using Wait for Interrupt (WFI) or Wait for Event (WFE) instructions of the Cortex-M4.

The processor can be awakened from an interrupt if the WFI instruction of the Cortex-M4 is used to enter Sleep mode, or from a wake-up event if the WFE instruction is used. The WFI instruction can also be used to enter Sleep mode with the SLEEPONEXIT bit set to 1 in the System Control Register (SCB_SCR) of the Cortex-M. If the SLEEPONEXIT bit of the SCB_SCR is set to 1, when the processor completes the execution of an exception handler, it returns to Thread mode and immediately enters Sleep mode. This mechanism can be used in applications that require the processor to run only when an exception occurs. Setting the SLEEPONEXIT bit to 1 enables an interrupt-driven application in order to avoid returning to an empty main application.

5.5.4 Low-power Mode Summary Table

The modes detailed above are the main low-power modes. Table 5-2 below provides a configuration summary of the low-power modes. For more information on power consumption, refer to Section 46. “Electrical Characteristics”.

Table 5-2. Low-power Mode Configuration Summary

Mode	SUPC, 32 kHz Oscillator RTC, RTT Backup Registers POR (Backup Region)	Core Regulator / LCD Regulator	Core 0/1 Memory Peripherals	Potential Wake-up Sources	Core at Wake-up	PIO State in Low-power Mode	PIO State at Wake-up	Typical Wake-up Time(1)
Backup Mode	ON	OFF/OFF	OFF / OFF (Not powered)	- FWUP pin - WKUP0-13 pins(5) - Supply Monitor - Anti-tamper inputs(5) - RTC or RTT alarm	Reset	Previous state saved	Reset state(7)	< 1.5 ms
Backup Mode with LCD	ON	OFF/ON	OFF / OFF (Not powered)	- FWUP pin - WKUP0-13 pins(5) - Supply Monitor - Anti-tamper inputs(5) - RTC or RTT alarm	Reset	Previous state saved	Unchanged (LCD Pins)/ Inputs with pull ups	< 1.5 ms
Wait Mode Flash in Standby Mode(6)	ON	ON/(4)	Core 0 and 1, memories and peripherals: Powered, but Not clocked	Any event from: - Fast start-up through WKUP0-13 pins - Anti-tamper inputs(5) - RTC or RTT alarm	Clocked back	Previous state saved	Unchanged	< 10 µs
Wait Mode Flash in Deep Power-down Mode(6)	ON	ON/(4)	Core 0 and 1, memories and peripherals: Powered, but Not clocked	Any event from: - Fast start-up through WKUP0-13 pins - Anti-tamper inputs(5) - RTC or RTT alarm	Clocked back	Previous state saved	Unchanged	< 75 µs
Sleep Mode	ON	ON/(4)	Core 0 and/or Core 1: Powered (Not clocked)(2)	Entry mode = WFI Any enabled Interrupts; Entry mode = WFE Any enabled event: - Fast start-up through WKUP0-13 pins - Anti-tamper inputs(5) - RTC or RTT alarm	Clocked back	Previous state saved	Unchanged	(3)

Notes:
1. When considering wake-up time, the time required to start the PLL is not taken into account. Once started, the device works from the 4, 8 or 12 MHz fast RC oscillator. The user has to add the PLL start-up time if it is needed in the system. The wake-up time is defined as the time taken for wake-up until the first instruction is fetched.
2. In this mode, the core is supplied and not clocked but some peripherals can be clocked.
3. Depends on MCK frequency.
4. LCD voltage regulator can be OFF if VDDLCD is supplied externally thus saving current consumption of the LCD voltage regulator.