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SAM4E Series

Atmel | SMART ARM-based Flash MCU

DATASHEET

Description

The Atmel® | SMART SAM4E series of Flash microcontrollers is based on the high-performance 32-bit ARM® Cortex®-M4 RISC processor and includes a floating point unit (FPU). It operates at a maximum speed of 120 MHz and features up to 1024 Kbytes of Flash, 2 Kbytes of cache memory and up to 128 Kbytes of SRAM.

The SAM4E offers a rich set of advanced connectivity peripherals including 10/100 Mbps Ethernet MAC supporting IEEE 1588 and dual CAN. With a single-precision FPU, advanced analog features, as well as a full set of timing and control functions, the SAM4E is the ideal solution for industrial automation, home and building control, machine-to-machine communications, automotive aftermarket and energy management applications.

The peripheral set includes a full-speed USB device port with embedded transceiver, a 10/100 Mbps Ethernet MAC supporting IEEE 1588, a high-speed MCI for SDIO/SD/MMC, an external bus interface featuring a static memory controller providing connection to SRAM, PSRAM, NOR Flash, LCD Module and NAND Flash, a parallel I/O capture mode for camera interface, hardware acceleration for AES256, 2 USARTs, 2 UARTs, 2 TWIs, 3 SPIs, as well as a 4-channel PWM, 3 three-channel general-purpose 32-bit timers (with stepper motor and quadrature decoder logic support), a low-power RTC, a low-power RTT, 256-bit General Purpose Backup Registers, 2 Analog Front End interfaces (16-bit ADC, DAC, MUX and PGA), one 12-bit DAC (2-channel) and an analog comparator.

The SAM4E devices have three software-selectable low-power modes: Sleep, Wait and Backup. In Sleep mode, the processor is stopped while all other functions can be kept running. In Wait mode, all clocks and functions are stopped but some peripherals can be configured to wake up the system based on predefined conditions.

The Real-time Event Managment allows peripherals to receive, react to and send events in Active and Sleep modes without processor intervention.

1. Features

- Core
  - ARM Cortex-M4 with 2 Kbytes Cache running at up to 120 MHz[1]
  - Memory Protection Unit (MPU)
  - DSP Instruction
  - Floating Point Unit (FPU)
  - Thumb®-2 Instruction Set
- Memories
  - Up to 1024 Kbytes Embedded Flash
  - 128 Kbytes Embedded SRAM
  - 16 Kbytes ROM with Embedded Boot Loader Routines (UART) and IAP Routines
  - Static Memory Controller (SMC): SRAM, NOR, NAND Support
  - NAND Flash Controller
- System
  - Embedded Voltage Regulator for Single Supply Operation
  - Power-on-Reset (POR), Brown-out Detector (BOD) and Dual Watchdog for Safe Operation
  - Quartz or Ceramic Resonator Oscillators: 3 to 20 MHz Main Power with Failure Detection and Optional Low-power 32.768 kHz for RTC or Device Clock
  - RTC with Gregorian and Persian Calendar Mode, Waveform Generation in Backup mode
  - RTC counter calibration circuitry compensates for 32.768 kHz crystal frequency inaccuracy
  - High Precision 4/8/12 MHz Factory Trimmed Internal RC Oscillator with 4 MHz Default Frequency for Device Startup. In-application Trimming Access for Frequency Adjustment
  - Slow Clock Internal RC Oscillator as Permanent Low-power Mode Device Clock
  - One PLL up to 240 MHz for Device Clock and for USB
  - Temperature Sensor
  - Low-power tamper detection on two inputs, anti-tampering by immediate clear of general-purpose backup registers (GPBR)
  - Up to 2 Peripheral DMA Controllers (PDC) with up to 33 Channels
  - One 4-channel DMA Controller
- Low-power Modes
  - Sleep, Wait and Backup modes, down to 0.9 µA in Backup mode with RTC, RTT, and GPBR
- Peripherals
  - Two USARTs with USART1 (ISO7816, IrDA®, RS-485, SPI, Manchester and Modem Modes)
  - USB 2.0 Device: Full Speed (12 Mbits), 2668 byte FIFO, up to 8 Endpoints. On-chip Transceiver
  - Two 2-wire UARTs
  - Two 2-wire Interfaces (TWI)
  - High-speed Multimedia Card Interface (SDIO/SD Card/MMC)
  - One Master/Slave Serial Peripheral Interface (SPI) with Chip Select Signals
  - Three 3-channel 32-bit Timer/Counter blocks with Capture, Waveform, Compare and PWM Mode. Quadrature Decoder Logic and 2-bit Gray Up/Down Counter for Stepper Motor
  - 32-bit low-power Real-time Timer (RTT) and low-power Real-time Clock (RTC) with calendar and alarm features
  - 256-bit General Purpose Backup Registers (GPBR)
  - One Ethernet MAC (GMAC) 10/100 Mbps in MII mode only with dedicated DMA and Support for IEEE1588, Wake-on-LAN
  - Two CAN Controllers with eight Mailboxes
  - 4-channel 16-bit PWM with Complementary Output, Fault Input, 12-bit Dead Time Generator Counter for Motor Control
  - Real-time Event Management

- Cryptography
  - AES 256-bit Key Algorithm compliant with FIPS Publication 197
- Analog
  - AFE (Analog Front End): 2x16-bit ADC, up to 24-channels, Differential Input Mode, Programmable Gain Stage, Auto Calibration and Automatic Offset Correction
  - One 2-channel 12-bit 1 Msps DAC
  - One Analog Comparator with Flexible Input Selection, Selectable Input Hysteresis
- I/O
  - Up to 117 I/O Lines with External Interrupt Capability (Edge or Level Sensitivity), Debouncing, Glitch Filtering and On-die Series Resistor Termination
  - Bidirectional Pad, Analog I/O, Programmable Pull-up/Pull-down
  - Five 32-bit Parallel Input/Output Controllers, Peripheral DMA Assisted Parallel Capture Mode
- Packages
  - 144-ball LFBGA, 10x10 mm, pitch 0.8 mm
  - 100-ball TFBGA, 9x9 mm, pitch 0.8 mm
  - 144-lead LQFP, 20x20 mm, pitch 0.5 mm
  - 100-lead LQFP, 14x14 mm, pitch 0.5 mm

Note: 1. 120 MHz: -40/+105°C, VDDCORE = 1.2V

1.1 Configuration Summary

The SAM4E series devices differ in memory size, package and features. Table 1-1 summarizes the configurations of the device family.

Table 1-1. Configuration Summary

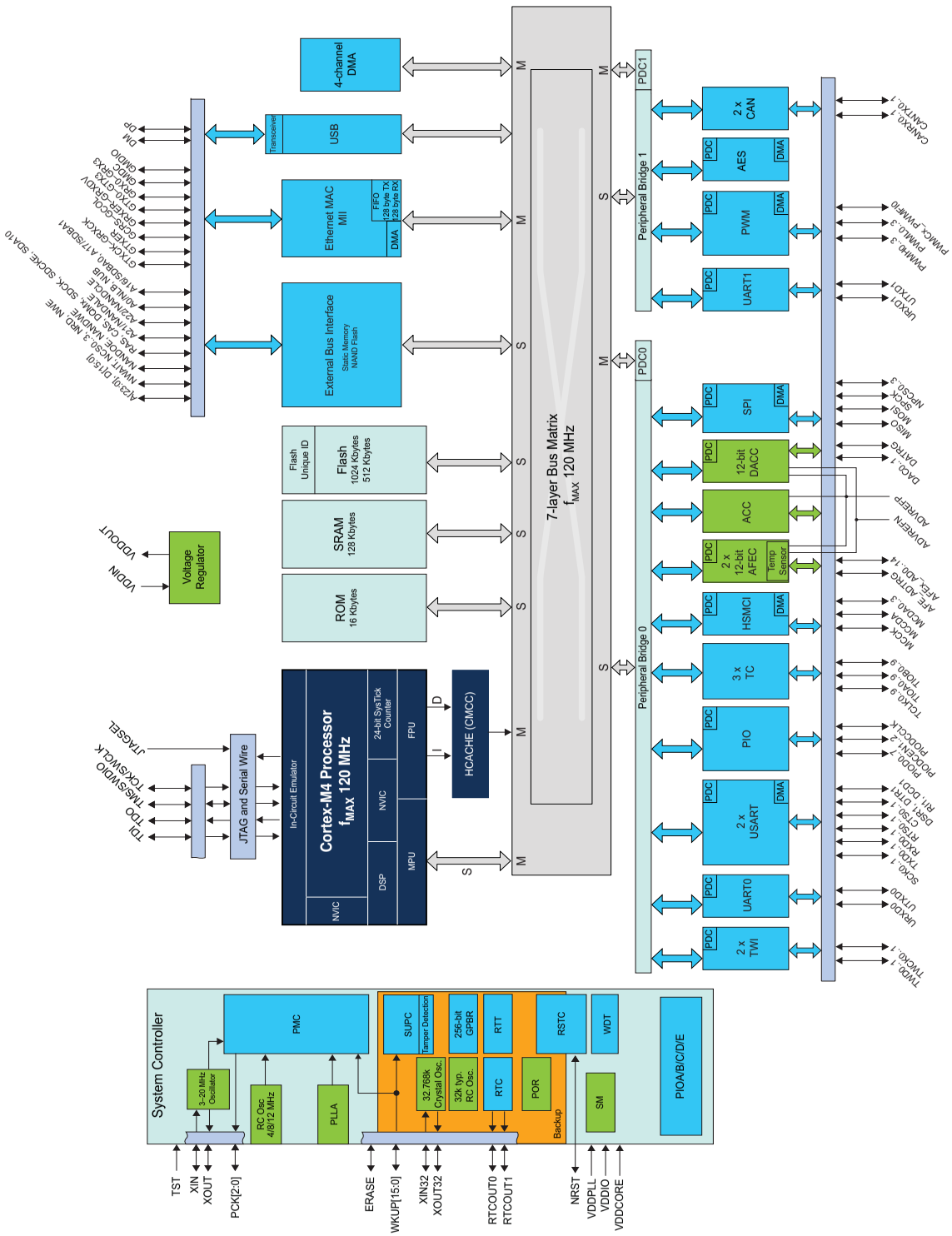
Feature	SAM4E16E	SAM4E8E	SAM4E16C	SAM4E8C
Flash	1024 Kbytes	512 Kbytes	1024 Kbytes	512 Kbytes
SRAM	128 Kbytes		128 Kbytes	
CMCC	2 Kbytes		2 Kbytes	
Package	LFBGA 144 LQFP 144		TFBGA 100 LQFP 100	
Number of PIOs	117		79	
External Bus Interface	8-bit Data, 4 Chip Selects, 24-bit Address		–	
Analog Front End (AFE0\AFE1)	Up to 16 bits(1) 16 ch. / 8 ch. (2)		Up to 16 bits(1) 6 ch. / 4 ch. (3)	
GMAC	10/100 Mbps		10/100 Mbps	
CAN	2		1	
12-bit DAC	2 ch.		2 ch.	
Timer	9(4)		9(5)	
PDC Channels	24 +9		21 +9	
USART/ UART	2/2(6)		2/2(6)	
USB	Full Speed		Full Speed	
HSMCI	1 port, 4 bits		1 port, 4 bits	
TWI	2		2	

Notes:
1. ADC is 12-bit, up to 16 bits with averaging.
   For details, please refer to Section 46. “SAM4E Electrical Characteristics”.
2. AFE0 is 16 channels and AFE1 is 8 channels. The total number of AFE channels is 24.
   One channel is reserved for the internal temperature sensor.
3. AFE0 is 6 channels and AFE1 is 4 channels. The total number of AFE channels is 10.
   One channel is reserved for the internal temperature sensor.
4. Nine TC channels are accessible through PIO.
5. Three TC channels are accessible through PIO and 6 channels are reserved for internal use.
6. Full Modem support on USART1.

2. Block Diagram

See Table 1-1 for detailed configurations of memory size, package and features of the SAM4E devices.

Figure 2-1. SAM4E 144-pin Block Diagram



3. Signal Description

Table 3-1 gives details on signal names classified by peripheral.

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Power Supplies					
VDDIO	Peripherals I/O Lines Power Supply	Power	–	–	1.62V to 3.6V
VDDIN	Voltage Regulator Input, DAC and Analog Comparator Power Supply	Power	–	–	1.62V to 3.6V(1)
VDDOUT	Voltage Regulator Output	Power	–	–	1.2V Output
VDDPLL	Oscillator and PLL Power Supply	Power	–	–	1.08 V to 1.32V
VDDCORE	Power the core, the embedded memories and the peripherals	Power	–	–	1.08V to 1.32V
GND	Ground	Ground	–	–	–
Clocks, Oscillators and PLLs					
XIN	Main Oscillator Input	Input	–	VDDIO	Reset State: - PIO Input - Internal Pull-up disabled - Schmitt Trigger enabled(2)
XOUT	Main Oscillator Output	Output	–		
XIN32	Slow Clock Oscillator Input	Input	–		
XOUT32	Slow Clock Oscillator Output	Output	–		
PCK0–PCK2	Programmable Clock Output	Output	–		Reset State: - PIO Input - Internal Pull-up enabled - Schmitt Trigger enabled(2)
Real-time Clock					
RTCOUT0	Programmable RTC waveform output	Output	–	VDDIO	Reset State: - PIO Input - Internal Pull-up enabled - Schmitt Trigger enabled(2)
RTCOUT1	Programmable RTC waveform output	Output	–		
Serial Wire/JTAG Debug Port - SWJ-DP					
TCK/SWCLK	Test Clock/Serial Wire Clock	Input	–	VDDIO	Reset State: - SWJ-DP Mode - Internal Pull-up disabled(3) - Schmitt Trigger enabled(2)
TDI	Test Data In	Input	–		
TDO/TRACESWO	Test Data Out / Trace Asynchronous Data Out	Output	–		
TMS/SWDIO	Test Mode Select /Serial Wire Input/Output	Input / I/O	–		
JTAGSEL	JTAG Selection	Input	High		Permanent Internal Pull-down
Flash Memory					
ERASE	Flash and NVM Configuration Bits Erase Command	Input	High	VDDIO	Reset State: - Erase Input - Internal Pull-down enabled - Schmitt Trigger enabled(2)

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Reset/Test					
NRST	Synchronous Microcontroller Reset	I/O	Low	VDDIO	Permanent Internal Pull-up
TST	Test Select	Input	–		Permanent Internal Pull-down
Wake-up					
WKUP[15:0]	Wake-up Inputs	Input	–	VDDIO	–
Universal Asynchronous Receiver Transceiver - UARTx					
URXDx	UART Receive Data	Input	–	–	–
UTXDx	UART Transmit Data	Output	–	–	–
PIO Controller - PIOA - PIOB - PIOC - PIOD - PIOE					
PA0–PA31	Parallel IO Controller A	I/O	–	VDDIO	Reset State: - PIO or System IOs(4) - Internal Pull-up enabled - Schmitt Trigger enabled(2)
PB0–PB14	Parallel IO Controller B	I/O	–		
PC0–PC31	Parallel IO Controller C	I/O	–		
PD0–PD31	Parallel IO Controller D	I/O	–		Reset State: - PIO or System IOs(4) - Internal Pull-up enabled - Schmitt Trigger enabled(2)
PE0–PE5	Parallel IO Controller E	I/O	–		
PIO Controller - Parallel Capture Mode					
PIODC0–PIODC7	Parallel Capture Mode Data	Input	–	VDDIO	–
PIODCCLK	Parallel Capture Mode Clock	Input	–		
PIODCEN1–2	Parallel Capture Mode Enable	Input	–		
High Speed Multimedia Card Interface - HSMCI					
MCCK	Multimedia Card Clock	I/O	–	–	–
MCCDA	Multimedia Card Slot A Command	I/O	–	–	–
MCDA0–MCDA3	Multimedia Card Slot A Data	I/O	–	–	–
Universal Synchronous Asynchronous Receiver Transmitter USARTx					
SCKx	USARTx Serial Clock	I/O	–	–	–
TXDx	USARTx Transmit Data	I/O	–	–	–
RXDx	USARTx Receive Data	Input	–	–	–
RTSx	USARTx Request To Send	Output	–	–	–
CTSx	USARTx Clear To Send	Input	–	–	–
DTR1	USART1 Data Terminal Ready	I/O	–	–	–
DSR1	USART1 Data Set Ready	Input	–	–	–
DCD1	USART1 Data Carrier Detect	Output	–	–	–
RI1	USART1 Ring Indicator	Input	–	–	–

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Timer/Counter - TC					
TCLKx	TC Channel x External Clock Input	Input	–	–	–
TIOAx	TC Channel x I/O Line A	I/O	–	–	–
TIOBx	TC Channel x I/O Line B	I/O	–	–	–
Serial Peripheral Interface - SPI					
MISO	Master In Slave Out	I/O	–	–	–
MOSI	Master Out Slave In	I/O	–	–	–
SPCK	SPI Serial Clock	I/O	–	–	–
SPI_NPCS0	SPI Peripheral Chip Select 0	I/O	Low	–	–
SPI_NPCS1–SPI_NPCS3	SPI Peripheral Chip Select	Output	Low	–	–
Two-Wire Interface - TWIx					
TWDx	TWIx Two-wire Serial Data	I/O	–	–	–
TWCKx	TWIx Two-wire Serial Clock	I/O	–	–	–
Analog					
ADVREF	ADC, DAC and Analog Comparator Reference	Analog	–	–[1]	–
12-bit Analog-Front-End - AFEx					
AFE0_AD0–AFE0_AD14	Analog Inputs	Analog, Digital	–	–[1]	–
AFE1_AD0–AFE1_AD7	Analog Inputs	Analog, Digital	–	–[1]	–
ADTRG	Trigger	Input	–	VDDIO	–
12-bit Digital-to-Analog Converter - DAC					
DAC0–DAC1	Analog output	Analog, Digital	–	–[1]	–
DATRG	DAC Trigger	Input	–	VDDIO	–
Fast Flash Programming Interface - FFPI					
PGMEN0-PGMEN1	Programming Enable	Input		VDDIO	–
PGMM0-PGMM3	Programming Mode	Input			–
PGMD0-PGMD15	Programming Data	I/O			–
PGMRDY	Programming Ready	Output	High		–
PGMNVALID	Data Direction	Output	Low		–
PGMNOE	Programming Read	Input	Low		–
PGMCK	Programming Clock	Input			–
PGMNCMD	Programming Command	Input	Low		–
External Bus Interface					
D0–D7	Data Bus	I/O	–	–	–
A0–A23	Address Bus	Output	–	–	–
NWAIT	External Wait Signal	Input	Low	–	–

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Static Memory Controller - SMC					
NCS0–NCS3	Chip Select Lines	Output	Low	–	–
NRD	Read Signal	Output	Low	–	–
NWE	Write Enable	Output	Low	–	–
NAND Flash Logic					
NANDOE	NAND Flash Output Enable	Output	Low	–	–
NANDWE	NAND Flash Write Enable	Output	Low	–	–
Pulse Width Modulation Controller - PWMC					
PWMH	PWM Waveform Output High for channel x	Output	–	–	–
PWML	PWM Waveform Output Low for channel x	Output	–	–	Only output in complementary mode when dead time insertion is enabled.
PWMFI0	**PWM Fault Input**	Input	–	–	–
Ethernet MAC 10/100 - GMAC					
GTXCK	Transmit Clock	Input	–	–	–
GRXCK	Receive Clock	Input	–	–	–
GTXEN	Transmit Enable	Output	–	–	–
GTX0–GTX3	Transmit Data	Output	–	–	–
GTXER	Transmit Coding Error	Output	–	–	–
GRXDV	Receive Data Valid	Input	–	–	–
GRX0–GRX3	Receive Data	Input	–	–	–
GRXER	Receive Error	Input	–	–	–
GCRS	Carrier Sense	Input	–	–	–
GCOL	Collision Detected	Input	–	–	–
GMDC	Management Data Clock	Output	–	–	–
GMDIO	Management Data Input/Output	I/O	–	–	–
Controller Area Network - CAN (x=[0:1])					
CANRXx	CAN Receive	Input	–	–	–
CANTXx	CAN Transmit	Output	–	–	–
USB Full Speed Device					
DDM	DDM USB Full Speed Data -	Analog, Digital	–	–[1]	Reset State: - USB Mode - Internal Pull-down
DDP	DDP USB Full Speed Data +		–	–[1]	Reset State: - USB Mode - Internal Pull-down

Notes: 1. See Section 5.4 “Typical Powering Schematics” for restrictions on voltage range of Analog Cells and USB.
2. Schmitt Triggers can be disabled through PIO registers.

3. TDO pin is set in input mode when the Cortex-M4 Core is not in debug mode. Thus the internal pull-up corresponding to this PIO line must be enabled to avoid current consumption due to floating input.
4. Some PIO lines are shared with System I/Os.

4. Package and Pinout

The SAM4E is available in TFBGA100, LFBGA144, LQFP100, and LQFP144 and packages described in Section 47. “SAM4E Mechanical Characteristics”.

4.1 100-ball TFBGA Package and Pinout

4.1.1 100-ball TFBGA Package Outline

The 100-ball TFBGA package has a 0.8 mm ball pitch and respects Green Standards. Refer to Section 47.1 “100-ball TFBGA Package Drawing” for details.

4.1.2 100-ball TFBGA Pinout

Table 4-1. SAM4E 100-ball TFBGA Pinout

A1	PB9	C6	PD29	F1	PA19/PGMD7	H6	PA14/PGMD2
A2	PB8	C7	PA30	F2	PA20/PGMD8	H7	PA25/PGMD13
A3	PB14	C8	PB5	F3	PD23	H8	PA27/PGMD15
A4	PB10	C9	PD10	F4	GND	H9	PA5/PGMRDY
A5	PD4	C10	PA1/PGMEN1	F5	GND	H10	PA4/PGMNCMD
A6	PD7	D1	ADVREF	F6	GND	J1	PA21/PGMD9
A7	PA31	D2	PD1	F7	TST	J2	PA7/PGMNVALID
A8	PA6/PGMNOE	D3	GND	F8	PB12	J3	PA22/PGMD10
A9	PA28	D4	GND	F9	PA3	J4	PD22
A10	JTAGSEL	D5	PD5	F10	PD14	J5	PA16/PGMD4
B1	PD31	D6	VDDCORE	G1	PA17/PGMD5	J6	PA15/PGMD3
B2	PB13	D7	VDDCORE	G2	PA18/PGMD6	J7	PD28
B3	VDDPLL	D8	PA0/PGMEN0	G3	PD26	J8	PA11/PGMM3
B4	PB11	D9	PD11	G4	PD24	J9	PA9/PGMM1
B5	PD3	D10	PA2	G5	PA13/PGMD1	J10	PD17
B6	PD6	E1	PB0	G6	VDDCORE	K1	PD30
B7	PD8	E2	PB1	G7	VDDIO	K2	PA8/PGMM0
B8	PD9	E3	PD2	G8	PB6	K3	PD20
B9	PB4	E4	GND	G9	PD16	K4	PD19
B10	PD15	E5	VDDIO	G10	NRST	K5	PA23/PGMD11
C1	PD0	E6	VDDIO	H1	PB2	K6	PD18
C2	VDDIN	E7	GND	H2	PB3	K7	PA24/PGMD12
C3	VDDOUT	E8	PD13	H3	PD25	K8	PA26/PGMD14
C4	GND	E9	PB7	H4	PD27	K9	PA10/PGMM2
C5	PA29	E10	PD12	H5	PD21	K10	PA12/PGMD0

4.2 144-ball LFBGA Package and Pinout

4.2.1 144-ball LFBGA Package Outline

The 144-ball LFBGA package has a 0.8 mm ball pitch and respects Green Standards. Refer to Section 47.2 “144-ball LFBGA Package Drawing” for details.

4.2.2 144-ball LFBGA Pinout

Table 4-2. SAM4E 144-ball LFBGA Pinout

A1	PE1	D1	ADVREF	G1	PC15	K1	PE4
A2	PB9	D2	GND	G2	PC13	K2	PA21/PGMD9
A3	PB8	D3	PD31	G3	PB1	K3	PA22/PGMD10
A4	PB11	D4	PD0	G4	GND	K4	PC2
A5	PD2	D5	GNDPLL	G5	GND	K5	PA16/PGMD4
A6	PA29	D6	PD4	G6	GND	K6	PA14/PGMD2
A7	PC21	D7	PD5	G7	GND	K7	PC6
A8	PD6	D8	PC19	G8	VDDIO	K8	PA25/PGMD13
A9	PC20	D9	PD9	G9	PD13	K9	PD20
A10	PA30	D10	PD29	G10	PD12	K10	PD28
A11	PD15	D11	PC16	G11	PC9	K11	PD16
A12	PB4	D12	PA1/PGMEN1	G12	PB12	K12	PA4/PGMNCMD
B1	PE2	E1	PC31	H1	PA19/PGMD7	L1	PE5
B2	PB13	E2	PC27	H2	PA18/PGMD6	L2	PA7/PGMNVALID
B3	VDDPLL	E3	PE3	H3	PA20/PGMD8	L3	PC3
B4	PB10	E4	PC0	H4	PB0	L4	PA23/PGMD11
B5	PD1	E5	GND	H5	VDDCORE	L5	PA15/PGMD3
B6	PC24	E6	GND	H6	VDDIO	L6	PD26
B7	PD3	E7	VDDIO	H7	VDDIO	L7	PA24/PGMD12
B8	PD7	E8	VDDCORE	H8	VDDCORE	L8	PC5
B9	PA6/PGMNOE	E9	PD8	H9	PD21	L9	PA10/PGMM2
B10	PC18	E10	PC14	H10	PD14	L10	PA12/PGMD0
B11	JTAGSEL	E11	PD11	H11	TEST	L11	PD17
B12	PC17	E12	PA2	H12	NRST	L12	PC28
C1	VDDIN	F1	PC30	J1	PA17/PGMD5	M1	PD30
C2	PE0	F2	PC26	J2	PB2	M2	PA8/PGMM0
C3	VDDOUT	F3	PC29	J3	PB3	M3	PA13/PGMD1
C4	PB14	F4	PC12	J4	PC1	M4	PC7
C5	PC25	F5	GND	J5	PC4	M5	PD25
C6	PC23	F6	GND	J6	PD27	M6	PD24
C7	PC22	F7	GND	J7	VDDCORE	M7	PD23
C8	PA31	F8	VDDIO	J8	PA26/PGMD14	M8	PD22
C9	PA28	F9	PB7	J9	PA11/PGMM3	M9	PD19
C10	PB5	F10	PC10	J10	PA27/PGMD15	M10	PD18
C11	PA0/PGMEN0	F11	PC11	J11	PB6	M11	PA5/PGMRDY
C12	PD10	F12	PA3	J12	PC8	M12	PA9/PGMM1

4.3 100-lead LQFP Package and Pinout

4.3.1 100-lead LQFP Package Outline

The 100-lead LQFP package has a 0.5 mm ball pitch and respects Green Standards. Please refer to Section 47.3 “100-lead LQFP Package Drawing” for details.

4.3.2 100-lead LQFP Pinout

Table 4-3. SAM4E 100-lead LQFP Pinout

1	PD0	26	PA22/PGMD10	51	PD28	76	PD29
2	PD31	27	PA13/PGMD1	52	PA5/PGMRDY	77	PB5
3	GND	28	VDDIO	53	PD17	78	PD9
4	VDDOUT	29	GND	54	PA9/PGMM1	79	PA28
5	VDDIN	30	PA16/PGMD4	55	PA4/PGMNCMD	80	PD8
6	GND	31	PA23/PGMD11	56	PD16	81	PA6/PGMNOE
7	GND	32	PD27	57	PB6	82	PA30
8	GND	33	PA15/PGMD3	58	NRST	83	PA31
9	ADVREF	34	PA14/PGMD2	59	PD14	84	PD7
10	GND	35	PD25	60	TST	85	PD6
11	PB1	36	PD26	61	PB12	86	VDDCORE
12	PB0	37	PD24	62	PD13	87	PD5
13	PA20/PGMD8	38	PA24PGMD12	63	PB7	88	PD4
14	PA19/PGMD7	39	PD23	64	PA3	89	PD3
15	PA18/PGMD6	40	PA25/PGMD13	65	PD12	90	PA29
16	PA17/PGMD5	41	PD22	66	PA2	91	PD2
17	PB2	42	PA26/PGMD14	67	GND	92	PD1
18	VDDCORE	43	PD21	68	VDDIO	93	VDDIO
19	VDDIO	44	PA11/PGMM3	69	PD11	94	PB10
20	PB3	45	PD20	70	PA1/PGMEN1	95	PB11
21	PA21/PGMD9	46	PA10/PGMM2	71	PD10	96	VDDPLL
22	VDDCORE	47	PD19	72	PA0/PGMEN0	97	PB14
23	PD30	48	PA12/PGMD0	73	JTAGSEL	98	PB8
24	PA7/PGMNVALID	49	PD18	74	PB4	99	PB9
25	PA8/PGMM0	50	PA27/PGMD15	75	PD15	100	PB13

4.4 144-lead LQFP Package and Pinout

4.4.1 144-lead LQFP Package Outline

The 144-lead LQFP package has a 0.5 mm ball pitch and respects Green Standards. Please refer to Section 47.4 “144-lead LQFP Package Drawing” for details.

4.4.2 144-lead LQFP Pinout

Table 4-4. SAM4E 144-lead LQFP Pinout

1	PD0	37	PA22/PGMD10	73	PA5/PGMRDY	109	PB5
2	PD31	38	PC1	74	PD17	110	PD9
3	VDDOUT	39	PC2	75	PA9/PGMM1	111	PC18
4	PE0	40	PC3	76	PC28	112	PA28
5	VDDIN	41	PC4	77	PA4/PGMNCMD	113	PD8
6	PE1	42	PA13/PGMD1	78	PD16	114	PA6/PGMNOE
7	PE2	43	VDDIO	79	PB6	115	GND
8	GND	44	GND	80	VDDIO	116	PA30
9	ADVREFP	45	PA16/PGMD4	81	VDDCORE	117	PC19
10	PE3	46	PA23/PGMD11	82	PC8	118	PA31
11	PC0	47	PD27	83	NRST	119	PD7
12	PC27	48	PC7	84	PD14	120	PC20
13	PC26	49	PA15/PGMD3	85	TEST	121	PD6
14	PC31	50	VDDCORE	86	PC9	122	PC21
15	PC30	51	PA14/PGMD2	87	PB12	123	VDDCORE
16	PC29	52	PD25	88	PD13	124	PC22
17	PC12	53	PD26	89	PB7	125	PD5
18	PC15	54	PC6	90	PC10	126	PD4
19	PC13	55	PD24	91	PA3	127	PC23
20	PB1	56	PA24/PGMD12	92	PD12	128	PD3
21	PB0	57	PD23	93	PA2	129	PA29
22	PA20/PGMD8	58	PC5	94	PC11	130	PC24
23	PA19/PGMD7	59	PA25/PGMD13	95	GND	131	PD2
24	PA18/PGMD6	60	PD22	96	VDDIO	132	PD1
25	PA17/PGMD5	61	GND	97	PC14	133	PC25
26	PB2	62	PA26/PGMD14	98	PD11	134	VDDIO
27	PE4	63	PD21	99	PA1/PGMEN1	135	GND
28	PE5	64	PA11/PGMM3	100	PC16	136	PB10
29	VDDCORE	65	PD20	101	PD10	137	PB11
30	VDDIO	66	PA10/PGMM2	102	PA0/PGMEN0	138	GND
31	PB3	67	PD19	103	PC17	139	VDDPLL
32	PA21/PGMD9	68	PA12/PGMD0	104	JTAGSEL	140	PB14
33	VDDCORE	69	PD18	105	PB4	141	PB8
34	PD30	70	PA27/PGMD15	106	PD15	142	PB9
35	PA7/PGMNVALID	71	PD28	107	VDDCORE	143	VDDIO
36	PA8/PGMM0	72	VDDIO	108	PD29	144	PB13

5. Power Considerations

5.1 Power Supplies

The SAM4E has several types of power supply pins:

- VDDCORE pins: power the core, the first flash rail, the embedded memories and the peripherals.
  Voltage ranges from 1.08V to 1.32V.
- VDDIO pins: power the peripheral I/O lines (Input/Output Buffers), the second flash rail, the backup part, the USB transceiver, 32 kHz crystal oscillator and oscillator pads.
  Voltage ranges from 1.62V to 3.6V.
- VDDIN pins: voltage regulator input, DAC and Analog Comparator power supply.
  Voltage ranges from 1.62V to 3.6V.
- VDDPLL pin: powers the PLL, the Fast RC and the 3 to 20 MHz oscillator.
  Voltage ranges from 1.08V to 1.32V.

5.2 Power-up Considerations

5.2.1 VDDIO Versus VDDCORE

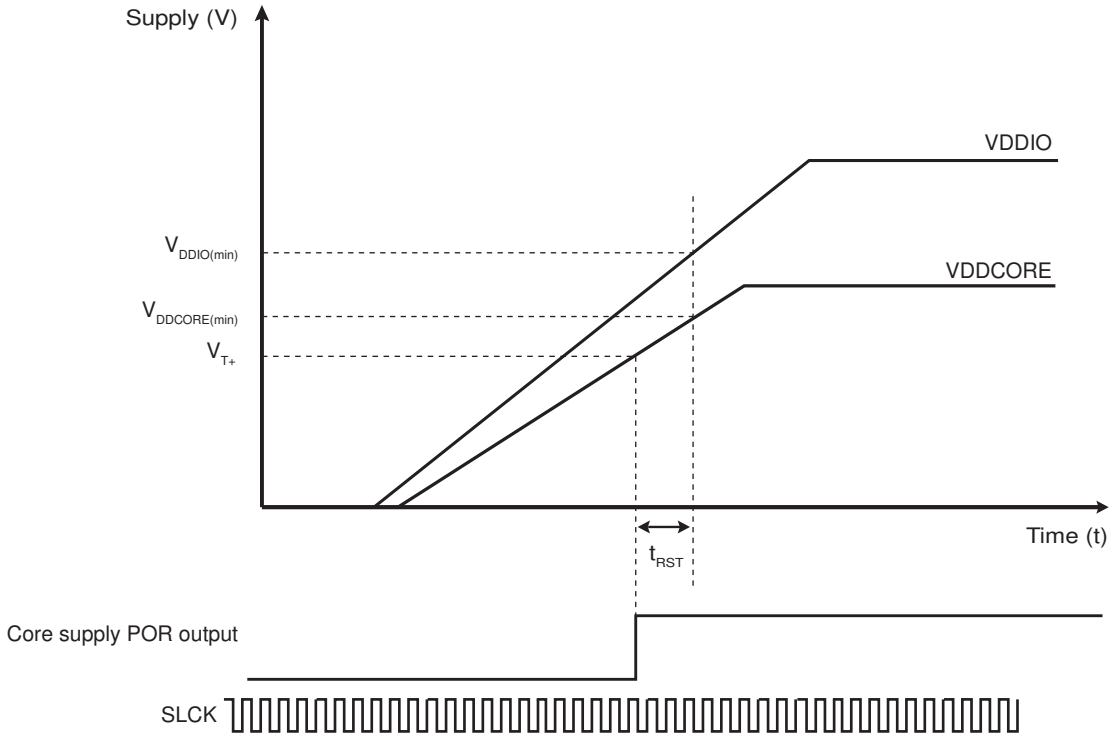
V_{DDIO} must always be higher than or equal to V_{DDCORE}.

V_{DDIO} must reach its minimum operating voltage (1.62 V) before V_{DDCORE} has reached $V_{DDCORE(min)}$. The minimum slope for V_{DDCORE} is defined by ($V_{DDCORE(min)}$ - V_{T+}) / t_{RST}.

If V_{DDCORE} rises at the same time as V_{DDIO}, the V_{DDIO} rising slope must be higher than or equal to 8.8 V/ms.

If VDDCORE is powered by the internal regulator, all power-up considerations are met

Figure 5-1. VDDCORE and VDDIO Constraints at Startup



5.2.2 VDDIO Versus VDDIN

At power-up, V_{DDIO} needs to reach 0.6 V before V_{DDIN} reaches 1.0 V.

VDDIO voltage needs to be equal to or below (VDDIN voltage + 0.5 V).

5.3 Voltage Regulator

The SAM4E embeds a voltage regulator that is managed by the Supply Controller.

This internal regulator is designed to supply the internal core of SAM4E. It features two operating modes:

- In Normal mode, the voltage regulator consumes less than 500 µA static current and draws 80 mA of output current. Internal adaptive biasing adjusts the regulator quiescent current depending on the required load current. In Wait Mode quiescent current is only 5 µA.
- In Backup mode, the voltage regulator consumes less than 1.5 µA while its output (VDDOUT) is driven internally to GND. The default output voltage is 1.20V and the start-up time to reach Normal mode is less than 300 µs.

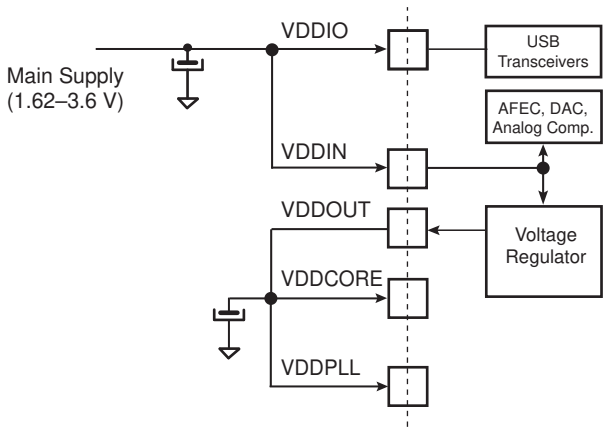
For adequate input and output power supply decoupling/bypassing, refer to Table 46-3, “1.2V Voltage Regulator Characteristics,” on page 1357.

5.4 Typical Powering Schematics

The SAM4E supports a 1.62–3.6 V single supply mode. The internal regulator input is connected to the source and its output feeds VDDCORE. Figure 5-2 shows the power schematics.

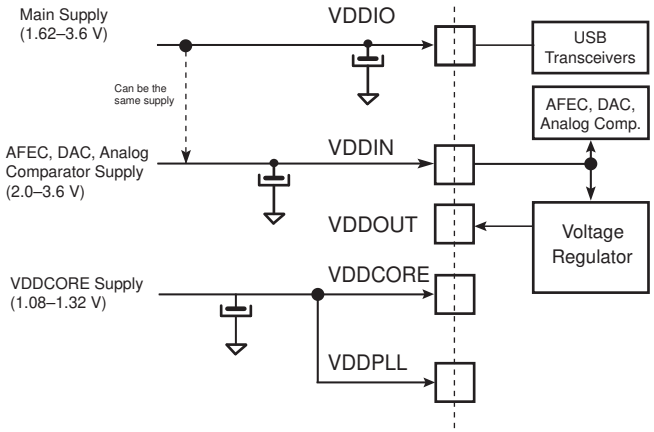
As VDDIN powers the voltage regulator, the DAC and the analog comparator, when the user does not want to use the embedded voltage regulator, it can be disabled by software via the SUPC (note that this is different from Backup mode).

Figure 5-2. Single Supply



Note: Restrictions:
- For USB, VDDIO needs to be greater than 3.0V
- For AFEC, DAC, and Analog Comparator, VDDIN needs to be greater than 2.4V

Figure 5-3. Core Externally Supplied



Note: Restrictions:
- For USB, VDDIO needs to be greater than 3.0V
- For AFEC, DAC, and Analog Comparator, VDDIN needs to be greater than 2.4V

5.5 Active Mode

Active mode is the normal running mode with the core clock running from the fast RC oscillator, the main crystal oscillator or the PLLA. The power management controller can be used to adapt the frequency and to disable the peripheral clocks.

5.6 Low-power Modes

The SAM4E has the following low-power modes: Backup mode, Wait mode and Sleep mode.

Note: The Wait For Event instruction (WFE) of the Cortex-M4 core can be used to enter any of the low-power modes, however, this may add complexity in the design of application state machines. This is due to the fact that the WFE instruction goes along with an event flag of the Cortex core (cannot be managed by the software application). The event flag can be set by interrupts, a debug event or an event signal from another processor. Since it is possible for an interrupt to occur just before the execution of WFE, WFE takes into account events that happened in the past. As a result, WFE prevents the device from entering wait mode if an interrupt event has occurred.
Atmel has made provision to avoid using the WFE instruction. The workarounds to ease application design are as follows:
- For backup mode, switch off the voltage regulator and configure the VROFF bit in the Supply Controller Control Register (SUPC_CR).
- For wait mode, configure the WAITMODE bit in the PMC Clock Generator Main Oscillator Register of the Power Management Controller (PMC)
- For sleep mode, use the Wait for Interrupt (WFI) instruction.

Complete information is available in Table 5-1 “Low-power Mode Configuration Summary”.

5.6.1 Backup Mode

The purpose of Backup mode is to achieve the lowest power consumption possible in a system which is performing periodic wake-ups to perform tasks but not requiring fast startup time. Total current consumption is 1 µA typical (VDDIO = 1.8 V at 25°C).

The Supply Controller, zero-power power-on reset, RTT, RTC, backup registers and 32 kHz oscillator (RC or crystal oscillator selected by software in the Supply Controller) are running. The regulator and the core supply are off.

The SAM4E can be woken up from this mode using the pins WKUP0–15, the supply monitor (SM), the RTT or RTC wake-up event.

Backup mode is entered by writing a 1 to the VROFF bit of the Supply Controller Control Register (SUPC_CR) (A key is needed to write the VROFF bit, refer to Section 18. “Supply Controller (SUPC)”) and with the SLEEPDEEP bit in the Cortex-M4 System Control Register set to 1. (See the power management description in Section 11. “ARM Cortex-M4 Processor”).

To enter Backup mode using the VROFF bit:

- Write a 1 to the VROFF bit of SUPC_CR.

To enter Backup mode using the WFE instruction:

- Write a 1 to the SLEEPDEEP bit of the Cortex-M4 processor.
- Execute the WFE instruction of the processor.

In both cases, exit from Backup mode happens if one of the following enable wake-up events occurs:

- Level transition, configurable debouncing on pins WKUPEN0–15
- Supply Monitor alarm
- RTC alarm
- RTT alarm

5.6.2 Wait Mode

The purpose of Wait mode is to achieve very low power consumption while maintaining the whole device in a powered state for a startup time of less than 10 µs. Current consumption in Wait mode is typically 32 µA (total current consumption) if the internal voltage regulator is used.

In this mode, the clocks of the core, peripherals and memories are stopped. However, the core, peripherals and memories power supplies are still powered. From this mode, a fast start up is available.

This mode is entered by setting the WAITMODE bit to 1 in the PMC Clock Generator Main Oscillator Register (CKGR_MOR) in conjunction with FLPM = 0 or FLPM = 1 bits of the PMC Fast Startup Mode Register (PMC_FSMR) or by the WFE instruction.

The Cortex-M4 is able to handle external or internal events in order to wake-up the core. This is done by configuring the external lines WKUP0–15 as fast startup wake-up pins (refer to Section 5.8 “Fast Start-up”). RTC or RTT Alarm and USB wake-up events can be used to wake up the CPU.

To enter Wait mode with WAITMODE bit:

1. Select the 4/8/12 MHz fast RC oscillator as Main Clock.
2. Set the FLPM field in the PMC_FSMR.
3. Set Flash Wait State to 0.
4. Set the WAITMODE bit = 1 in CKGR_MOR.
5. Wait for Master Clock Ready MCKRDY = 1 in the PMC Status Register (PMC_SR).

To enter Wait mode with WFE:

1. Select the 4/8/12 MHz fast RC oscillator as Main Clock.
2. Set the FLPM field in the PMC_FSMR.
3. Set Flash Wait State to 0.
4. Set the LPM bit in the PMC_FSMR.
5. Execute the Wait-For-Event (WFE) instruction of the processor.

In both cases, depending on the value of the field FLPM, the Flash enters one of three different modes:

- FLPM = 0 in Standby mode (low consumption)
- FLPM = 1 in Deep power-down mode (extra low consumption)
- FLPM = 2 in Idle mode. Memory ready for Read access

Table 5-1 summarizes the power consumption, wake-up time and system state in Wait mode.

5.6.3 Sleep Mode

The purpose of Sleep mode is to optimize power consumption of the device versus response time. In this mode, only the core clock is stopped. The peripheral clocks can be enabled. The current consumption in this mode is application dependent.

This mode is entered via Wait for Interrupt (WFI) or WFE instructions with bit LPM = 0 in PMC_FSMR.

The processor can be woken up from an interrupt if the WFI instruction of the Cortex-M4 is used or from an event if the WFE instruction is used.

5.6.4 Low-power Mode Summary Table

The modes detailed above are the main low-power modes. Each part can be set to on or off separately and wake-up sources can be configured individually. Table 5-1 provides the configuration summary of the low-power modes.

Table 5-1. Low-power Mode Configuration Summary

Mode	SUPC, 32 kHz Osc., RTC, RTT, GPBR, POR (Backup Region)	Regulator	Core Memory Peripherals	Mode Entry	Potential Wake-Up Sources	Core at Wake-Up	PIO State while in Low-Power Mode	PIO State at Wake Up	Consumption (2) (3)	Wake-up Time(1)
Backup Mode	ON	OFF	OFF (Not powered)	VROFF = 1 or WFE + SLEEPDEEP = 1	WKUP0–15 pins SM alarm RTC alarm RTT alarm	Reset	Previous state saved	PIOA & PIOB & PIOC & PIOD & PIOE Inputs with pull-ups	1 µA typ(4)	< 1 ms
Wait Mode w/Flash in Standby Mode	ON	ON	Powered (Not clocked)	WAITMODE = 1 + FLPM = 0 or WFE + SLEEPDEEP = 0 + LPM = 1 + FLPM = 0	Any Event from: Fast startup through WKUP0–15 RTC alarm RTT alarm USB wake-up	Clocked back	Previous state saved	Unchanged	56 µA(5)	10 µs
Wait Mode w/Flash in Deep Power-down Mode	ON	ON	Powered (Not clocked)	WAITMODE = 1 + FLPM = 1 or WFE + SLEEPDEEP = 0 + LPM = 1 + FLPM = 1	Any Event from: Fast startup through WKUP0–15 RTC alarm RTT alarm USB wake-up	Clocked back	Previous state saved	Unchanged	46.6 µA	< 100 µs
Sleep Mode	ON	ON	Powered(7) (Not clocked)	WFE or WFI + SLEEPDEEP = 0 + LPM = 0	Entry mode = WFI Interrupt Only; Entry mode = WFE Any Enabled Interrupt and/or Any Event from: Fast start-up through WKUP0–15 RTC alarm RTT alarm USB wake-up	Clocked back	Previous state saved	Unchanged	(6)	(6)

Notes:
1. When considering wake-up time, the time required to start the PLL is not taken into account. Once started, the device works with the 4/8/12 MHz fast RC oscillator. The user has to add the PLL start-up time if it is needed in the system. The wake-up time is defined as the time taken for wake up until the first instruction is fetched.
2. The external loads on PIOs are not taken into account in the calculation.
3. Supply Monitor current consumption is not included.
4. Total consumption is 1 µA typical (VDDIO = 1.8 V at 25°C).
5. Power consumption on VDDCORE. For total current consumption, please refer to Section 46. “SAM4E Electrical Characteristics”.
6. Depends on MCK frequency.
7. In this mode the core is supplied and not clocked but some peripherals can be clocked.

5.7 Wake-up Sources

The wake-up events allow the device to exit the Backup mode. When a wake-up event is detected, the Supply Controller performs a sequence which automatically reenables the core power supply and the SRAM power supply, if they are not already enabled. See Figure 18-4 ”Wake-up Sources”.

5.8 Fast Start-up

The SAM4E allows the processor to restart in a few microseconds while the processor is in Wait mode or in Sleep mode. A fast start-up can occur upon detection of a low level on one of the 19 wake-up inputs (WKUP0 to 15 + RTC + RTT + USB).

The fast restart circuitry (shown in Figure 29-4 ”Fast Startup Circuitry”) is fully asynchronous and provides a fast start-up signal to the Power Management Controller. As soon as the fast start-up signal is asserted, the PMC automatically restarts the embedded 4/8/12 MHz Fast RC oscillator, switches the master clock on this 4 MHz clock by default and reenables the processor clock.

6. Input/Output Lines

The SAM4E has several kinds of input/output (I/O) lines such as general purpose I/Os (GPIO) and system I/Os. GPIOs can have alternate functionality due to multiplexing capabilities of the PIO controllers. The same PIO line can be used whether in I/O mode or by the multiplexed peripheral. System I/Os include pins such as test pins, oscillators, erase or analog inputs.

6.1 General Purpose I/O Lines

GPIO Lines are managed by PIO Controllers. All I/Os have several input or output modes such as pull-up or pull-down, input Schmitt triggers, multi-drive (open-drain), glitch filters, debouncing or input change interrupt. Programming of these modes is performed independently for each I/O line through the PIO controller user interface. For more details, refer to Section 33. “Parallel Input/Output Controller (PIO)”.

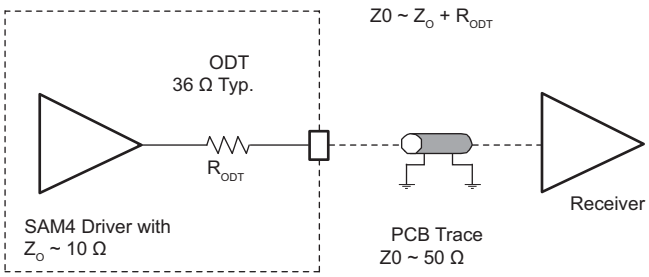
Some GPIOs can have an alternate function as analog input. When a GPIO is set in analog mode, all digital features of the I/O are disabled.

The input/output buffers of the PIO lines are supplied through VDDIO power supply rail.

The SAM4E device embeds high speed pads able. See Section 46.11 “AC Characteristics” for more details. Typical pull-up and pull-down value is 100 kΩ for all I/Os.

Each I/O line also embeds an ODT (On-Die Termination), (see Figure 6-1 below). It consists of an internal series resistor termination scheme for impedance matching between the driver output (SAM4E) and the PCB trace impedance preventing signal reflection. The series resistor helps to reduce IOs switching current (di/dt) thereby reducing in turn, EMI. It also decreases overshoot and undershoot (ringing) due to inductance of interconnect between devices or between boards. In conclusion, ODT helps diminish signal integrity issues.

Figure 6-1. On-die Termination



6.2 System I/O Lines

Table 6-1 lists the SAM4E system I/O lines shared with PIO lines.

These pins are software configurable as general purpose I/O or system pins. At startup, the default function of these pins is always used.

Table 6-1. System I/O Configuration Pin List

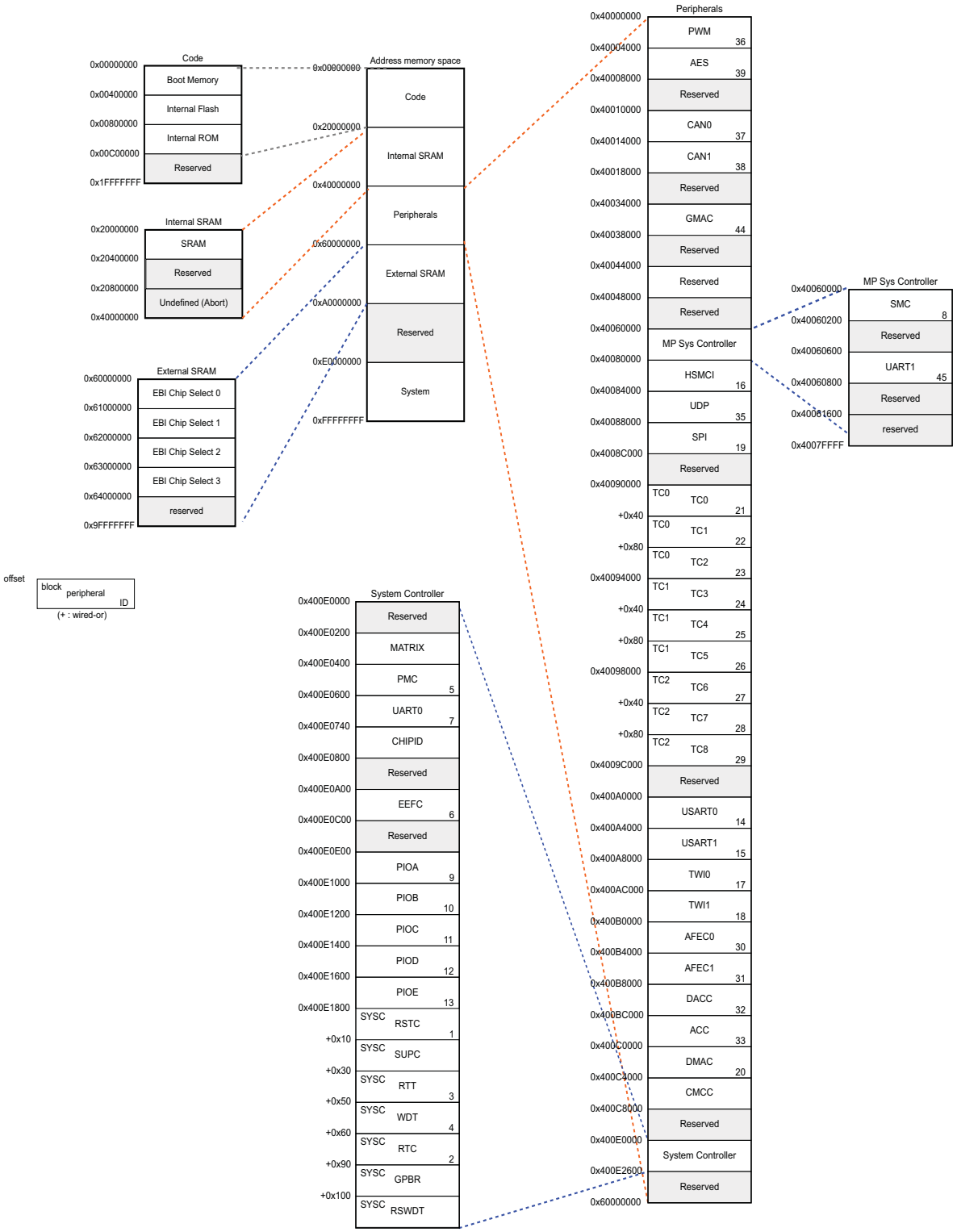
CCFG_SYSIO Bit No.	Default Function after Reset	Other Function	Constraints for Normal Start	Configuration
12	ERASE	PB12	Low Level at startup(1)	In Matrix User Interface Registers (Refer to the System I/O Configuration Register in Section 24. “Bus Matrix (MATRIX)”.)
7	TCK/SWCLK	PB7	–	
6	TMS/SWDIO	PB6	–	
5	TDO/TRACESWO	PB5	–	
4	TDI	PB4	–	
–	PA7	XIN32(2)	–	(3)
–	PA8	XOUT32(2)	–	
–	PB9	XIN	–	(4)
–	PB8	XOUT	–	

Notes:
1. If PB12 is used as PIO input in user applications, a low level must be ensured at startup to prevent Flash erase before the user application sets PB12 into PIO mode.
2. When the 32kHz oscillator is used in Bypass mode, XIN32 (PA7) is used as external clock source input and XOUT32 (PA8) can be left unconnected or used as GPIO.
3. Refer to Section 18.4.2 “Slow Clock Generator”.
4. Refer to Section 28.5.3 “3 to 20 MHz Crystal or Ceramic Resonator-based Oscillator”.

7. Memories

7.1 Product Mapping

Figure 7-1. SAM4E Product Mapping



7.2 Embedded Memories

7.2.1 Internal SRAM

The SAM4E device (1024 Kbytes) embeds a total of 128-Kbyte high-speed SRAM.

The SRAM is accessible over System Cortex-M4 bus at address 0x2000_0000.

The SRAM is in the bit band region. The bit band alias region is from 0x2200_0000 to 0x23FF_FFFF.

7.2.2 Internal ROM

The SAM4E device embeds an Internal ROM, which contains the SAM Boot Assistant (SAM-BA®), In Application Programming routines (IAP) and Fast Flash Programming Interface (FFPI).

At any time, the ROM is mapped at address 0x0080 0000.

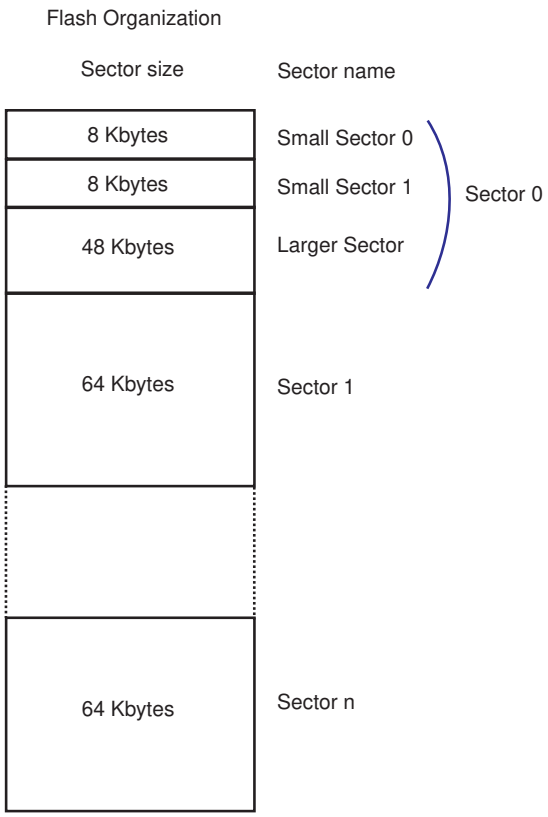
7.2.3 Embedded Flash

7.2.3.1 Flash Overview

The memory is organized in sectors. Each sector has a size of 64 Kbytes. The first sector of 64 Kbytes is divided into three smaller sectors.

The three smaller sectors are organized to consist of two sectors of 8 Kbytes and one sector of 48 Kbytes. Refer to Figure 7-2.

Figure 7-2. Global Flash Organization



Each Sector is organized in pages of 512 bytes.