Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

SAM4N8 / SAM4N16

Atmel | SMART ARM-based MCU

DATASHEET

Description

The Atmel® | SMART SAM4N series is a member of a family of Flash microcontrollers based on the high performance 32-bit ARM® Cortex®-M4 RISC processor. It operates at a maximum speed of 100 MHz and features up to 1024 Kbytes of Flash and up to 80 Kbytes of SRAM. The peripheral set includes 3 USARTs, 4 UARTs, 3 TWIs, 1 SPI, as well as 1 PWM timer, 2 three-channel general-purpose 16-bit timers (with stepper motor and quadrature decoder logic support), a low-power RTC, a low-power RTT, 256-bit general purpose backup registers, a 10-bit ADC (up to 12-bit with digital averaging) and a 10-bit DAC with an internal voltage reference.

The SAM4N devices have three software-selectable low-power modes: Sleep, Wait and Backup. In Sleep mode, the processor is stopped while all other functions can be kept running. In Wait mode, all clocks and functions are stopped but some peripherals can be configured to wake up the system based on predefined conditions. In Backup mode, only the RTC, RTT, and wake-up logic are running.

The Real-time Event Managment allows peripherals to receive, react to and send events in Active and Sleep modes without processor intervention.

The SAM4N device is a medium range general purpose microcontroller with the best ratio in terms of reduced power consumption, processing power and peripheral set. This enables the SAM4N to sustain a wide range of applications including industrial automation and M2M (machine-to-machine), energy metering, consumer and appliance, building and home control.

It operates from 1.62V to 3.6V and is available in 48, 64, and 100-pin QFP, 48 and 64-pin QFN, and 100-ball BGA packages.

The SAM4N series offers pin-to-pin compatibility with Atmel SAM4S, SAM3S, SAM3N and SAM7S devices, facilitating easy migration within the portfolio.

The SAM4N series is the ideal migration path from the SAM4S for applications that require a reduced BOM cost.

1. Features

- Core
  - ARM Cortex-M4 running at up to 100 MHz
  - Memory Protection Unit (MPU)
  - Thumb®-2 instruction Set
- Pin-to-pin compatible with SAM3N, SAM3S products (48/64/100-pin versions), SAM4S (64/100-pin versions) and SAM7S legacy products (64-pin version)
- Memories
  - Up to 1024 Kbytes embedded Flash
  - Up to 80 Kbytes embedded SRAM
  - 8 Kbytes ROM with embedded boot loader routines (UART) and IAP routines, single-cycle access at maximum speed
- System
  - Embedded voltage regulator for single supply operation
  - Power-on-Reset (POR), Brown-out Detector (BOD) and Watchdog for safe operation
  - Quartz or ceramic resonator oscillators: 3 to 20 MHz main power with Failure Detection and optional low power 32.768 kHz for RTC or device clock
  - High precision 8/12 MHz factory trimmed internal RC oscillator with 4 MHz default frequency for device startup. In-application trimming access for frequency adjustment
  - Slow Clock Internal RC oscillator as permanent low-power mode device clock
  - PLL up to 240 MHz for device clock
  - Temperature Sensor
  - Up to 23 peripheral DMA (PDC) channels
- Low-power Modes
  - Sleep, Wait, and Backup modes, down to 0.7 µA in Backup mode with RTC, RTT, and GPBR
- Peripherals
  - Up to 3 USARTs with ISO7816, IrDA (only USART0), RS-485, and SPI Mode
  - Up to 4 two-wire UARTs
  - Up to 3 Two-wire Interfaces (TWI)
  - 1 SPI
  - 2 Three-channel 16-bit Timer Counter blocks with capture, waveform, compare and PWM mode, Quadrature Decoder Logic and 2-bit Gray Up/Down for Stepper Motor
  - 1 Four-channel 16-bit PWM
  - 32-bit low-power Real-time Timer (RTT) and low-power Real-time Clock (RTC) with calendar and alarm features
  - 256-bit General Purpose Backup Registers (GPBR)
- I/Os
  - Up to 79 I/O lines with external interrupt capability (edge or level sensitivity), debouncing, glitch filtering and on-die Series Resistor Termination. Individually Programmable Open-drain, Pull-up and Pull-down resistor and Synchronous Output
  - Three 32-bit Parallel Input/Output Controllers
- Analog
  - One 10-bit ADC up to 510 ksps, with Digital Averaging Function providing Enhanced Resolution Mode up to 12-bit, up to 16-channels
  - One 10-bit DAC up to 1 msps
  - Internal voltage reference, 3V typ

- Packages
  - 100-lead LQFP – 14 x 14 mm, pitch 0.5 mm
  - 100-ball TFBGA – 9 x 9 mm, pitch 0.8 mm
  - 100-ball VFBGA – 7 x 7 mm, pitch 0.65 mm
  - 64-lead LQFP – 10 x 10 mm, pitch 0.5 mm
  - 64-pad QFN – 9 x 9 mm, pitch 0.5 mm
  - 48-lead LQFP – 7 x7 mm, pitch 0.5 mm
  - 48-pad QFN – 7 x 7 mm, pitch 0.5 mm

1.1 Configuration Summary

The SAM4N series devices differ in memory size, package and features. Table 1-1 summarizes the configurations of the device family.

Table 1-1. Configuration Summary

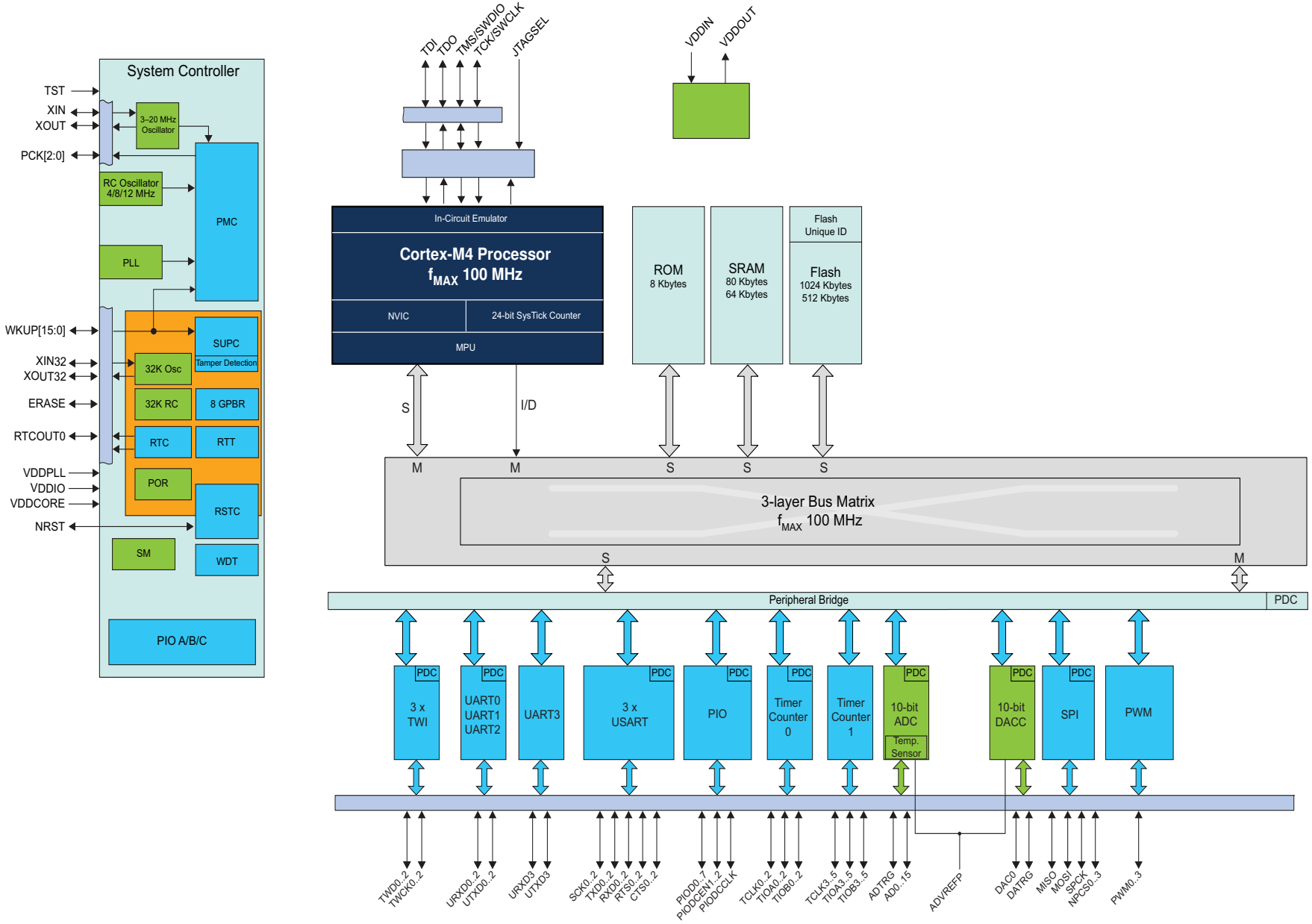
Feature	SAM4N16C	SAM4N16B	SAM4N8C	SAM4N8B	SAM4N8A
Flash	1024 Kbytes	1024 Kbytes	512 Kbytes	512 Kbytes	512 Kbytes
SRAM	80 Kbytes	80 Kbytes	64 Kbytes	64 Kbytes	64 Kbytes
Package	LQFP100 TFBGA100 VFBGA100	LQFP64 QFN64	LQFP100 TFBGA100 VFBGA100	LQFP64 QFN64	LQFP48 QFN48
Number of PIOs	79	47	79	47	34
10-bit ADC	17 ch (1)	11 ch (1)	17 ch (1)	11 ch (1)	9 ch (1)
10-bit DAC	1 ch	1 ch	1 ch	1 ch	–
16-bit Timer	6	6(2)	6	6(2)	6(5)
PDC Channels	23	23	23	23	23
USART/UART	3/4	2/4	3/4	2/4	1/4
SPI	4(3)	3(3)	4(3)	3(3)	2(3)
TWI	3	3	3	3	3
PWM	7(4)	4(4)	7(4)	4(4)	4(4)

Notes:
1. Includes Temperature Sensor
2. Only 3 channels output
3. USARTs with SPI mode are taken into account.
4. Timer Counter in PWM mode is taken into account
5. Only 2 channels output

2. Block Diagram

See Table 1-1 for detailed configurations of memory size, package and features of the SAM4N devices.

Figure 2-1. SAM4N 100-pin Version Block Diagram



3. Signals Description

Table 3-1 gives details on signal names classified by peripheral.

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Power Supplies					
VDDIO	Peripherals I/O Lines Power Supply	Power			1.62V to 3.6V
VDDIN	Voltage Regulator, ADC and DAC Power Supply	Power			1.6V to 3.6V
VDDOUT	Voltage Regulator Output	Power			1.2V Output
VDDPLL	Oscillator Power Supply	Power			1.08V to 1.32V
VDDCORE	Core Chip Power Supply	Power			1.08V to 1.32V Connected externally to VDDOUT
GND	Ground	Ground			
Clocks, Oscillators and PLLs					
XIN	Main Oscillator Input	Input		VDDIO	
XOUT	Main Oscillator Output	Output			
XIN32	Slow Clock Oscillator Input	Input		VDDIO	
XOUT32	Slow Clock Oscillator Output	Output			
PCK0–PCK2	Programmable Clock Output	Output			
ICE and JTAG					
TCK	Test Clock	Input		VDDIO	No pull-up resistor
TDI	Test Data In	Input		VDDIO	No pull-up resistor
TDO	Test Data Out	Output		VDDIO	
TRACESWO	Trace Asynchronous Data Out	Output		VDDIO	
SWDIO	Serial Wire Input/Output	I/O		VDDIO	
SWCLK	Serial Wire Clock	Input		VDDIO	
TMS	Test Mode Select	Input		VDDIO	No pull-up resistor
JTAGSEL	JTAG Selection	Input	High	VDDIO	Pull-down resistor
Flash Memory					
ERASE	Flash and NVM Configuration Bits Erase Command	Input	High	VDDIO	Pull-down (15 kΩ) resistor
Reset/Test					
NRST	Microcontroller Reset	I/O	Low	VDDIO	Pull-up resistor
TST	Test Mode Select	Input		VDDIO	Pull-down resistor
Universal Asynchronous Receiver Transmitter - UARTx					
URXDx	UART Receive Data	Input			
UTXDx	UART Transmit Data	Output			

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
PIO Controller - PIOA - PIOB - PIOC					
PA0–PA31	Parallel IO Controller A	I/O		VDDIO	Pulled-up input at reset
PB0–PB14	Parallel IO Controller B	I/O		VDDIO	Pulled-up input at reset
PC0–PC31	Parallel IO Controller C	I/O		VDDIO	Pulled-up input at reset
Universal Synchronous Asynchronous Receiver Transmitter USARTx					
SCKx	USARTx Serial Clock	I/O			
TXDx	USARTx Transmit Data	I/O			
RXDx	USARTx Receive Data	Input			
RTSx	USARTx Request To Send	Output			
CTSx	USARTx Clear To Send	Input			
Timer Counter - TCx					
TCLKx	TC Channel x External Clock Input	Input			
TIOAx	TC Channel x I/O Line A	I/O			
TIOBx	TC Channel x I/O Line B	I/O			
Pulse Width Modulation Controller - PWMC					
PWM	PWM Waveform Output for channel	Output			
Serial Peripheral Interface - SPI					
MISO	Master In Slave Out	I/O			
MOSI	Master Out Slave In	I/O			
SPCK	SPI Serial Clock	I/O			
NPCS0	SPI Peripheral Chip Select 0	I/O	Low		
NPCS1–NPCS3	SPI Peripheral Chip Select	Output	Low		
Two-wire Interface - TWIx					
TWDx	TWIx Two-wire Serial Data	I/O			
TWCKx	TWIx Two-wire Serial Clock	I/O			
Analog					
ADVREFP[1]	ADC and DAC Reference	Analog			
10-bit Analog-to-Digital Converter - ADC					
AD0–AD15	Analog Inputs	Analog			
ADTRG	ADC Trigger	Input			
Digital-to-Analog Converter - DAC					
DAC0	DAC Channel Analog Output	Analog			
DACTRG	DAC Trigger	Input			

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Fast Flash Programming Interface - FFPI					
PGMEN0–PGMEN2	Programming Enabling	Input		VDDIO	
PGMM0–PGMM3	Programming Mode	Input		VDDIO	
PGMD0–PGMD15	Programming Data	I/O		VDDIO	
PGMRDY	Programming Ready	Output	High	VDDIO	
PGMNVALID	Data Direction	Output	Low	VDDIO	
PGMNOE	Programming Read	Input	Low	VDDIO	
PGMCK	Programming Clock	Input		VDDIO	
PGMNCMD	Programming Command	Input	Low	VDDIO	

Note: 1. “ADVREFP” is named “ADVREF” in Section 17. “Supply Controller (SUPC)” and in Section 34. “Analog-to-Digital Converter (ADC)”.

4. Package and Pinout

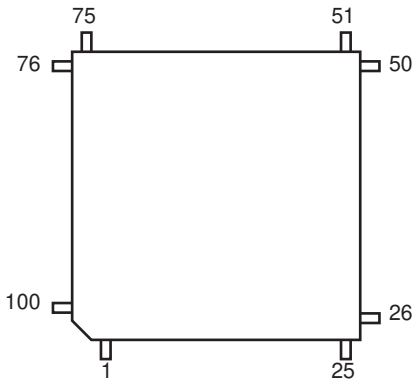
SAM4N devices are pin-to-pin compatible with SAM3N4.

Table 4-1. SAM4N Packages

Device	100 Pins/Balls	64 Pins/Balls	48 Pins/Balls
SAM4N16	LQFP, TFBGA and VFBGA	LQFP and QFN	–
SAM4N8	LQFP, TFBGA and VFBGA	LQFP and QFN	LQFP and QFN

4.1 Overview of the 100-lead LQFP Package

Figure 4-1. Orientation of the 100-lead LQFP Package

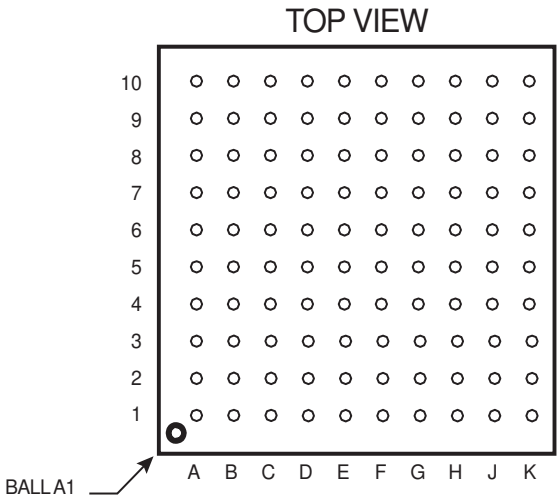


Refer to Section 37. “SAM4N Mechanical Characteristics” for mechanical drawings and specifications.

4.2 Overview of the 100-ball TFBGA Package

The 100-ball TFBGA package respects the Green Standards.

Figure 4-2. Orientation of the 100-ball TFBGA Package

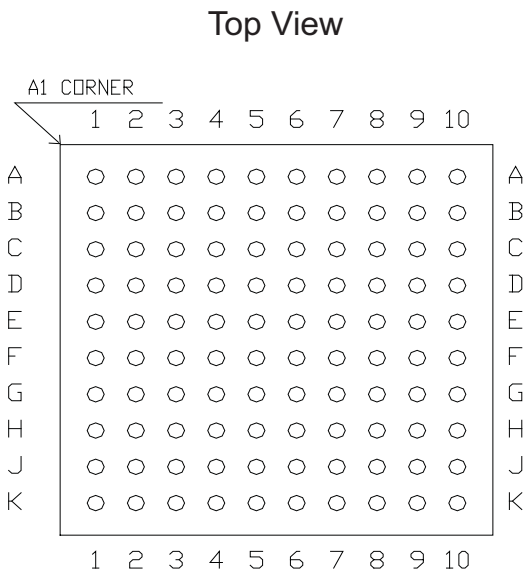


Refer to Section 37. “SAM4N Mechanical Characteristics” for mechanical drawings and specifications.

4.3 Overview of the 100-ball VFBGA Package (7 x 7 x 1 mm - 0.65 mm ball pitch)

The 100-ball VFBGA package respects the Green Standards.

Figure 4-3. Orientation of the 100-ball VFBGA Package



Refer to Section 37. “SAM4N Mechanical Characteristics” for mechanical drawings and specifications.

4.4 100-lead LQFP, TFBGA and VFBGA Pinout

Table 4-2. SAM4N8/16 100-lead LQFP Pinout

1	ADVREFP	26	GND	51	TDI/PB4	76	TDO/TRACESWO/PB5
2	GND	27	VDDIO	52	PA6/PGMNOE	77	JTAGSEL
3	PB0/AD4	28	PA16/PGMD4	53	PA5/PGMRDY	78	PC18
4	PC29/AD13	29	PC7	54	PC28	79	TMS/SWDIO/PB6
5	PB1/AD5	30	PA15/PGMD3	55	PA4/PGMNCMD	80	PC19
6	PC30/AD14	31	PA14/PGMD2	56	VDDCORE	81	PA31
7	PB2/AD6	32	PC6	57	PA27	82	PC20
8	PC31/AD15	33	PA13/PGMD1	58	PC8	83	TCK/SWCLK/PB7
9	PB3/AD7	34	PA24	59	PA28	84	PC21
10	VDDIN	35	PC5	60	NRST	85	VDDCORE
11	VDDOUT	36	VDDCORE	61	TST	86	PC22
12	PA17/PGMD5/AD0	37	PC4	62	PC9	87	ERASE/PB12
13	PC26	38	PA25	63	PA29	88	PB10
14	PA18/PGMD6/AD1	39	PA26	64	PA30	89	PB11
15	PA21/AD8	40	PC3	65	PC10	90	PC23
16	VDDCORE	41	PA12/PGMD0	66	PA3	91	VDDIO
17	PC27	42	PA11/PGMM3	67	PA2/PGMEN2	92	PC24
18	PA19/PGMD7/AD2	43	PC2	68	PC11	93	PB13/DAC0
19	PC15/AD11	44	PA10/PGMM2	69	VDDIO	94	PC25
20	PA22/AD9	45	GND	70	GND	95	GND
21	PC13/AD10	46	PA9/PGMM1	71	PC14	96	PB8/XOUT
22	PA23	47	PC1	72	PA1/PGMEN1	97	PB9/PGMCK/XIN
23	PC12/AD12	48	PA8/XOUT32/PGMM0	73	PC16	98	VDDIO
24	PA20/AD3	49	PA7/XIN32/PGMNVALID	74	PA0/PGMEN0	99	PB14
25	PC0	50	VDDIO	75	PC17	100	VDDPLL

Table 4-3. SAM4N8/16 100-ball TFBGA Pinout

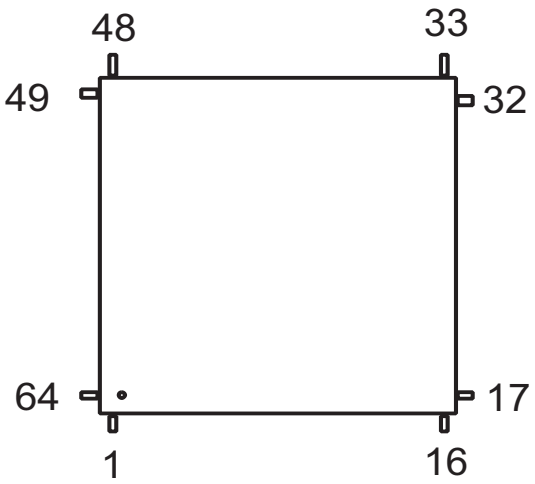
A1	PB1/AD5	C6	TCK/SWCLK/PB7	F1	PA18/PGMD6/AD1	H6	PC4
A2	PC29/AD13	C7	PC16	F2	PC26	H7	PA11/PGMM3
A3	VDDIO	C8	PA1/PGMEN1	F3	VDDOUT	H8	PC1
A4	PB9/PGMCK/XIN	C9	PC17	F4	GND	H9	PA6/PGMNOE
A5	PB8/XOUT	C10	PA0/PGMEN0	F5	VDDIO	H10	TDI/PB4
A6	PB13/DAC0	D1	PB3/AD7	F6	PA27	J1	PC15/AD11
A7	PB11	D2	PB0/AD4	F7	PC8	J2	PC0
A8	PB10	D3	PC24	F8	PA28	J3	PA16/PGMD4
A9	TMS/SWDIO/PB6	D4	PC22	F9	TST	J4	PC6
A10	JTAGSEL	D5	GND	F10	PC9	J5	PA24
B1	PC30	D6	GND	G1	PA21/AD8	J6	PA25
B2	ADVREFP	D7	VDDCORE	G2	PC27	J7	PA10/PGMM2
B3	GND	D8	PA2/PGMEN2	G3	PA15/PGMD3	J8	GND
B4	PB14	D9	PC11	G4	VDDCORE	J9	VDDCORE
B5	PC21	D10	PC14	G5	VDDCORE	J10	VDDIO
B6	PC20	E1	PA17/PGMD5/ AD0	G6	PA26	K1	PA22/AD9
B7	PA31	E2	PC31	G7	PA12/PGMD0	K2	PC13/AD10
B8	PC19	E3	VDDIN	G8	PC28	K3	PC12/AD12
B9	PC18	E4	GND	G9	PA4/PGMNCMD	K4	PA20/AD3
B10	TDO/TRACESWO/ PB5	E5	GND	G10	PA5/PGMRDY	K5	PC5
C1	PB2/AD6	E6	NRST	H1	PA19/PGMD7/ AD2	K6	PC3
C2	VDDPLL	E7	PA29	H2	PA23	K7	PC2
C3	PC25	E8	PA30/AD14	H3	PC7	K8	PA9/PGMM1
C4	PC23	E9	PC10	H4	PA14/PGMD2	K9	PA8/XOUT32/ PGMM0
C5	ERASE/PB12	E10	PA3	H5	PA13/PGMD1	K10	PA7/XIN32/ PGMNVALID

Table 4-4. SAM4N8/16 100-ball VFBGA Pinout

A1	ADVREFP	C6	PC9	F1	VDDOUT	H6	PA12/PGMD0
A2	VDDPLL	C7	TMS/SWDIO/PB6	F2	PA18/PGMD6/AD1	H7	PA9/PGMM1
A3	PB9/PGMCK/XIN	C8	PA1/PGMEN1	F3	PA17/PGMD5/AD0	H8	VDDCORE
A4	PB8/XOUT	C9	PA0/PGMEN0	F4	GND	H9	PA6/PGMNOE
A5	JTAGSEL	C10	PC16	F5	GND	H10	PA5/PGMRDY
A6	PB11	D1	PB1/AD5	F6	PC26	J1	PA20/AD3
A7	PB10	D2	PC30	F7	PA4/PGMNCMD	J2	PC12/AD12
A8	PC20	D3	PC31	F8	PA28	J3	PA16/PGMD4
A9	PC19	D4	PC22	F9	TST	J4	PC6
A10	TDO/TRACESWO/ PB5	D5	PC5	F10	PC8	J5	PA24
B1	GND	D6	PA29	G1	PC15/AD11	J6	PA25
B2	PC25	D7	PA30/AD14	G2	PA19/PGMD7/AD2	J7	PA11/PGMM3
B3	PB14	D8	GND	G3	PA21/PGMD9/AD8	J8	VDDCORE
B4	PB13/DAC0	D9	PC14	G4	PA15/PGMD3	J9	VDDCORE
B5	PC23	D10	PC11	G5	PC3	J10	TDI/PB4
B6	PC21	E1	VDDIN	G6	PA10/PGMM2	K1	PA23
B7	TCK/SWCLK/PB7	E2	PB3/AD7	G7	PC1	K2	PC0
B8	PA31	E3	PB2/AD6	G8	PC28	K3	PC7
B9	PC18	E4	GND	G9	NRST	K4	PA13/PGMD1
B10	PC17	E5	GND	G10	PA27	K5	PA26
C1	PB0/AD4	E6	GND	H1	PC13/AD10	K6	PC2
C2	PC29/AD13	E7	VDDIO	H2	PA22/AD9	K7	VDDIO
C3	PC24	E8	PC10	H3	PC27	K8	VDDIO
C4	ERASE/PB12	E9	PA2/PGMEN2	H4	PA14/PGMD2	K9	PA8/XOUT32/ PGMM0
C5	VDDCORE	E10	PA3	H5	PC4	K10	PA7/XIN32/ PGMNVALID

4.5 Overview of the 64-lead LQFP Package

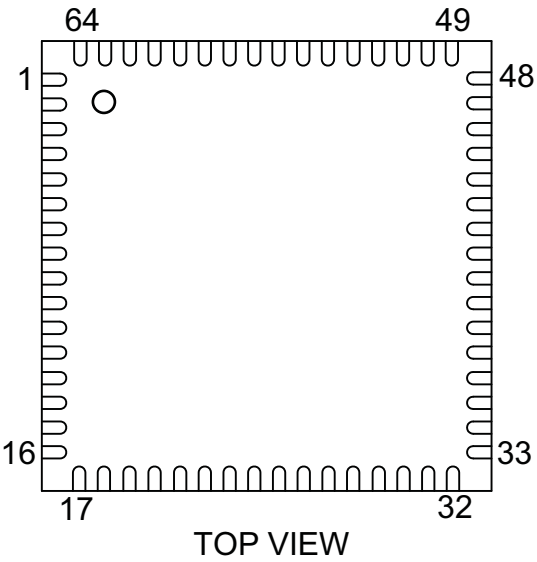
Figure 4-4. Orientation of the 64-lead LQFP Package



Refer to Section 37. “SAM4N Mechanical Characteristics” for mechanical drawings and specifications.

4.6 Overview of the 64-lead QFN Package

Figure 4-5. Orientation of the 64-lead QFN Package



Refer to Section 37. “SAM4N Mechanical Characteristics” for mechanical drawings and specifications.

4.7 64-lead LQFP and QFN Pinout

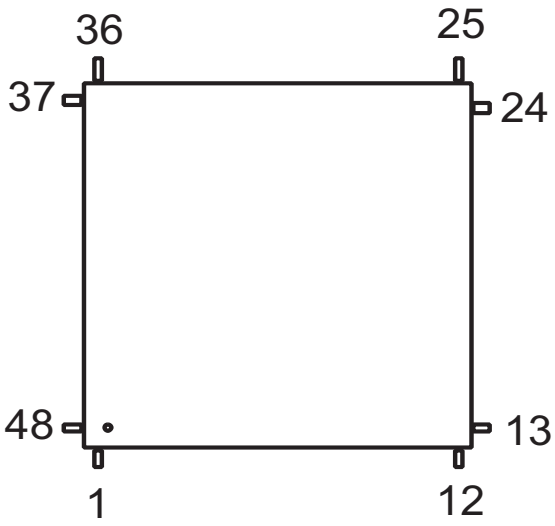
Table 4-5. 64-pin SAM4N8/16 Pinout

1	ADVREFP	17	GND	33	TDI/PB4	49	TDO/TRACESWO/PB5
2	GND	18	VDDIO	34	PA6/PGMNOE	50	JTAGSEL
3	PB0/AD4	19	PA16/PGMD4	35	PA5/PGMRDY	51	TMS/SWDIO/PB6
4	PB1/AD5	20	PA15/PGMD3	36	PA4/PGMNCMD	52	PA31
5	PB2/AD6	21	PA14/PGMD2	37	PA27/PGMD15	53	TCK/SWCLK/PB7
6	PB3/AD7	22	PA13/PGMD1	38	PA28	54	VDDCORE
7	VDDIN	23	PA24/PGMD12	39	NRST	55	ERASE/PB12
8	VDDOUT	24	VDDCORE	40	TST	56	PB10
9	PA17/PGMD5/AD0	25	PA25/PGMD13	41	PA29	57	PB11
10	PA18/PGMD6/AD1	26	PA26/PGMD14	42	PA30	58	VDDIO
11	PA21/PGMD9/AD8	27	PA12/PGMD0	43	PA3	59	PB13/DAC0
12	VDDCORE	28	PA11/PGMM3	44	PA2/PGMEN2	60	GND
13	PA19/PGMD7/AD2	29	PA10/PGMM2	45	VDDIO	61	XOUT/PB8
14	PA22/PGMD10/AD9	30	PA9/PGMM1	46	GND	62	XIN/PGMCK/PB9
15	PA23/PGMD11	31	PA8/XOUT32/PGMM0	47	PA1/PGMEN1	63	PB14
16	PA20/PGMD8/AD3	32	PA7/XIN32/XOUT32/ PGMNVALID	48	PA0/PGMEN0	64	VDDPLL

Note: The bottom pad of the QFN package must be connected to ground.

4.8 Overview of the 48-lead LQFP Package

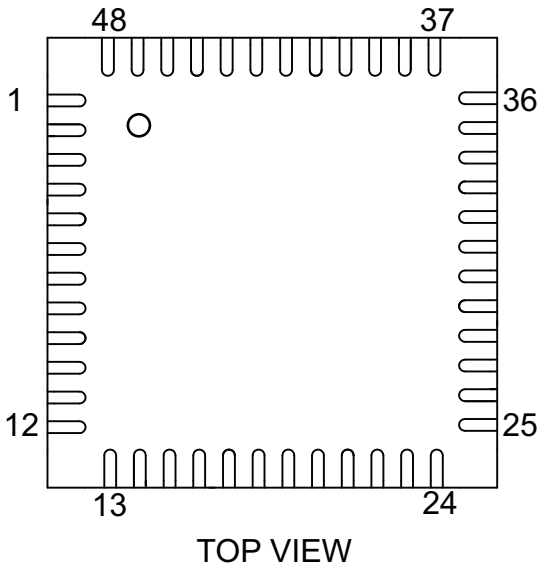
Figure 4-6. Orientation of the 48-lead LQFP Package



Refer to Section 37. “SAM4N Mechanical Characteristics” for mechanical drawings and specifications.

4.9 Overview of the 48-lead QFN Package

Figure 4-7. Orientation of the 48-lead QFN Package



Refer to Section 37. “SAM4N Mechanical Characteristics” for mechanical drawings and specifications.

4.10 48-lead LQFP and QFN Pinout

Table 4-6. 48-pin SAM4N8 Pinout

1	ADVREFP	13	VDDIO	25	TDI/PB4	37	TDO/TRACESWO/PB5
2	GND	14	PA16/PGMD4	26	PA6/PGMNOE	38	JTAGSEL
3	PB0/AD4	15	PA15/PGMD3	27	PA5/PGMRDY	39	TMS/SWDIO/PB6
4	PB1/AD5	16	PA14/PGMD2	28	PA4/PGMNCMD	40	TCK/SWCLK/PB7
5	PB2/AD6	17	PA13/PGMD1	29	NRST	41	VDDCORE
6	PB3/AD7	18	VDDCORE	30	TST	42	ERASE/PB12
7	VDDIN	19	PA12/PGMD0	31	PA3	43	PB10
8	VDDOUT	20	PA11/PGMM3	32	PA2/PGMEN2	44	PB11
9	PA17/PGMD5/AD0	21	PA10/PGMM2	33	VDDIO	45	XOUT/PB8
10	PA18/PGMD6/AD1	22	PA9/PGMM1	34	GND	46	XIN/P/PB9/GMCK
11	PA19/PGMD7/AD2	23	PA8/XOUT32/PGMM0	35	PA1/PGMEN1	47	VDDIO
12	PA20/AD3	24	PA7/XIN32/PGMNVALID	36	PA0/PGMEN0	48	VDDPLL

Note: The bottom pad of the QFN package must be connected to ground.

5. Power Considerations

5.1 Power Supplies

The SAM4N8/16 product has several types of power supply pins:

- VDDCORE pins: power the core, including the processor, the embedded memories and the peripherals; voltage ranges from 1.08V to 1.32V.
- VDDIO pins: power the Peripherals I/O lines; voltage ranges from 1.62V to 3.6V.
- VDDIN pin: Voltage Regulator, ADC and DAC power supply; voltage ranges from 1.6V to 3.6V for Voltage Regulator, ADC and DAC.
- VDDPLL pin: powers the Main Oscillator; voltage ranges from 1.08V to 1.32V.

5.2 Power-up Considerations

5.2.1 VDDIO Versus VDDCORE

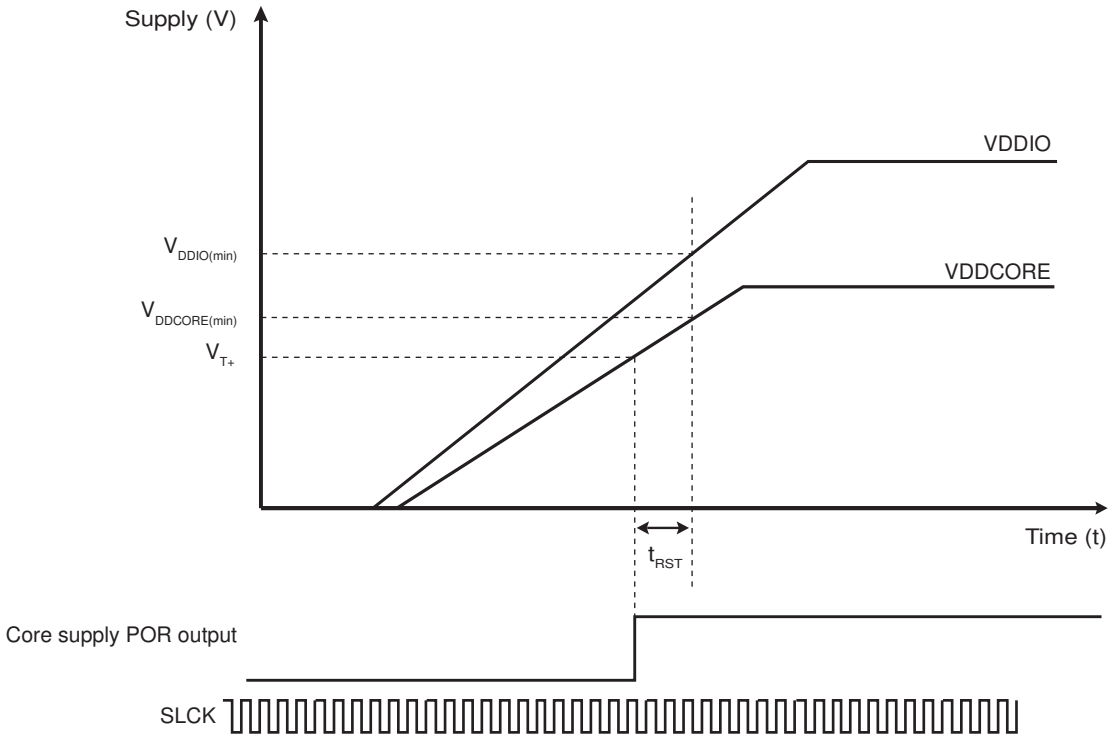
V_{DDIO} must always be higher than or equal to V_{DDCORE}.

V_{DDIO} must reach its minimum operating voltage (1.62 V) before V_{DDCORE} has reached $V_{DDCORE(min)}$. The minimum slope for V_{DDCORE} is defined by ($V_{DDCORE(min)}$ - V_{T+}) / t_{RST}.

If V_{DDCORE} rises at the same time as V_{DDIO}, the V_{DDIO} rising slope must be higher than or equal to 8.8 V/ms.

If VDDCORE is powered by the internal regulator, all power-up considerations are met

Figure 5-1. VDDCORE and VDDIO Constraints at Startup



5.2.2 VDDIO Versus VDDIN

At power-up, V_{DDIO} needs to reach 0.6 V before V_{DDIN} reaches 1.0 V.

VDDIO voltage needs to be equal to or below (VDDIN voltage + 0.5 V).

5.3 Voltage Regulator

The SAM4N embeds a core voltage regulator that is managed by the Supply Controller and that supplies the Cortex-M4 core, internal memories (SRAM, ROM and Flash logic) and the peripherals. An internal adaptive biasing adjusts the regulator quiescent current depending on the required load current.

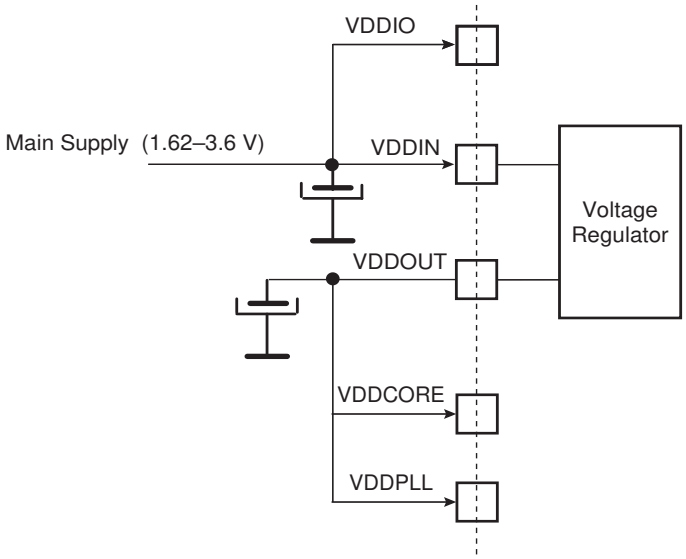
For adequate input and output power supply decoupling/bypassing, refer to Table 36-3, “1.2V Voltage Regulator Characteristics,” on page 795.

5.4 Typical Powering Schematics

The SAM4N8/16 supports a 1.62–3.6 V single supply mode. The internal regulator input connected to the source and its output feeds VDDCORE. Figure 5-2 shows the power schematics.

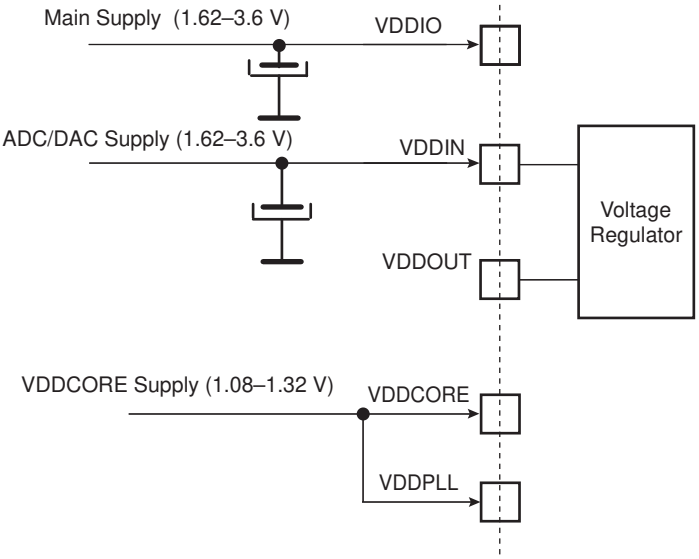
As VDDIN powers voltage regulator and ADC/DAC, when the user does not want to use the embedded voltage regulator, he can disable it by software via the SUPC (note that it is different from backup mode).

Figure 5-2. Single Supply



Note: For temperature sensor, VDDIO needs to be greater than 2.4V.

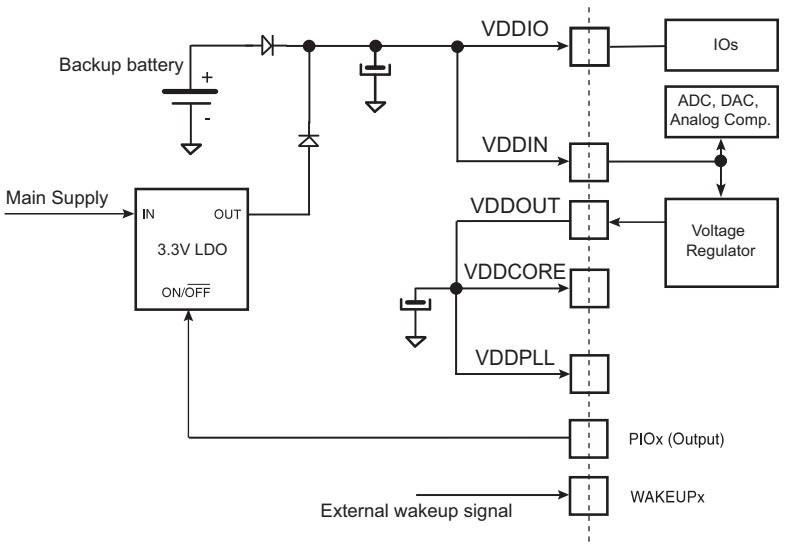
Figure 5-3. Core Externally Supplied



Note: For temperature sensor, VDDIO needs to be greater than 2.4V.

Figure 5-4 provides an example of the powering scheme when using a backup battery. Since the PIO state is preserved when in backup mode, any free PIO line can be used to switch off the external regulator by driving the PIO line at low level (PIO is input, pull-up enabled after backup reset). External wake-up of the system can be from a push button or any signal, see Section 5.7 “Wake-up Sources” for further details.

Figure 5-4. Core Externally Supplied (Backup Battery)



Note: The two diodes provide a “switchover circuit (for illustration purpose) between the backup battery and the main supply when the system is put in backup mode.

Note: For temperature sensor, VDDIO needs to be greater than 2.4V.

5.5 Active Mode

Active mode is the normal running mode with the core clock running from the fast RC oscillator, the main crystal oscillator or the PLL. The power management controller can be used to adapt the frequency and to disable the peripheral clocks.

5.6 Low-power Modes

The SAM4N has the following low-power modes: Backup, Wait, and Sleep.

Note: The Wait For Event instruction (WFE) of the Cortex-M4 core can be used to enter any of the low-power modes, however, this may add complexity in the design of application state machines. This is due to the fact that the WFE instruction goes along with an event flag of the Cortex core (cannot be managed by the software application). The event flag can be set by interrupts, a debug event or an event signal from another processor. Since it is possible for an interrupt to occur just before the execution of WFE, WFE takes into account events that happened in the past. As a result, WFE prevents the device from entering Wait mode if an interrupt event has occurred.
Atmel has made provisions to avoid using the WFE instruction. The workarounds to ease application design are as follows:
- For Backup mode, switch off the voltage regulator and configure the VROFF bit in the Supply Controller Control Register (SUPC_CR).
- For Wait mode, configure the WAITMODE bit in the PMC Clock Generator Main Oscillator Register of the Power Management Controller (PMC)
- For Sleep mode, use the Wait for Interrupt (WFI) instruction.

Complete information is available in Table 5-1 “Low Power Mode Configuration Summary”.

5.6.1 Backup Mode

The purpose of Backup mode is to achieve the lowest power consumption possible in a system which is performing periodic wake-ups to perform tasks but not requiring fast startup time. Total current consumption is 1 µA typical (VDDIO = 1.8V at 25°C).

The Supply Controller, zero-power power-on reset, RTT, RTC, backup registers and 32 kHz oscillator (RC or crystal oscillator selected by software in the Supply Controller) are running. The regulator and the core supply are off.

The SAM4N can be awakened from this mode using the pins WKUP0–15, the supply monitor (SM), the RTT or RTC wake-up event.

Backup mode can be entered by using the VROFF bit in the Supply Controller Control Register (SUPC_CR) or by using the WFE instruction. The corresponding procedures are described below.

The procedure to enter Backup mode using the VROFF bit is the following:

Write a 1 to the VROFF bit in SUPC_CR (SUPC_CR.KEY field value must be configured correctly; refer to Section 17.5.3 “Supply Controller Control Register”).

The procedure to enter Backup mode using the WFE instruction is the following:

1. Write a 1 to the SLEEPDEEP bit in the Cortex-M4 processor System Control Register (SBC_SCR) (refer to Section 11.9.1.6 “System Control Register”).
2. Execute the WFE instruction of the processor.

In both cases, exit from Backup mode happens if one of the following enable wake-up events occurs:

- Level transition, configurable debouncing on pins WKUPEN0–15
- Supply Monitor alarm
- RTC alarm
- RTT alarm

5.6.2 Wait Mode

The purpose of the Wait mode is to achieve very low power consumption while maintaining the whole device in a powered state for a startup time of less than 10 µs. Current consumption in wait mode is typically 32 µA (total current consumption) if the internal voltage regulator is used.

In this mode, the clocks of the core, peripherals and memories are stopped. However, the core, peripherals and memories power supplies are still powered. From this mode, a fast startup is available.

This mode is entered by setting the WAITMODE bit in the PMC Clock Generator Main Oscillator Register (CKGR_MOR) in conjunction with configuring the Flash Low Power Mode field (FLPM = 00 or 01) in the PMC Fast Startup Mode Register (PMC_FSMR) or by the WFE instruction.

The Cortex-M4 is able to handle external events or internal events in order to wake up the core. This is done by configuring the external lines WKUP0–15 as fast startup wake-up pins (refer to Section 5.8 “Fast Startup”). RTC or RTT alarm can be used to wake up the CPU.

The procedure to enter Wait mode using the WAITMODE bit is the following:

1. Select the 4/8/12 MHz fast RC oscillator as source of MCK Clock
2. Configure the FLPM field in PMC_FSMR
3. Set Flash wait state to 0
4. Set the WAITMODE bit in CKGR_MOR
5. Wait for Master Clock Ready MCKRDY = 1 in the PMC Status Register (PMC_SR)

The procedure to enter Wait mode using the WFE instruction is the following:

1. Select the 4/8/12 MHz fast RC oscillator as Main Clock.
2. Set the FLPM field in the PMC_FSMR.
3. Set Flash wait state to 0.
4. Set the LPM bit in the PMC_FSMR.
5. Execute the WFE instruction of the processor.

In both cases, depending on the value of the field FLPM, the Flash enters one of three different modes:

- FLPM = 0 in Standby mode (low consumption)
- FLPM = 1 in Deep power-down mode (extra low consumption)
- FLPM = 2 in Idle mode. Memory ready for Read access

Table 5-1 summarizes the power consumption, wake-up time and system state in Wait mode.

5.6.3 Sleep Mode

The purpose of Sleep mode is to optimize power consumption of the device versus response time. In this mode, only the core clock is stopped. The peripheral clocks can be enabled. The current consumption in this mode is application dependent.

This mode is entered via WFI or WFE instructions with bit LPM = 0 in PMC_FSMR.

The processor can be awakened from an interrupt if the WFI instruction of the Cortex-M4 is used or from an event if the WFE instruction is used.

5.6.4 Low Power Mode Summary Table

The modes detailed above are the main low power modes. Each part can be set to on or off separately and wake-up sources can be individually configured. Table 5-1 shows a summary of the configurations of the low power modes.

Table 5-1. Low Power Mode Configuration Summary

Mode	SUPC, 32 kHz Osc., RTC, RTT, GPBR, POR (VDDBU Region)	Regulator	Core Memory Peripherals	Mode Entry	Potential Wake-up Sources	Core at Wake-up	PIO State while in Low-power Mode	PIO State at Wake-up	Consumption (2) (3)	Wake-up Time(1)
Backup Mode	ON	OFF	OFF (Not powered)	VROFF = 1 or WFE + SLEEPDEEP = 1	Pins WKUP0–15 SM alarm RTC alarm RTT alarm	Reset	Previous state saved	PIOA & PIOB & PIOC Inputs with pull-ups	0.9 µA typ(4)	< 1 ms
Wait Mode w/Flash in Standby Mode	ON	ON	Powered (Not clocked)	WAITMODE = 1 + FLPM = 0 or WFE + SLEEPDEEP = 0 + LPM = 1 + FLPM = 0	Any event from: - Fast startup through pins WKUP0–15 - RTC alarm - RTT alarm	Clocked back	Previous state saved	Unchanged	28.4 µA(5)	< 10 µs
Wait Mode w/Flash in Deep Power Down Mode	ON	ON	Powered (Not clocked)	WAITMODE = 1 + FLPM = 1 or WFE + SLEEPDEEP = 0 + LPM = 1 + FLPM = 1	Any event from: - Fast startup through pins WKUP0–15 - RTC alarm - RTT alarm	Clocked back	Previous state saved	Unchanged	23.9 µA(5)	< 100 µs
Sleep Mode	ON	ON	Powered(7) (Not clocked)	WFE or WFI + SLEEPDEEP = 0 + LPM = 0	Entry mode = WFI Interrupt only; any enabled interrupt Entry mode = WFE Any enabled interrupt and/or any event from: - Fast startup through pins WKUP0–15 - RTC alarm - RTT alarm	Clocked back	Previous state saved	Unchanged	(6)	(6)

Notes:
1. When considering wake-up time, the time required to start the PLL is not taken into account. Once started, the device works with the 4/8/12 MHz fast RC oscillator. The user has to add the PLL startup time if it is needed in the system. The wake-up time is defined as the time taken for wake-up until the first instruction is fetched.
2. The external loads on PIOs are not taken into account in the calculation.
3. BOD current consumption is not included.
4. Total consumption 0.9 µA typ at 1.8V on VDDIO at 25°C.
5. Total consumption (VDDIO + VDDIN)
6. Depends on MCK frequency.
7. In this mode the core is supplied and not clocked but some peripherals can be clocked.

5.7 Wake-up Sources

The wake-up events allow the device to exit the Backup mode. When a wake-up event is detected, the Supply Controller performs a sequence which automatically reenables the core power supply and the SRAM power supply, if they are not already enabled. See Figure 17-4, "Wake-up Sources" on page 311.

5.8 Fast Startup

The SAM4N8/16 allows the processor to restart in a few microseconds while the processor is in Wait mode. A fast startup can occur upon detection of a low level on one of the 18 wake-up inputs (WKUP0 to 15 + RTC + RTT).

The fast restart circuitry (shown in Figure 25-3, "Fast Start-up Circuitry" on page 401) is fully asynchronous and provides a fast startup signal to the Power Management Controller. As soon as the fast startup signal is asserted, the PMC automatically restarts the embedded 4/18/12 MHz fast RC oscillator, switches the master clock on this 4 MHz clock by default and reenables the processor clock.

6. Input/Output Lines

The SAM4N8/16 has several kinds of input/output (I/O) lines such as general purpose I/Os (GPIO) and system I/Os. GPIOs can have alternate functionality due to multiplexing capabilities of the PIO controllers. The same PIO line can be used whether in I/O mode or by the multiplexed peripheral. System I/Os include pins such as test pins, oscillators, erase or analog inputs.

6.1 General Purpose I/O Lines

GPIO lines are managed by PIO controllers. All I/Os have several input or output modes such as pull-up or pull-down, input Schmitt triggers, multi-drive (open-drain), glitch filters, debouncing or input change interrupt. Programming of these modes is performed independently for each I/O line through the PIO controller user interface. For more details, refer to Section 27. “Parallel Input/Output (PIO) Controller”.

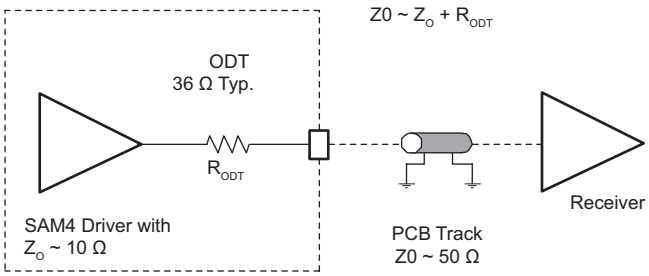
Some GPIOs can have alternate function as analog input. When the GPIO is set in analog mode, all digital features of the I/O are disabled.

The input/output buffers of the PIO lines are supplied through VDDIO power supply rail.

The SAM4N8/16 embeds high-speed pads. See Section 36.10 “AC Characteristics” for more details.

Each I/O line also embeds an ODT (On-Die Termination) (see Figure 6-1). It consists of an internal series resistor termination scheme for impedance matching between the driver output (SAM4N) and the PCB track impedance, preventing signal reflection. The series resistor helps to reduce IOs switching current (di/dt) thereby reducing in turn, EMI. It also decreases overshoot and undershoot (ringing) due to inductance of interconnect between devices or between boards. In conclusion, ODT helps diminish signal integrity issues.

Figure 6-1. On-die Termination



6.2 System I/O Lines

Table 6-1 lists the SAM4N system I/O lines shared with PIO lines.

These pins are software configurable as general purpose I/O or system pins. At startup, the default function of these pins is always used.

Table 6-1. System I/O Configuration

CCFG_SYSIO Bit No.	Default Function after Reset	Other Function	Constraints for Normal Start	Configuration
12	ERASE	PB12	Low level at startup(1)	In Matrix User Interface Registers (Refer to System I/O Configuration Register in Section 22. “Bus Matrix (MATRIX)”.)
7	TCK/SWCLK	PB7	–	
6	TMS/SWDIO	PB6	–	
5	TDO/TRACESWO	PB5	–	
4	TDI	PB4	–	
–	PA7	XIN32	–	(2)
–	PA8	XOUT32	–	
–	PB9	XIN	–	(3)
–	PB8	XOUT	–	

Notes:
1. If PB12 is used as PIO input in user applications, a low level must be ensured at startup to prevent Flash erase before the user application sets PB12 into PIO mode.
2. Refer to Section 17.4.2 “Slow Clock Generator”.
3. Refer to Section 24.5.3 “3 to 20 MHz Crystal or Ceramic Resonator-based Oscillator”.

6.2.1 Serial Wire JTAG Debug Port (SWJ-DP) Pins

The SWJ-DP pins are TCK/SWCLK, TMS/SWDIO, TDO/TRACESWO, TDI and commonly provided on a standard 20-pin JTAG connector defined by ARM. For more details about voltage reference and reset state, refer to Table 3-1 on page 5.

At startup, SWJ-DP pins are configured in SWJ-DP mode to allow connection with debugging probe. Please refer to Section 12. “Debug and Test Features”.

SWJ-DP pins can be used as standard I/Os to provide users more general input/output pins when the debug port is not needed in the end application. Mode selection between SWJ-DP mode (system IO mode) and general IO mode is performed through the AHB Matrix Special Function Registers (MATRIX_SFR). Configuration of the pad for pull-up, triggers, debouncing and glitch filters is possible regardless of the mode.

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level. It integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations.

By default, the JTAG Debug Port is active. If the debugger host wants to switch to the Serial Wire Debug Port, it must provide a dedicated JTAG sequence on TMS/SWDIO and TCK/SWCLK which disables the JTAG-DP and enables the SW-DP. When the Serial Wire Debug Port is active, TDO/TRACESWO can be used for trace.

The asynchronous TRACE output (TRACESWO) is multiplexed with TDO. So the asynchronous trace can only be used with SW-DP, not JTAG-DP. For more information about SW-DP and JTAG-DP switching, please refer to Section 12. “Debug and Test Features”.

6.3 Test Pin

The TST pin is used for JTAG Boundary Scan Manufacturing Test or Fast Flash programming mode of the SAM4N series. The TST pin integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations. To enter fast programming mode, see Section 20. “Fast Flash Programming Interface (FFPI)”. For more on the manufacturing and test mode, refer to Section 12. “Debug and Test Features”.