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SAM4S Series

Atmel | SMART ARM-based Flash MCU

DATASHEET

Description

The Atmel® | SMART SAM4S series is a member of a family of Flash microcontrollers based on the high-performance 32-bit ARM® Cortex®-M4 RISC processor. It operates at a maximum speed of 120 MHz and features up to 2048 Kbytes of Flash, with optional dual-bank implementation and cache memory, and up to 160 Kbytes of SRAM. The peripheral set includes a full-speed USB Device port with embedded transceiver, a high-speed MCI for SDIO/SD/MMC, an External Bus Interface featuring a Static Memory Controller to connect to SRAM, PSRAM, NOR Flash, LCD Module and NAND Flash, 2 USARTs, 2 UARTs, 2 TWIs, 3 SPIs, an I2S, as well as a PWM timer, two 3-channel general-purpose 16-bit timers (with stepper motor and quadrature decoder logic support), an RTC, a 12-bit ADC, a 12-bit DAC and an analog comparator.

The SAM4S series is ready for capacitive touch, offering native support for the Atmel QTouch® library for easy implementation of buttons, wheels and sliders.

The Atmel | SMART SAM4S devices have three software-selectable low-power modes: Sleep, Wait and Backup. In Sleep mode, the processor is stopped while all other functions can be kept running. In Wait mode, all clocks and functions are stopped but some peripherals can be configured to wake up the system based on predefined conditions. In Backup mode, only the low-power RTC and wakeup logic are running.

The real-time event management allows peripherals to receive, react to and send events in Active and Sleep modes without processor intervention.

The SAM4S device is a medium-range general-purpose microcontroller with the best ratio in terms of reduced power consumption, processing power and peripheral set. This enables the SAM4S to sustain a wide range of applications that includes consumer, industrial control, and PC peripherals.

SAM4S devices operate from 1.62V to 3.6V.

The SAM4S series is pin-to-pin compatible with the SAM3N, SAM3S series (48-, 64- and 100-pin versions), SAM4N and SAM7S legacy series (64-pin versions).

Features

- Core
  - ARM Cortex-M4 with 2 Kbytes of cache running at up to 120 MHz
  - Memory Protection Unit (MPU)
  - DSP Instruction Set
  - Thumb®-2 instruction set
- Pin-to-pin compatible with SAM3N, SAM3S, SAM4N and SAM7S legacy products (64-pin version)
- Memories
  - Up to 2048 Kbytes embedded Flash with optional dual-bank and cache memory, ECC, Security Bit and Lock Bits
  - Up to 160 Kbytes embedded SRAM
  - 16 Kbytes ROM with embedded boot loader routines (UART, USB) and IAP routines
  - 8-bit Static Memory Controller (SMC): SRAM, PSRAM, NOR and NAND Flash support
- System
  - Embedded voltage regulator for single supply operation
  - Power-on-Reset (POR), Brown-out Detector (BOD) and Watchdog for safe operation
  - Quartz or ceramic resonator oscillators: 3 to 20 MHz main power with failure detection and optional low-power 32.768 kHz for RTC or device clock
  - RTC with Gregorian and Persian calendar mode, waveform generation in low-power modes
  - RTC counter calibration circuitry compensates for 32.768 kHz crystal frequency inaccuracy
  - High-precision 8/12 MHz factory-trimmed internal RC oscillator with 4 MHz default frequency for device startup, in-application trimming access for frequency adjustment
  - Slow clock internal RC oscillator as permanent low-power mode device clock
  - Two PLLs up to 240 MHz for device clock and for USB
  - Temperature sensor
  - Low-power tamper detection on two inputs, anti-tampering by immediate clear of general-purpose backup registers (GPBR)
  - Up to 22 Peripheral DMA (PDC) channels
- Low-power Modes
  - Sleep, Wait and Backup modes; consumption down to 1 µA in Backup mode
- Peripherals
  - USB 2.0 Device: 12 Mbps, 2668 byte FIFO, up to 8 bidirectional Endpoints, on-chip transceiver
  - Up to two USARTs with ISO7816, IrDA®, RS-485, SPI, Manchester and Modem Mode
  - Two 2-wire UARTs
  - Up to two 2-Wire Interface modules (I2C-compatible), one SPI, one Serial Synchronous Controller (I2S), one high-speed Multimedia Card Interface (SDIO/SD Card/MMC)
  - Two 3-channel 16-bit Timer Counters with capture, waveform, compare and PWM mode, Quadrature decoder logic and 2-bit Gray up/down counter for stepper motor
  - 4-channel 16-bit PWM with complementary output, fault input, 12-bit dead time generator counter for motor control
  - 32-bit Real-time Timer and RTC with calendar, alarm and 32 kHz trimming features
  - 256-bit General Purpose Backup Registers (GPBR)
  - Up to 16-channel, 1Msps ADC with differential input mode and programmable gain stage and auto calibration
  - One 2-channel 12-bit 1Msps DAC
  - One Analog Comparator with flexible input selection, selectable input hysteresis
  - 32-bit Cyclic Redundancy Check Calculation Unit (CRCCU) for data integrity check of off-/on-chip memories
  - Register Write Protection

- I/O
  - Up to 79 I/O lines with external interrupt capability (edge or level sensitivity), debouncing, glitch filtering and on-die series resistor termination
  - Three 32-bit Parallel Input/Output Controllers, Peripheral DMA-assisted Parallel Capture mode
- Packages
  - 100-lead packages
    - LQFP – 14 x 14 mm, pitch 0.5 mm
    - TFBGA – 9 x 9 mm, pitch 0.8 mm
    - VFBGA – 7 x 7 mm, pitch 0.65 mm
  - 64-lead packages
    - LQFP – 10 x 10 mm, pitch 0.5 mm
    - QFN – 9 x 9 mm, pitch 0.5 mm
    - WLCSP – 4.42 x 4.72 mm, pitch 0.4 mm (SAM4SD32/SAM4SD16)
    - WLCSP – 4.42 x 3.42 mm, pitch 0.4 mm (SAM4S16/S8)
    - WLCSP – 3.32 x 3.32 mm, pitch 0.4 mm (SAM4S4/S2)
  - 48-lead packages
    - LQFP – 7 x 7 mm, pitch 0.5 mm
    - QFN – 7 x 7 mm, pitch 0.5 mm

Safety Features Highlight

- Flash
  - Built-in ECC (hamming), single error correction
  - Security bit and lock bits

1. Configuration Summary

The SAM4S series devices differ in memory size, package and features. Table 1-1 and Table 1-2 summarize the configurations of the device family.

Table 1-1. Configuration Summary for SAM4SD32/SD16/SA16/S16 Devices

Feature	SAM4SD32C	SAM4SD32B	SAM4SD16C	SAM4SD16B	SAM4SA16C	SAM4SA16B	SAM4S16C	SAM4S16B
Flash	2 x 1024 Kbytes	2 x 1024 Kbytes	2 x 512 Kbytes	2 x 512 Kbytes	1024 Kbytes	1024 Kbytes	1024 Kbytes	1024 Kbytes
SRAM	160 Kbytes	160 Kbytes	160 Kbytes	160 Kbytes	160 Kbytes	160 Kbytes	128 Kbytes	128 Kbytes
HCACHE	2 Kbytes	2 Kbytes	2 Kbytes	2 Kbytes	2 Kbytes	2 Kbytes	–	–
Package	LQFP100 TFBGA100 VFBGA100	LQFP64 QFN64 WLCSP64	LQFP100 TFBGA100 VFBGA100	LQFP64 QFN64 WLCSP64	LQFP100 TFBGA100 VFBGA100	LQFP64 QFN64	LQFP100 TFBGA100 VFBGA100	LQFP64 QFN64 WLCSP64
Number of PIOs	79	47	79	47	79	47	79	47
External Bus Interface	8-bit data, 4 chip selects, 24-bit address	–	8-bit data, 4 chip selects, 24-bit address	–	8-bit data, 4 chip selects, 24-bit address	–	8-bit data, 4 chip selects, 24-bit address	–
12-bit ADC	16 ch.(1)	11 ch.(1)	16 ch.(1)	11 ch.(1)	16 ch.(1)	11 ch.(1)	16 ch.(1)	11 ch.(1)
12-bit DAC	2 ch.	2 ch.	2 ch.	2 ch.	2 ch.	2 ch.	2 ch.	2 ch.
Timer Counter Channels	6	6(2)	6	6(2)	6	6(2)	6	6(2)
PDC Channels	22	22	22	22	22	22	22	22
USART/UART	2/2(3)	2/2(3)	2/2(3)	2/2(3)	2/2(3)	2/2(3)	2/2(3)	2/2(3)
HSMCI	1 port, 4 bits	1 port, 4 bits	1 port, 4 bits	1 port, 4 bits	1 port, 4 bits	1 port, 4 bits	1 port, 4 bits	1 port, 4 bits

Table 1-2. Configuration Summary for SAM4S8/S4/S2 Devices

Feature	SAM4S8C	SAM4S8B	SAM4S4C	SAM4S4B	SAM4S4A	SAM4S2C	SAM4S2B	SAM4S2A
Flash	512 Kbytes	512 Kbytes	256 Kbytes	256 Kbytes	256 Kbytes	128 Kbytes	128 Kbytes	128 Kbytes
SRAM	128 Kbytes	128 Kbytes	64 Kbytes	64 Kbytes	64 Kbytes	64 Kbytes	64 Kbytes	64 Kbytes
HCACHE	–	–	–	–	–	–	–	–
Package	LQFP100 TFBGA100 VFBGA100	LQFP64 QFN64 WLCSP64	LQFP100 TFBGA100 VFBGA100	LQFP64 QFN64 WLCSP64	LQFP48 QFN48	LQFP100 TFBGA100 VFBGA100	LQFP64 QFN64 WLCSP64	LQFP48 QFN48
Number of PIOs	79	47	79	47	34	79	47	34
External Bus Interface	8-bit data, 4 chip selects, 24-bit address	–	8-bit data, 4 chip selects, 24-bit address	–	–	8-bit data, 4 chip selects, 24-bit address	–	–
12-bit ADC	16 ch.(1)	11 ch.(1)	16 ch.(1)	11 ch.(1)	8 ch.	16 ch.(1)	16 ch.(1)	8 ch
12-bit DAC	2 ch.	2 ch.	2 ch.	2 ch.	–	2 ch.	2 ch.	–
Timer Counter Channels	6	6(2)	6	6(2)	6(2)	6	6(2)	6(2)
PDC Channels	22	22	22	22	22	22	22	22
USART/UART	2/2(3)	2/2(3)	2/2(3)	2/2(3)	2/1	2/2(3)	2/2(3)	2/1
HSMCI	1 port, 4 bits	1 port, 4 bits	1 port, 4 bits	1 port, 4 bits	–	1 port, 4 bits	1 port, 4 bits	–

Notes:
1. One channel is reserved for internal temperature sensor.
2. Three TC channels are reserved for internal use.
3. Full modem support on USART1.

2. Block Diagram

Figure 2-1. SAM4SD32/SD16/SA16 100-pin Version Block Diagram

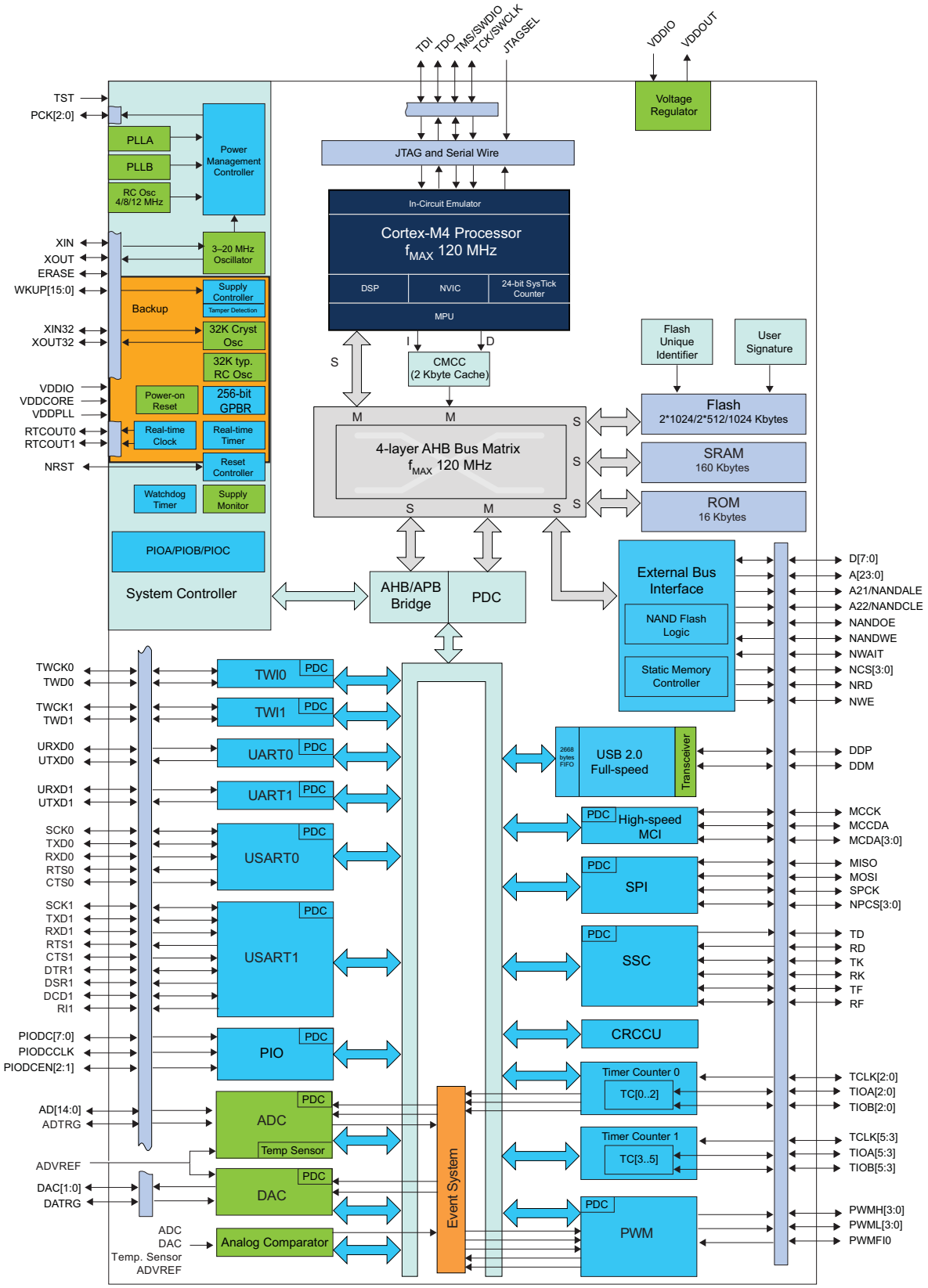


Figure 2-2. SAM4SD32/SD16/SA16 64-pin Version Block Diagram

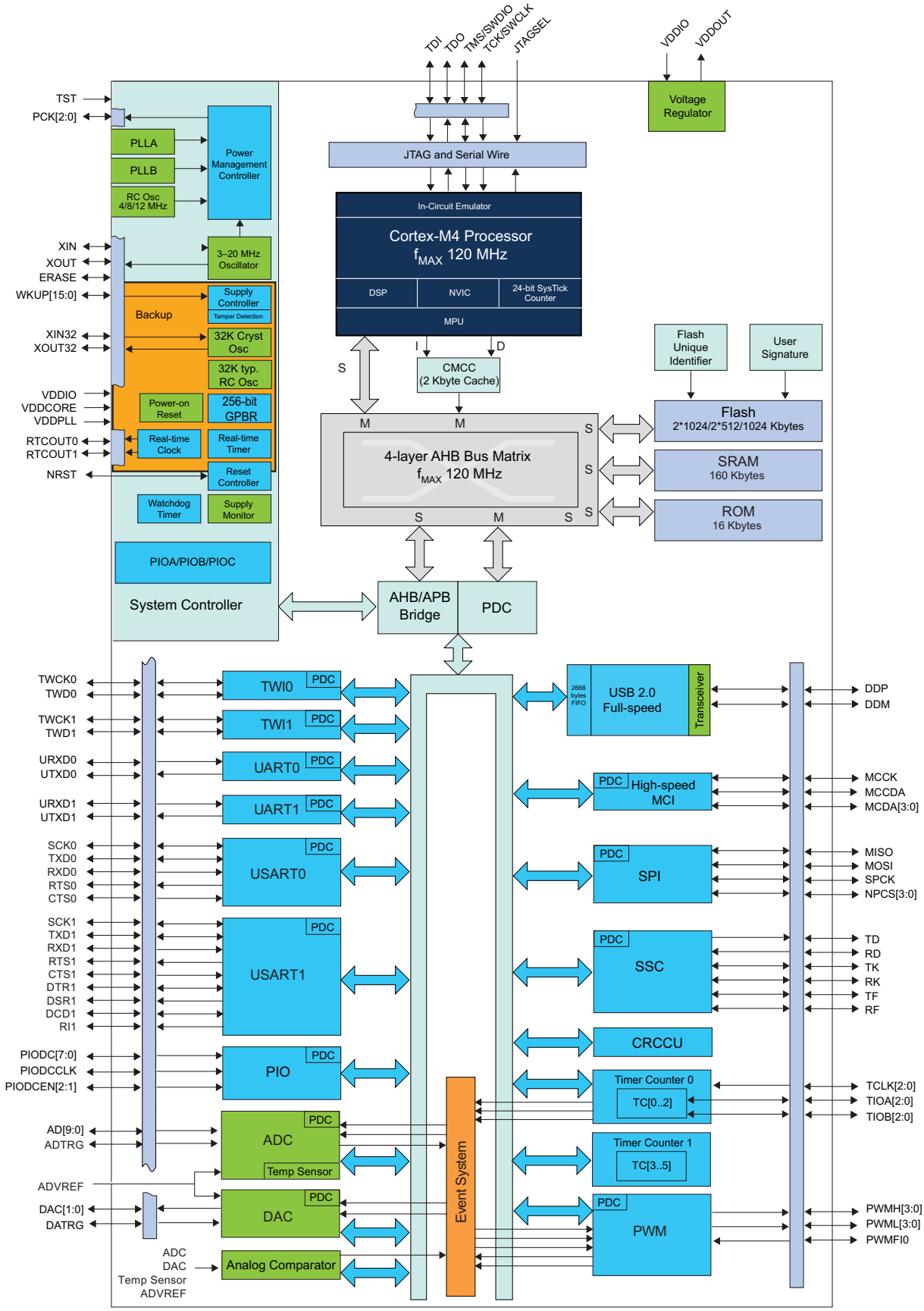


Figure 2-3. SAM4S16/S8 100-pin Version Block Diagram

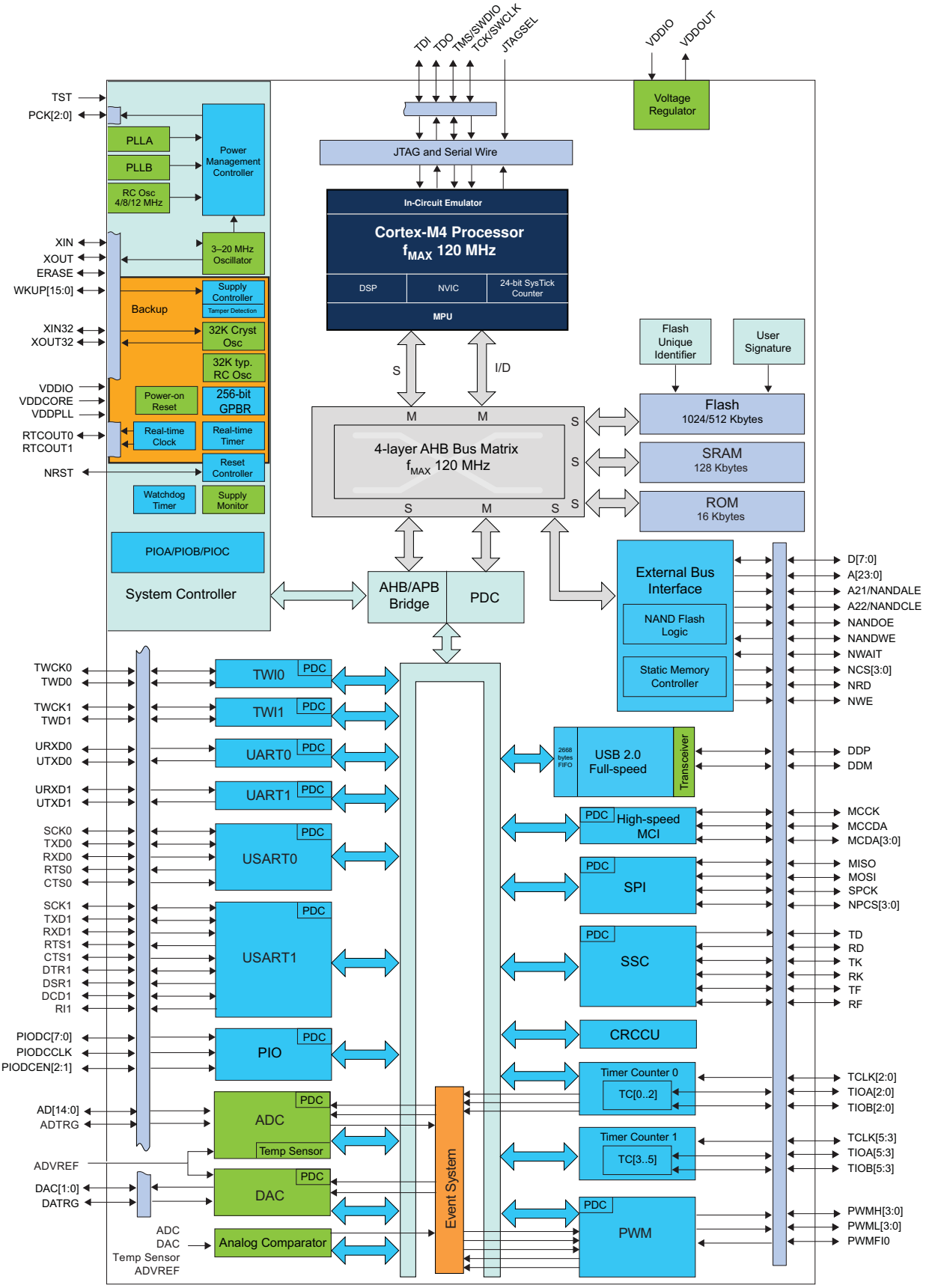


Figure 2-4. SAM4S16/S8 64-pin Version Block Diagram

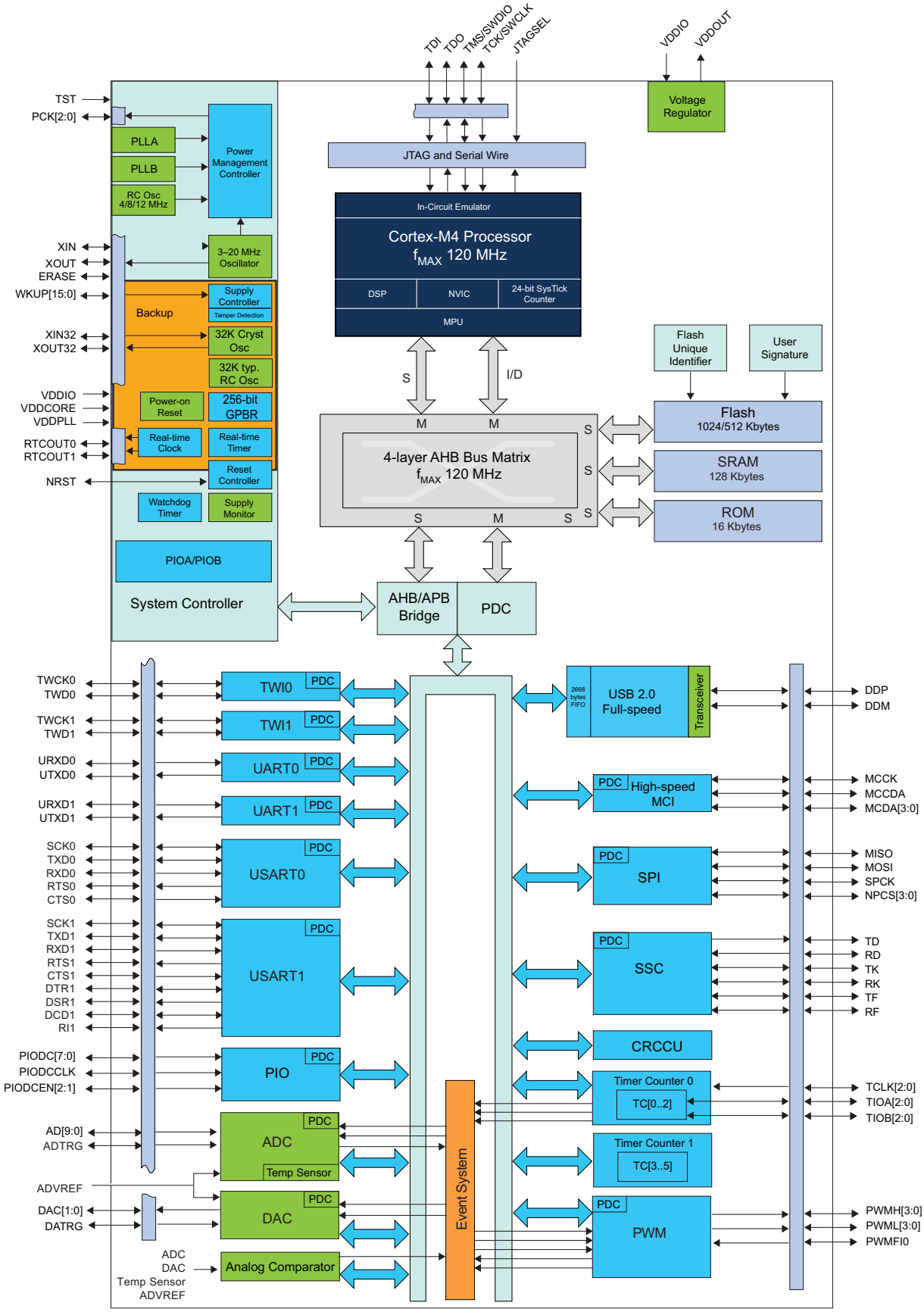


Figure 2-5. SAM4S4/S2 100-pin Version Block Diagram

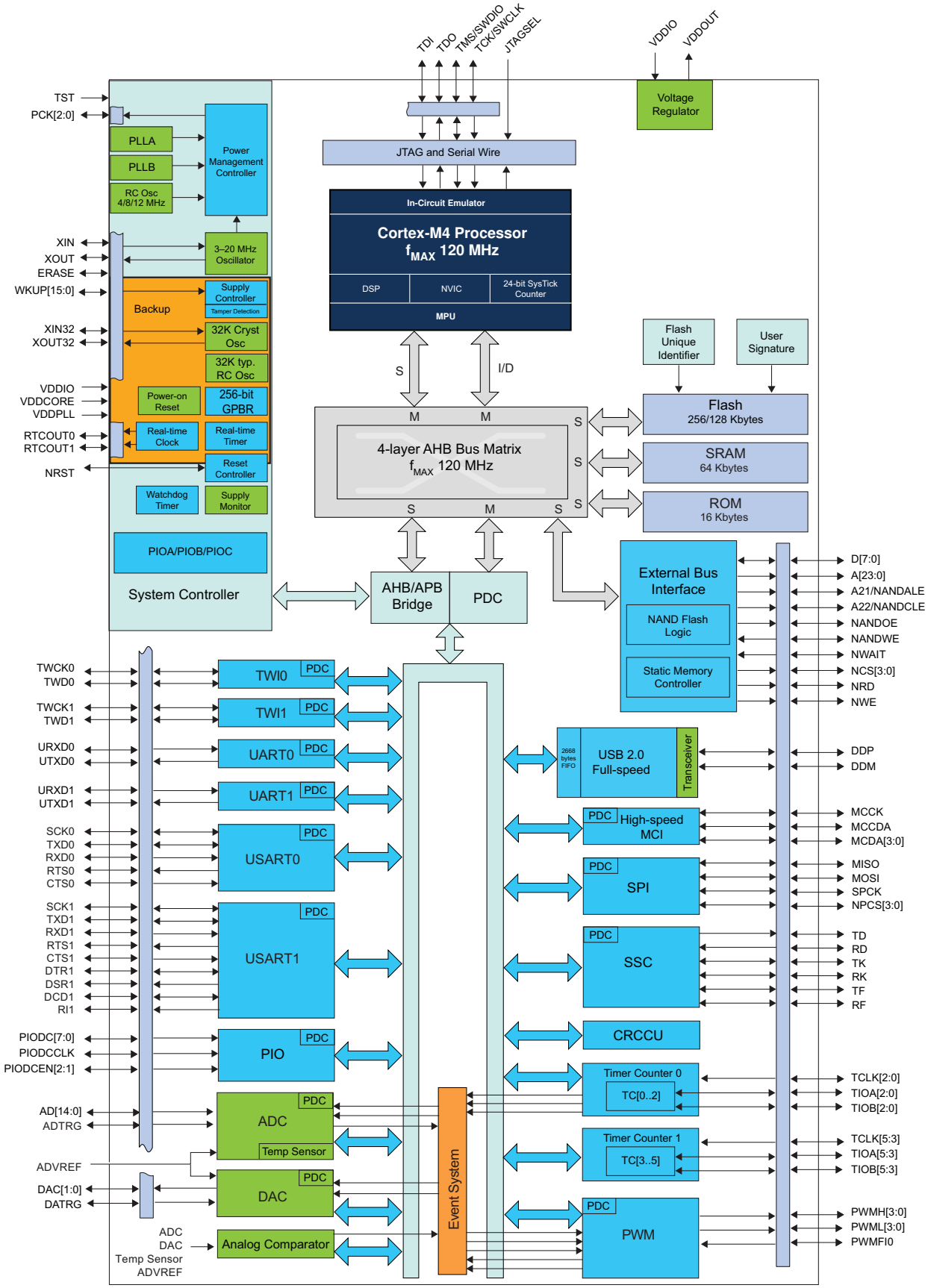


Figure 2-6. SAM4S4/S2 64-pin Version Block Diagram

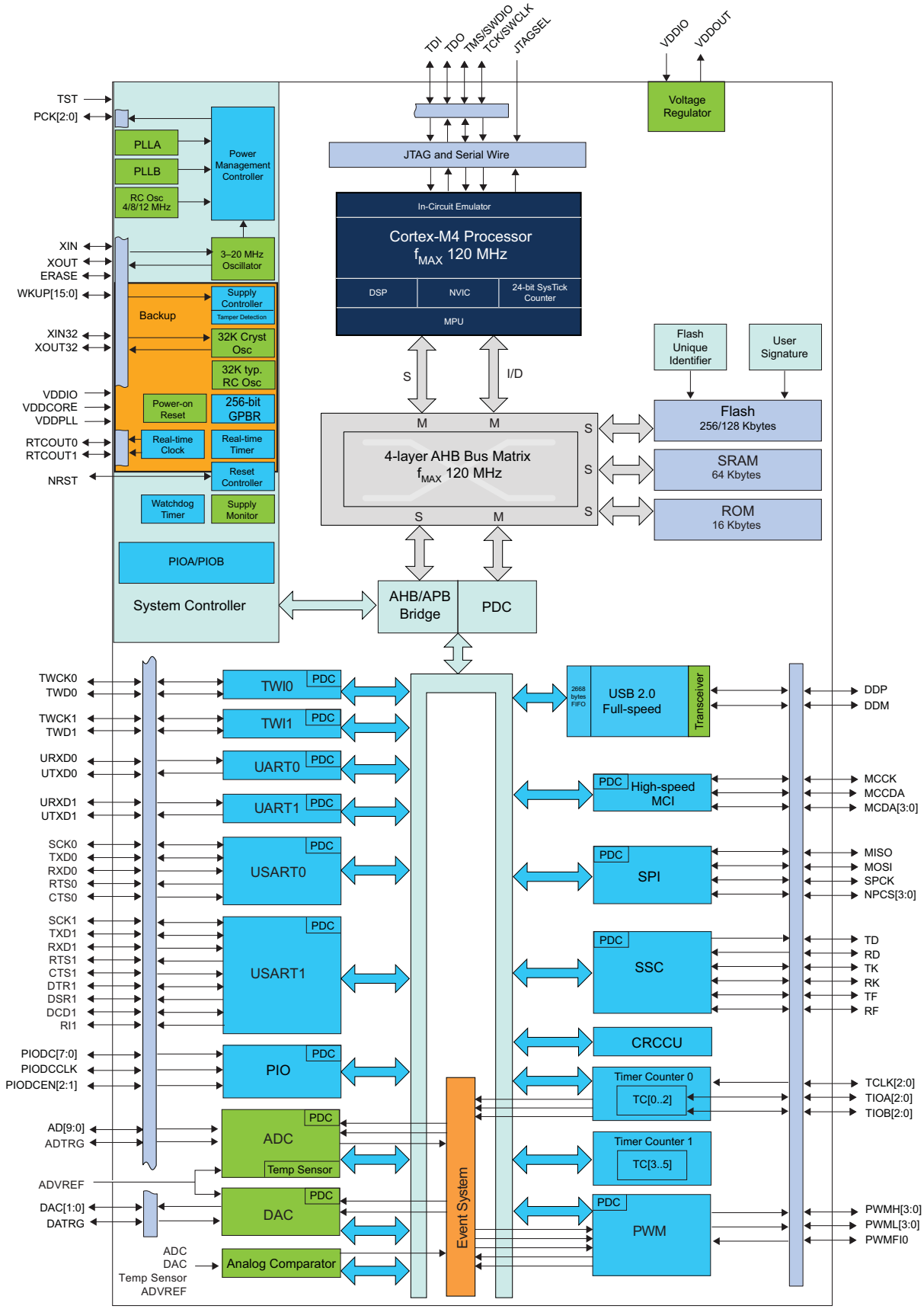
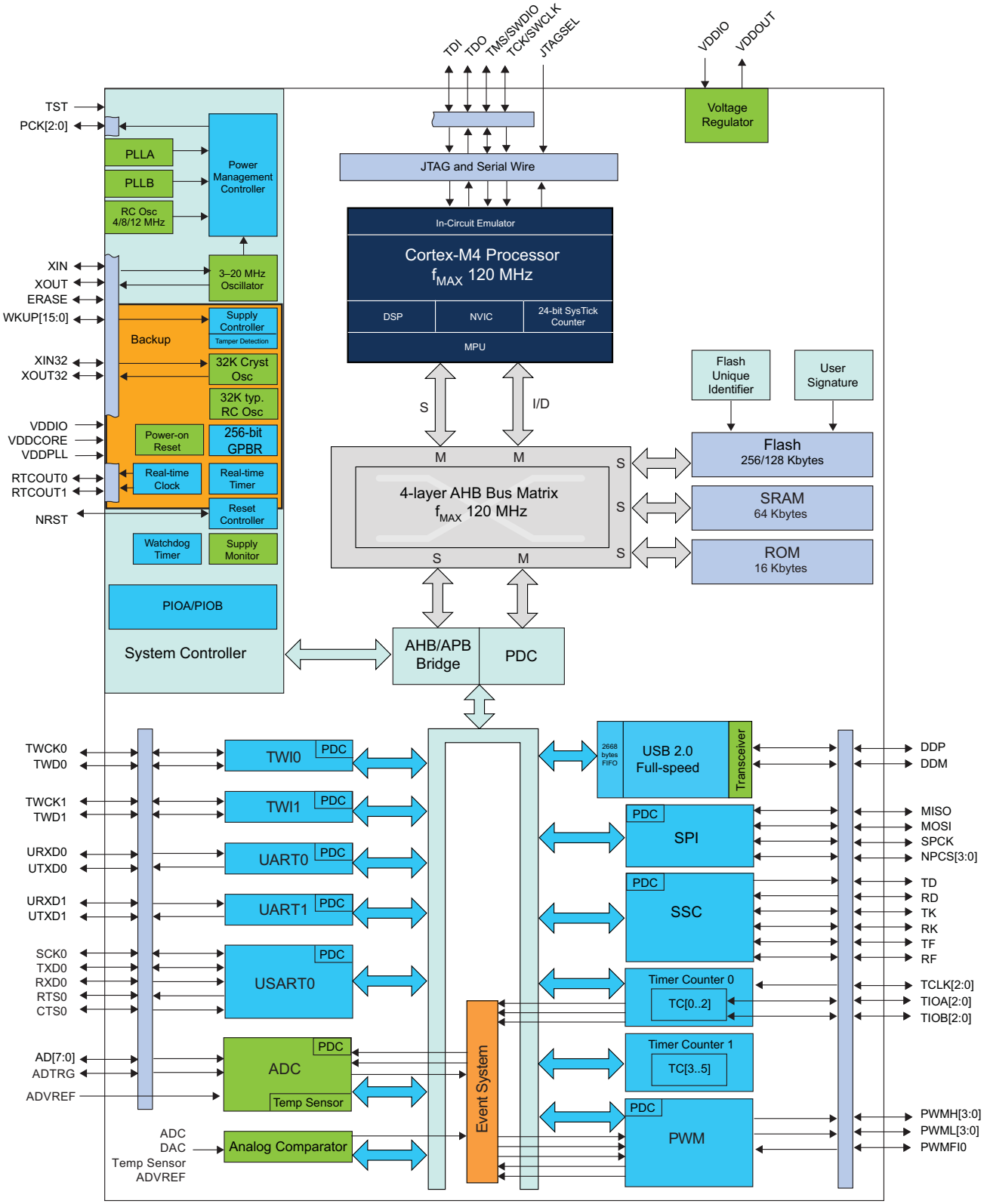


Figure 2-7. SAM4S4/S2 48-pin Version Block Diagram



3. Signal Description

Table 3-1 gives details on signal names classified by peripheral.

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Power Supplies					
VDDIO	Peripherals I/O Lines and USB transceiver Power Supply	Power	–	–	1.62V to 3.6V
VDDIN	Voltage Regulator Input, ADC, DAC and Analog Comparator Power Supply	Power	–	–	1.62V to 3.6V(4)
VDDOUT	Voltage Regulator Output	Power	–	–	1.2V output
VDDPLL	Oscillator and PLL Power Supply	Power	–	–	1.08V to 1.32V
VDDCORE	Power the core, the embedded memories and the peripherals	Power	–	–	1.08V to 1.32V
GND	Ground	Ground	–	–	–
Clocks, Oscillators and PLLs					
XIN	Main Oscillator Input	Input	–	VDDIO	Reset State: - PIO Input - Internal Pull-up disabled - Schmitt Trigger enabled(1)
XOUT	Main Oscillator Output	Output	–		
XIN32	Slow Clock Oscillator Input	Input	–		
XOUT32	Slow Clock Oscillator Output	Output	–		
PCK0–PCK2	Programmable Clock Output	Output	–		Reset State: - PIO Input - Internal Pull-up enabled - Schmitt Trigger enabled(1)
Real Time Clock - RTC					
RTCOUT0	Programmable RTC waveform output	Output	–	VDDIO	Reset State: - PIO Input - Internal Pull-up enabled - Schmitt Trigger enabled(1)
RTCOUT1	Programmable RTC waveform output	Output	–		
Serial Wire/JTAG Debug Port - SWJ-DP					
TCK/SWCLK	Test Clock/Serial Wire Clock	Input	–	VDDIO	Reset State: - SWJ-DP Mode - Internal pull-up disabled(5) - Schmitt Trigger enabled(1)
TDI	Test Data In	Input	–		
TDO/TRACESWO	Test Data Out / Trace Asynchronous Data Out	Output	–		
TMS/SWDIO	Test Mode Select /Serial Wire Input/Output	Input / I/O	–		
JTAGSEL	JTAG Selection	Input	High		Permanent Internal pull-down

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Flash Memory					
ERASE	Flash and NVM Configuration Bits Erase Command	Input	High	VDDIO	Reset State: - Erase Input - Internal pull-down enabled - Schmitt Trigger enabled[1]
Reset/Test					
NRST	Synchronous Microcontroller Reset	I/O	Low	VDDIO	Permanent Internal pull-up
TST	Test Select	Input	–		Permanent Internal pull-down
Wake-up					
WKUP[15:0]	Wake-up Inputs	Input	–	VDDIO	–
Universal Asynchronous Receiver Transceiver - UARTx					
URXDx	UART Receive Data	Input	–	–	–
UTXDx	UART Transmit Data	Output	–	–	–
PIO Controller - PIOA - PIOB - PIOC					
PA0–PA31	Parallel IO Controller A	I/O	–	VDDIO	Reset State: - PIO or System IOs[2] - Internal pull-up enabled - Schmitt Trigger enabled[1]
PB0–PB14	Parallel IO Controller B	I/O	–		
PC0–PC31	Parallel IO Controller C	I/O	–		
PIO Controller - Parallel Capture Mode					
PIODC0–PIODC7	Parallel Capture Mode Data	Input	–	VDDIO	–
PIODCCLK	Parallel Capture Mode Clock	Input	–		
PIODCEN1–2	Parallel Capture Mode Enable	Input	–		
External Bus Interface					
D0–D7	Data Bus	I/O	–	–	–
A0–A23	Address Bus	Output	–	–	–
NWAIT	External Wait Signal	Input	Low	–	–
Static Memory Controller - SMC					
NCS0–NCS3	Chip Select Lines	Output	Low	–	–
NRD	Read Signal	Output	Low	–	–
NWE	Write Enable	Output	Low	–	–
NAND Flash Logic					
NANDOE	NAND Flash Output Enable	Output	Low	–	–
NANDWE	NAND Flash Write Enable	Output	Low	–	–

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
High Speed Multimedia Card Interface - HSMCI					
MCCK	Multimedia Card Clock	Output	–	–	–
MCCDA	Multimedia Card Slot A Command	I/O	–	–	–
MCDA0–MCDA3	Multimedia Card Slot A Data	I/O	–	–	–
Universal Synchronous Asynchronous Receiver Transmitter - USARTx					
SCKx	USARTx Serial Clock	I/O	–	–	–
TXDx	USARTx Transmit Data	I/O	–	–	–
RXDx	USARTx Receive Data	Input	–	–	–
RTSx	USARTx Request To Send	Output	–	–	–
CTSx	USARTx Clear To Send	Input	–	–	–
DTR1	USART1 Data Terminal Ready	Output	–	–	–
DSR1	USART1 Data Set Ready	Input	–	–	–
DCD1	USART1 Data Carrier Detect	Output	–	–	–
RI1	USART1 Ring Indicator	Input	–	–	–
Synchronous Serial Controller - SSC					
TD	SSC Transmit Data	Output	–	–	–
RD	SSC Receive Data	Input	–	–	–
TK	SSC Transmit Clock	I/O	–	–	–
RK	SSC Receive Clock	I/O	–	–	–
TF	SSC Transmit Frame Sync	I/O	–	–	–
RF	SSC Receive Frame Sync	I/O	–	–	–
Timer/Counter - TC					
TCLKx	TC Channel x External Clock Input	Input	–	–	–
TIOAx	TC Channel x I/O Line A	I/O	–	–	–
TIOBx	TC Channel x I/O Line B	I/O	–	–	–
Pulse Width Modulation Controller - PWMC					
PWMHx	PWM Waveform Output High for channel x	Output	–	–	–
PWMLx	PWM Waveform Output Low for channel x	Output	–	–	Only output in complementary mode when dead time insertion is enabled.
PWMFI0–2	PWM Fault Input	Input	–	–	PWMFI1 and PWMFI2 on SAM4S4/S2 only

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Serial Peripheral Interface - SPI					
MISO	Master In Slave Out	I/O	–	–	–
MOSI	Master Out Slave In	I/O	–	–	–
SPCK	SPI Serial Clock	I/O	–	–	–
SPI_NPCS0	SPI Peripheral Chip Select 0	I/O	Low	–	–
SPI_NPCS1–SPI_NPCS3	SPI Peripheral Chip Select	Output	Low	–	–
Two-Wire Interface - TWI					
TWDx	TWIx Two-wire Serial Data	I/O	–	–	–
TWCKx	TWIx Two-wire Serial Clock	I/O	–	–	–
Analog					
ADVREF	ADC, DAC and Analog Comparator Reference	Analog	–	–	–
12-bit Analog-to-Digital Converter - ADC					
AD0–AD14	Analog Inputs	Analog, Digital	–	–	–
ADTRG	ADC Trigger	Input	–	VDDIO	–
12-bit Digital-to-Analog Converter - DAC					
DAC0–DAC1	Analog output	Analog, Digital	–	–	–
DACTRG	DAC Trigger	Input	–	VDDIO	–
Fast Flash Programming Interface - FFPI					
PGMEN0-PGMEN2	Programming Enabling	Input	–	VDDIO	–
PGMM0–PGMM3	Programming Mode	Input	–	VDDIO	–
PGMD0–PGMD15	Programming Data	I/O	–		–
PGMRDY	Programming Ready	Output	High		–
PGMNVALID	Data Direction	Output	Low		–
PGMNOE	Programming Read	Input	Low		–
PGMCK	Programming Clock	Input	–		–
PGMNCMD	Programming Command	Input	Low		–
USB Full Speed Device					
DDM	USB Full Speed Data -	Analog, Digital	–	VDDIO	Reset State: - USB Mode - Internal Pull-down[3]
DDP	USB Full Speed Data +				

Note:
1. Schmitt triggers can be disabled through PIO registers.
2. Some PIO lines are shared with system I/Os.
3. Refer to USB section of the product Electrical Characteristics for information on pull-down value in USB mode.
4. See “Typical Powering Schematics” section for restrictions on voltage range of analog cells.
5. TDO pin is set in input mode when the Cortex-M4 processor is not in debug mode. Thus the internal pull-up corresponding to this PIO line must be enabled to avoid current consumption due to floating input

4. Package and Pinout

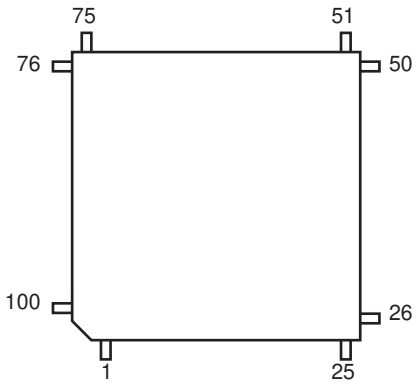
SAM4S devices are pin-to-pin compatible with SAM3N, SAM3S products in 48-, 64- and 100-pin versions, SAM4N and SAM7S legacy products in 64-pin versions.

4.1 100-lead Packages and Pinouts

Refer to Table 1-1 and Table 1-2 for the overview of devices available in 100-lead packages.

4.1.1 100-lead LQFP Package Outline

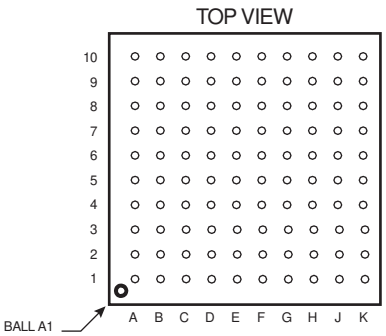
Figure 4-1. Orientation of the 100-lead LQFP Package



4.1.2 100-ball TFBGA Package Outline

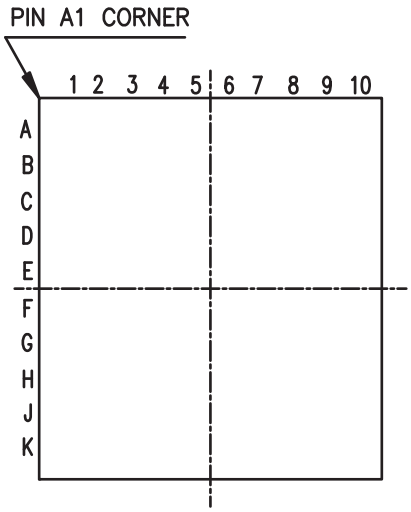
The 100-ball TFBGA package has a 0.8 mm ball pitch and respects Green Standards. Its dimensions are 9 x 9 x 1.1 mm. Figure 4-2 shows the orientation of the 100-ball TFBGA package.

Figure 4-2. Orientation of the 100-ball TFBGA Package



4.1.3 100-ball VFBGA Package Outline

Figure 4-3. Orientation of the 100-ball VFBGA Package



4.1.4 100-lead LQFP Pinout

Table 4-1. SAM4SD32/SD16/SA16/S16/S8/S4/S2 100-lead LQFP Pinout

1	ADVREF	26	GND	51	TDI/PB4	76	TDO/TRACESWO/PB5
2	GND	27	VDDIO	52	PA6/PGMNOE	77	JTAGSEL
3	PB0/AD4	28	PA16/PGMD4	53	PA5/PGMRDY	78	PC18
4	PC29/AD13	29	PC7	54	PC28	79	TMS/SWDIO/PB6
5	PB1/AD5	30	PA15/PGMD3	55	PA4/PGMNCMD	80	PC19
6	PC30/AD14	31	PA14/PGMD2	56	VDDCORE	81	PA31
7	PB2/AD6	32	PC6	57	PA27/PGMD15	82	PC20
8	PC31	33	PA13/PGMD1	58	PC8	83	TCK/SWCLK/PB7
9	PB3/AD7	34	PA24/PGMD12	59	PA28	84	PC21
10	VDDIN	35	PC5	60	NRST	85	VDDCORE
11	VDDOUT	36	VDDCORE	61	TST	86	PC22
12	PA17/PGMD5/AD0	37	PC4	62	PC9	87	ERASE/PB12
13	PC26	38	PA25/PGMD13	63	PA29	88	DDM/PB10
14	PA18/PGMD6/AD1	39	PA26/PGMD14	64	PA30	89	DDP/PB11
15	PA21/PGMD9/AD8	40	PC3	65	PC10	90	PC23
16	VDDCORE	41	PA12/PGMD0	66	PA3	91	VDDIO
17	PC27	42	PA11/PGMM3	67	PA2/PGMEN2	92	PC24
18	PA19/PGMD7/AD2	43	PC2	68	PC11	93	PB13/DAC0
19	PC15/AD11	44	PA10/PGMM2	69	VDDIO	94	PC25
20	PA22/PGMD10/AD9	45	GND	70	GND	95	GND
21	PC13/AD10	46	PA9/PGMM1	71	PC14	96	PB8/XOUT
22	PA23/PGMD11	47	PC1	72	PA1/PGMEN1	97	PB9/PGMCK/XIN
23	PC12/AD12	48	PA8/XOUT32/PGMM0	73	PC16	98	VDDIO
24	PA20/PGMD8/AD3	49	PA7/XIN32/ PGMNVALID	74	PA0/PGMEN0	99	PB14/DAC1
25	PC0	50	VDDIO	75	PC17	100	VDDPLL

4.1.5 100-ball TFBGA Pinout

Table 4-2. SAM4SD32/SD16/SA16/S16/S8/S4/S2 100-ball TFBGA Pinout

A1	PB1/AD5	C6	TCK/SWCLK/PB7	F1	PA18/PGMD6/AD1	H6	PC4
A2	PC29/AD13	C7	PC16	F2	PC26	H7	PA11/PGMM3
A3	VDDIO	C8	PA1/PGMEN1	F3	VDDOUT	H8	PC1
A4	PB9/PGMCK/XIN	C9	PC17	F4	GND	H9	PA6/PGMNOE
A5	PB8/XOUT	C10	PA0/PGMEN0	F5	VDDIO	H10	TDI/PB4
A6	PB13/DAC0	D1	PB3/AD7	F6	PA27/PGMD15	J1	PC15/AD11
A7	DDP/PB11	D2	PB0/AD4	F7	PC8	J2	PC0
A8	DDM/PB10	D3	PC24	F8	PA28	J3	PA16/PGMD4
A9	TMS/SWDIO/PB6	D4	PC22	F9	TST	J4	PC6
A10	JTAGSEL	D5	GND	F10	PC9	J5	PA24/PGMD12
B1	PC30/AD14	D6	GND	G1	PA21/PGMD9/AD8	J6	PA25/PGMD13
B2	ADVREF	D7	VDDCORE	G2	PC27	J7	PA10/PGMM2
B3	GNDANA	D8	PA2/PGMEN2	G3	PA15/PGMD3	J8	GND
B4	PB14/DAC1	D9	PC11	G4	VDDCORE	J9	VDDCORE
B5	PC21	D10	PC14	G5	VDDCORE	J10	VDDIO
B6	PC20	E1	PA17/PGMD5/AD0	G6	PA26/PGMD14	K1	PA22/PGMD10/AD9
B7	PA31	E2	PC31	G7	PA12/PGMD0	K2	PC13/AD10
B8	PC19	E3	VDDIN	G8	PC28	K3	PC12/AD12
B9	PC18	E4	GND	G9	PA4/PGMNCMD	K4	PA20/PGMD8/AD3
B10	TDO/TRACESWO/PB5	E5	GND	G10	PA5/PGMRDY	K5	PC5
C1	PB2/AD6	E6	NRST	H1	PA19/PGMD7/AD2	K6	PC3
C2	VDDPLL	E7	PA29	H2	PA23/PGMD11	K7	PC2
C3	PC25	E8	PA30	H3	PC7	K8	PA9/PGMM1
C4	PC23	E9	PC10	H4	PA14/PGMD2	K9	PA8/XOUT32/PGMM0
C5	ERASE/PB12	E10	PA3	H5	PA13/PGMD1	K10	PA7/XIN32/ PGMNVALID

4.1.6 100-ball VFBGA Pinout

Table 4-3. SAM4SD32/SD16/SA16/S16/S8/S4/S2 100-ball VFBGA Pinout

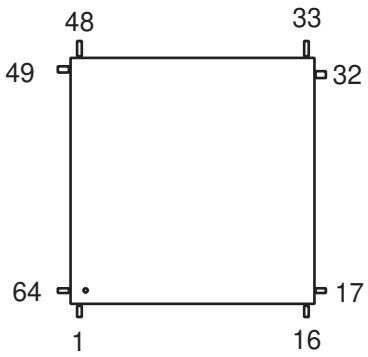
A1	ADVREF	C6	PC9	F1	VDDOUT	H6	PA12/PGMD0
A2	VDDPLL	C7	TMS/SWDIO/PB6	F2	PA18/PGMD6/AD1	H7	PA9/PGMM1
A3	PB9/PGMCK/XIN	C8	PA1/PGMEN1	F3	PA17/PGMD5/AD0	H8	VDDCORE
A4	PB8/XOUT	C9	PA0/PGMEN0	F4	GND	H9	PA6/PGMNOE
A5	JTAGSEL	C10	PC16	F5	GND	H10	PA5/PGMRDY
A6	DDP/PB11	D1	PB1/AD5	F6	PC26	J1	PA20/AD3/PGMD8
A7	DDM/PB10	D2	PC30/AD14	F7	PA4/PGMNCMD	J2	PC12/AD12
A8	PC20	D3	PC31	F8	PA28	J3	PA16/PGMD4
A9	PC19	D4	PC22	F9	TST	J4	PC6
A10	TDO/TRACESWO/PB5	D5	PC5	F10	PC8	J5	PA24/PGMD12
B1	GNDANA	D6	PA29	G1	PC15/AD11	J6	PA25/PGMD13
B2	PC25	D7	PA30	G2	PA19/PGMD7/AD2	J7	PA11/PGMM3
B3	PB14/DAC1	D8	GND	G3	PA21/AD8/PGMD9	J8	VDDCORE
B4	PB13/DAC0	D9	PC14	G4	PA15/PGMD3	J9	VDDCORE
B5	PC23	D10	PC11	G5	PC3	J10	TDI/PB4
B6	PC21	E1	VDDIN	G6	PA10/PGMM2	K1	PA23/PGMD11
B7	TCK/SWCLK/PB7	E2	PB3/AD7	G7	PC1	K2	PC0
B8	PA31	E3	PB2/AD6	G8	PC28	K3	PC7
B9	PC18	E4	GND	G9	NRST	K4	PA13/PGMD1
B10	PC17	E5	GND	G10	PA27/PGMD15	K5	PA26/PGMD14
C1	PB0/AD4	E6	GND	H1	PC13/AD10	K6	PC2
C2	PC29/AD13	E7	VDDIO	H2	PA22/AD9/PGMD10	K7	VDDIO
C3	PC24	E8	PC10	H3	PC27	K8	VDDIO
C4	ERASE/PB12	E9	PA2/PGMEN2	H4	PA14/PGMD2	K9	PA8/XOUT32/PGMM0
C5	VDDCORE	E10	PA3	H5	PC4	K10	PA7/XIN32/ PGMNVALID

4.2 64-lead Packages and Pinouts

Refer to Table 1-1 and Table 1-2 for the overview of devices available in 64-lead packages.

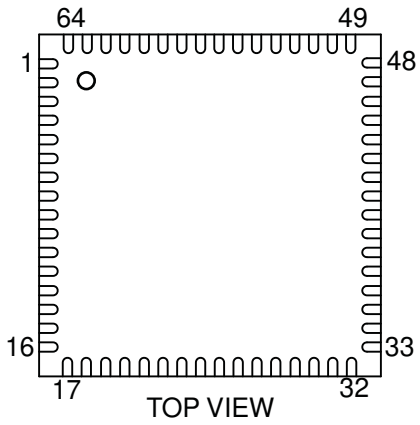
4.2.1 64-lead LQFP Package Outline

Figure 4-4. Orientation of the 64-lead LQFP Package



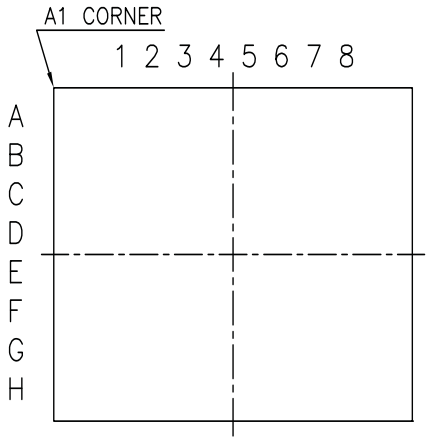
4.2.2 64-lead QFN Package Outline

Figure 4-5. Orientation of the 64-lead QFN Package



4.2.3 64-ball WLCSP Package Outline

Figure 4-6. Orientation of the 64-ball WLCSP Package



4.2.4 64-lead LQFP and QFN Pinout

Table 4-4. 64-pin SAM4SD32/SD16/SA16/S16/S8/S4/S2 Pinout

1	ADVREF	17	GND	33	TDI/PB4	49	TDO/TRACESWO/PB5
2	GND	18	VDDIO	34	PA6/PGMNOE	50	JTAGSEL
3	PB0/AD4	19	PA16/PGMD4	35	PA5/PGMRDY	51	TMS/SWDIO/PB6
4	PB1/AD5	20	PA15/PGMD3	36	PA4/PGMNCMD	52	PA31
5	PB2/AD6	21	PA14/PGMD2	37	PA27/PGMD15	53	TCK/SWCLK/PB7
6	PB3/AD7	22	PA13/PGMD1	38	PA28	54	VDDCORE
7	VDDIN	23	PA24/PGMD12	39	NRST	55	ERASE/PB12
8	VDDOUT	24	VDDCORE	40	TST	56	DDM/PB10
9	PA17/PGMD5/AD0	25	PA25/PGMD13	41	PA29	57	DDP/PB11
10	PA18/PGMD6/AD1	26	PA26/PGMD14	42	PA30	58	VDDIO
11	PA21/PGMD9/AD8	27	PA12/PGMD0	43	PA3	59	PB13/DAC0
12	VDDCORE	28	PA11/PGMM3	44	PA2/PGMEN2	60	GND
13	PA19/PGMD7/AD2	29	PA10/PGMM2	45	VDDIO	61	XOUT/PB8
14	PA22/PGMD10/AD9	30	PA9/PGMM1	46	GND	62	XIN/PGMCK/PB9
15	PA23/PGMD11	31	PA8/XOUT32/PGMM0	47	PA1/PGMEN1	63	PB14/DAC1
16	PA20/PGMD8/AD3	32	PA7/XIN32/PGMNVALID	48	PA0/PGMEN0	64	VDDPLL

Note: The bottom pad of the QFN package must be connected to ground.

4.2.5 64-ball WLCSP Pinout

Table 4-5. SAM4SD32/S32/SD16/S16/S8 64-ball WLCSP Pinout

A1	PA31	C1	GND	E1	PA29	G1	PA5
A2	PB7	C2	PA1	E2	TST	G2	PA6
A3	VDDCORE	C3	PA0	E3	NRST	G3	PA9
A4	PB10	C4	PB12	E4	PA28	G4	PA11
A5	VDDIO	C5	ADVREF	E5	PA25	G5	VDDCORE
A6	GND	C6	PB3	E6	PA23	G6	PA14
A7	PB9	C7	PB1	E7	PA18	G7	PA20
A8	PB14	C8	PB0	E8	VDDIN	G8	PA19
B1	PB5	D1	VDDIO	F1	PA27	H1	PA7
B2	JTAGSEL	D2	PA3	F2	VDDCORE	H2	PA8
B3	PB6	D3	PA30	F3	PA4	H3	PA10
B4	PB11	D4	PA2	F4	PB4	H4	PA12
B5	PB13	D5	PA13	F5	PA26	H5	PA24
B6	VDDPLL	D6	PA21	F6	PA16	H6	PA15
B7	PB8	D7	PA17	F7	PA22	H7	VDDIO
B8	GND	D8	PB2	F8	VDDOUT	H8	GND

Table 4-6. SAM4S4/S2 64-ball WLCSP Pinout

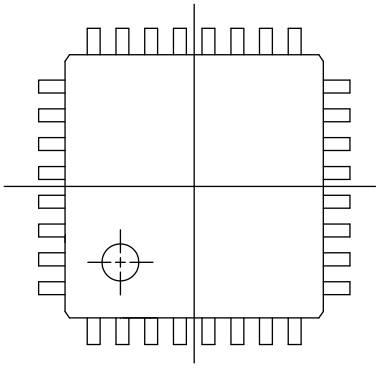
A1	PB5	C1	GND	E1	PA3	G1	VDDCORE
A2	PA31	C2	PA0	E2	PA30	G2	PA4
A3	VDDCORE	C3	PB7	E3	PA29	G3	PA9
A4	VDDIO	C4	PB12	E4	PA27	G4	PA11
A5	GND	C5	PA10	E5	PA24	G5	PA25
A6	PB8	C6	PB0	E6	PA18	G6	PA14
A7	PB9	C7	PB2	E7	PA17	G7	VDDIO
A8	ADVREF	C8	PB1	E8	VDDIN	G8	PA19
B1	PA1	D1	VDDIO	F1	TST	H1	PB4
B2	JTAGSEL	D2	PA2	F2	NRST	H2	PA7
B3	PB10	D3	PA28	F3	PA5	H3	PA8
B4	PB11	D4	PB6	F4	PA6	H4	PA12
B5	PB13	D5	PA26	F5	PA13	H5	VDDCORE
B6	VDDPLL	D6	PA23	F6	PA22	H6	PA15
B7	PB14	D7	PA16	F7	PA21	H7	GND
B8	GNDANA	D8	PB3	F8	VDDOUT	H8	PA20

4.3 48-lead Packages and Pinouts

Refer to Table 1-1 for the overview of devices available in 48-lead packages.

4.3.1 48-lead LQFP Package Outline

Figure 4-7. Orientation of the 48-lead LQFP Package



4.3.2 48-lead QFN Package Outline

Figure 4-8. Orientation of the 48-lead QFN Package