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SAMA5D2 SIP

SAMA5D2 System-In-Package (SIP) MPU with up to 1Gbit DDR2 SDRAM

Scope

This document is an overview of the main features of the SAMA5D2 SIP. The sole reference documents for product information on the SAMA5D2 and the DDR2-SDRAM memories are listed in the table below.

Introduction

The SAMA5D2 System-In-Package (SIP) integrates the ARM® Cortex®-A5 processor-based SAMA5D2 MPU with up to 1 Gbit DDR2-SDRAM in a single package.

By combining the high-performance, ultra-low-power SAMA5D2 with DDR2-SDRAM in a single package, PCB routing complexity, area and number of layers is reduced in the majority of cases. This makes board design easier and more robust by facilitating design for EMI, ESD and signal integrity.

Three DDR2-SDRAM memory sizes are available: 128 Mbit, 512 Mbit and 1 Gbit. While the first option targets applications with a small OS or bare metal, the larger options are suitable for applications using Linux.

The SAMA5D2 SIP is available in BGA196 and BGA289 package options.

Reference Documents

Type	Document Title	Available	Ref. No.
Datasheet	SAMA5D2 Series	www.microchip.com	DS60001476
Datasheet	2M × 4 Banks × 16 bit DDR2 SDRAM (128 Mbit)	www.winbond.com	W9712G6KB
Datasheet	8M × 4 Banks × 16 bit DDR2 SDRAM (512 Mbit)	www.winbond.com	W9751G6KB
Datasheet	8M × 8 Banks × 16 bit DDR2 SDRAM (1 Gbit)	www.winbond.com	W971GG6SB

Table of Contents

1. Features

- ARM Cortex-A5 core
  - ARMv7-A architecture
  - ARM TrustZone
  - NEON™ Media Processing Engine
  - Up to 500 MHz
  - ETM/ETB 8 Kbytes
- Memory Architecture
  - Memory Management Unit
  - 32-Kbyte L1 data cache, 32-Kbyte L1 instruction cache
  - 128-Kbyte L2 cache configurable to be used as an internal SRAM
  - DDR2-SDRAM memory up to 1 Gb
  - One 128-Kbyte scrambled internal SRAM
  - One 160-Kbyte internal ROM
    - 64-Kbyte scrambled and maskable ROM embedding boot loader/Secure boot loader
    - 96-Kbyte unscrambled, unmaskable ROM for NAND Flash BCH ECC table
  - High-bandwidth scramblable 16-bit Double Data Rate (DDR) multiport dynamic RAM controller supporting Winbond DDR2-SDRAM up to 1 Gb , including “on-the-fly” encryption/decryption path
  - 8-bit SLC/MLC NAND controller, with up to 32-bit Error Correcting Code (PMECC)
- System running up to 166 MHz
  - Reset controller, shutdown controller, periodic interval timer, independent watchdog timer and secure Real-Time Clock (RTC) with clock calibration
  - One 600 to 1200 MHz PLL for the system and one 480 MHz PLL optimized for USB high speed
  - Digital fractional PLL for audio (11.2896 MHz and 12.288 MHz)
  - Internal low-power 12 MHz RC and 32 KHz typical RC
  - Selectable 32.768-Hz low-power oscillator and 8 to 24 MHz oscillator
  - 51 DMA Channels including two 16-channel 64-bit Central DMA Controllers
  - 64-bit Advanced Interrupt Controller (AIC)
  - 64-bit Secure Advanced Interrupt Controller (SAIC)
  - Three programmable external clock signals
- Low-Power Modes
  - Ultra Low-power mode with fast wakeup capability
  - Low-power Backup mode with 5-Kbyte SRAM and SleepWalking™ features
    - Wakeup from up to nine wakeup pins, UART reception, analog comparison
    - Fast wakeup capability
    - Extended Backup mode with DDR2-SDRAM in Self-Refresh mode
- Peripherals
  - LCD TFT controller up to 1024x768, with four overlays, rotation, post-processing and alpha blending, 24-bit parallel RGB

  - ITU-R BT. 601/656/1120 Image Sensor Controller (ISC) supporting up to 5 M-pixel sensors with a parallel 12-bit interface for Raw Bayer, YCbCr, Monochrome and JPEG-compressed sensor interface
  - Two Synchronous Serial Controllers (SSC), two Inter-IC Sound Controllers (I2SC), and one Stereo Class D amplifier
  - One Peripheral Touch Controller (PTC) with up to 8 X-lines and 8 Y-lines (64-channel capacitive touch)
  - One Pulse Density Modulation Interface Controller (PDMIC)
  - One USB high-speed device port (UDPHS) and one USB high-speed host port or two USB high-speed host ports (UHPHS)
  - One USB high-speed host port with a High-Speed Inter-Chip (HSIC) interface
  - One 10/100 Ethernet MAC (GMAC)
    - Energy efficiency support (IEEE 802.3az standard)
    - Ethernet AVB support with IEEE802.1AS time stamping
    - IEEE802.1Qav credit-based traffic-shaping hardware support
    - IEEE1588 Precision Time Protocol (PTP)
  - Two high-speed memory card hosts:
    - SDMMC0: SD 3.0, eMMC 4.51, 8 bits
    - SDMMC1: SD 2.0, eMMC 4.41, 4 bits only
  - Two master/slave Serial Peripheral Interfaces (SPI)
  - Two Quad Serial Peripheral Interfaces (QSPI)
  - Five FLEXCOMs (USART, SPI and TWI)
  - Five UARTs
  - Two master CAN-FD (MCAN) controllers with SRAM-based mailboxes, and time- and event-triggered transmission
  - One Rx only UART in backup area (RXLP)
  - One analog comparator (ACC) in backup area
  - Two 2-wire interfaces (TWIHS) up to 400 Kbits/s supporting the I^2C protocol and SMBUS (TWIHS)
  - Two 3-channel 32-bit Timer/Counters (TC), supporting basic PWM modes
  - One full-featured 4-channel 16-bit Pulse Width Modulation (PWM) controller
  - One 12-channel, 12-bit, Analog-to-Digital Converter (ADC) with Resistive TouchScreen capability
- Safety
  - Zero-power Power-On Reset (POR) cells
  - Main crystal clock failure detector
  - Write-protected registers
  - Integrity Check Monitor (ICM) based on SHA256
  - Memory Management Unit
  - Independent watchdog
- Security
  - 5 Kbytes of internal scrambled SRAM:
    - 1 Kbyte non-erasable on tamper detection
    - 4 Kbytes erasable on tamper detection
  - 256 bits of scrambled and erasable registers

  - Up to eight tamper pins for static or dynamic intrusion detections
  - Environmental monitors on specific versions: temperature, voltage, frequency and active die shield(1)
  - Secure Boot Loader(2)
  - On-the-fly AES encryption/decryption on DDR2-SDRAM and QSPI memories (AESB)
  - RTC including time-stamping on security intrusions
  - Programmable fuse box with 544 fuse bits (including JTAG protection and BMS)
- Hardware cryptography
  - SHA (SHA1, SHA224, SHA256, SHA384, SHA512): compliant with FIPS PUB 180-2
  - AES: 256-, 192-, 128-bit key algorithm, compliant with FIPS PUB 197
  - TDES: two-key or three-key algorithms, compliant with FIPS PUB 46-3
  - True Random Number Generator (TRNG) compliant with NIST Special Publication 800-22 Test Suite and FIPS PUBs 140-2 and 140-3
- Up to 128 I/Os
  - Fully programmable through set/clear registers
  - Multiplexing of up to eight peripheral functions per I/O line
  - Each I/O line can be assigned to a peripheral or used as a general purpose I/O
  - PIO controller features a synchronous output providing up to 32 bits of data output in one write operation

Note:

1. For environmental monitors, refer to the document *SAMA5D23 and SAMA5D28 Environmental Monitors* (document no. 44036), available under Non-Disclosure Agreement (NDA). Contact a Microchip sales representative for details.
2. For secure boot strategies, refer to the document *SAMA5D2 Series Secure Boot Strategy* (document no. 44040), available under Non-Disclosure Agreement (NDA). Contact a Microchip sales representative for details.

2. DDR2-SDRAM Features

- Power Supply: V_{DD}, V_{DDQ} = 1.8 V ±0.1 V
- Double Data Rate architecture: two data transfers per clock cycle
- CAS Latency: 3
- Burst Length: 8
- Bi-directional, differential data strobes (DQS and DQSN) are transmitted/received with data
- Edge-aligned with Read data and center-aligned with Write data
- DLL aligns DQ and DQS transitions with clock
- Differential clock inputs (CLK and CLKN)
- Data masks (DM) for write data
- Commands entered on each positive CLK edge, data and data mask are referenced to both edges of DQS
- Auto-refresh and Self-refresh modes
- Precharged Powerdown and Active Powerdown
- Write Data Mask
- Write Latency = Read Latency - 1 (WL = RL - 1)
- Interface: SSTL_18

3. Configuration Summary

Table 3-1. Configuration Summary

Feature	SAMA5D225	SAMA5D27		SAMA5D28
Package	TFBGA196	TFBGA289		
DDR2-SDRAM	128 Mb	512 Mb	1 Gb	1 Gb
SMC	Up to 16-bit			
Internal Memory Bus Width	16-bit			
PIOs	90	128		
SRAM	128 Kbytes			
QSPI	2			
LCD	24-bit RGB			
Camera Interface (ISC)	1			
EMAC	1			
PTC	4 X-lines x 8 Y-lines	8 X-lines x 8 Y-lines		
CAN	1	2		
USB	2 (2 Hosts or 1 Host/1 Device)	3 (2 Hosts/1 HSIC or 1 Host/1 Device/1 HSIC)		
UART/SPI/I^2C	9 / 7 / 7	10 / 7 / 7		
SDIO/SD/MMC	2			
I^2S/SSC/Class D/PDM	2 / 2 / 1 / 1			
ADC Inputs	5	12		
Timers	5	6		
PWM	4 (PWM) + 5 (TC)	4 (PWM) + 6 (TC)		
Tamper Pins	6	8		
AESB	Yes			
Environmental Monitors, Die Shield	–	–		Yes

4. Chip Identifier

Table 4-1. SAMA5D2 SIP Chip ID Registers

Chip Name	CHIPID_CIDR	CHIPID_EXID
SAMA5D225C-D1M	0x8A5C08C2	0x00000053
SAMA5D27C-D5M		0x00000032
SAMA5D27C-D1G		0x00000033
SAMA5D28C-D1G		0x00000013

5. Package and Ballout

The SAMA5D2 SIP is available in the packages listed below.

Important: SAMA5D2 SIP devices are not pin-to-pin compatible with SAMA5D2 devices.

For mechanical characteristics of the TFBGA196, refer to the SAMA5D2 Series Datasheet, ref. no. DS60001476, available via www.microchip.com.

For mechanical characteristics of the TFBGA289, see Mechanical Characteristics.

Table 5-1. Packages

Package Name	Ball Count	Ball Pitch	Package Size
TFBGA196	196	0.75 mm	11 x 11 (mm)
TFBGA289	289	0.8 mm	14 x 14 (mm)

Table 5-2. Ball Description

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
U13	M8	VDDSDMMC	GPIO_EMMC	PA0	I/O	–	–	A	SDMMC0_CK	I/O	1	PIO, I, PU, ST
								B	QSPI0_SCK	O	1	
								F	D0	I/O	2	
N7	F7	VDDSDMMC	GPIO_EMMC	PA1	I/O	–	–	A	SDMMC0_CMD	I/O	1	PIO, I, PU, ST
								B	QSPI0_CS	O	1	
								F	D1	I/O	2	
U14	L8	VDDSDMMC	GPIO_EMMC	PA2	I/O	–	–	A	SDMMC0_DAT0	I/O	1	PIO, I, PU, ST
								B	QSPI0_IO0	I/O	1	
								F	D2	I/O	2	
T13	G8	VDDSDMMC	GPIO_EMMC	PA3	I/O	–	–	A	SDMMC0_DAT1	I/O	1	PIO, I, PU, ST
								B	QSPI0_IO1	I/O	1	
								F	D3	I/O	2	
U15	K8	VDDSDMMC	GPIO_EMMC	PA4	I/O	–	–	A	SDMMC0_DAT2	I/O	1	PIO, I, PU, ST
								B	QSPI0_IO2	I/O	1	
								F	D4	I/O	2	
U16	P9	VDDSDMMC	GGPIO_EMMC	PA5	I/O	–	–	A	SDMMC0_DAT3	I/O	1	PIO, I, PU, ST
								B	QSPI0_IO3	I/O	1	
								F	D5	I/O	2	
U17	P10	VDDSDMMC	GPIO_EMMC	PA6	I/O	–	–	A	SDMMC0_DAT4	I/O	1	PIO, I, PU, ST
								B	QSPI1_SCK	O	1	
								D	TIOA5	I/O	1	
								E	FLEXCOM2_IO0	I/O	1	

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
								F	D6	I/O	2	
R11	P11	VDDSDMMC	GPIO_EMMC	PA7	I/O	–	–	A	SDMMC0_DAT5	I/O	1	PIO, I, PU, ST
								B	QSPI1_IO0	I/O	1	
								D	TIOB5	I/O	1	
								E	FLEXCOM2_IO1	I/O	1	
								F	D7	I/O	2	
R9	K9	VDDSDMMC	GPIO_EMMC	PA8	I/O	–	–	A	SDMMC0_DAT6	I/O	1	PIO, I, PU, ST
								B	QSPI1_IO1	I/O	1	
								D	TCLK5	I	1	
								E	FLEXCOM2_IO2	I/O	1	
								F	NWE/NANDWE	O	2	
P8	J9	VDDSDMMC	GPIO_EMMC	PA9	I/O	–	–	A	SDMMC0_DAT7	I/O	1	PIO, I, PU, ST
								B	QSPI1_IO2	I/O	1	
								D	TIOA4	I/O	1	
								E	FLEXCOM2_IO3	O	1	
								F	NCS3	O	2	
R10	N14	VDDSDMMC	GPIO_EMMC	PA10	I/O	–	–	A	SDMMC0_RSTN	O	1	PIO, I, PU, ST
								B	QSPI1_IO3	I/O	1	
								D	TIOB4	I/O	1	
								E	FLEXCOM2_IO4	O	1	
								F	A21/NANDALE	O	2	
P15	N13	VDDIOP1	GPIO	PA11	I/O	–	–	A	SDMMC0_1V8SEL	O	1	PIO, I, PU, ST
								B	QSPI1_CS	O	1	
								D	TCLK4	I	1	
								F	A22/NANDCLE	O	2	
N17	L12	VDDIOP1	GPIO	PA12	I/O	–	–	A	SDMMC0_WP	I	1	PIO, I, PU, ST
								B	IRQ	I	1	
								F	NRD/NANDOE	O	2	
P16	M14	VDDIOP1	GPIO	PA13	I/O	–	–	A	SDMMC0_CD	I	1	PIO, I, PU, ST
								E	FLEXCOM3_IO1	I/O	1	
								F	D8	I/O	2	
M17	J10	VDDIOP1	GPIO_QSPI	PA14	I/O	–	–	A	SPI0_SPCK	I/O	1	PIO, I, PU, ST
								B	TK1	I/O	1	
								C	QSPI0_SCK	O	2	
								D	I2SC1_MCK	O	2	
								E	FLEXCOM3_IO2	I/O	1	
								F	D9	I/O	2	
N16	L14	VDDIOP1	GPIO	PA15	I/O	–	–	A	SPI0_MOSI	I/O	1	PIO, I, PU, ST
								B	TF1	I/O	1	
								C	QSPI0_CS	O	2	
								D	I2SC1_CK	I/O	2	

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
								E	FLEXCOM3_IO0	I/O	1	
								F	D10	I/O	2	
M11	H14	VDDIOP1	GPIO_IO	PA16	I/O	–	–	A	SPI0_MISO	I/O	1	PIO, I, PU, ST
								B	TD1	O	1	
								C	QSPI0_IO0	I/O	2	
								D	I2SC1_WS	I/O	2	
								E	FLEXCOM3_IO3	O	1	
								F	D11	I/O	2	
N14	K14	VDDIOP1	GPIO_IO	PA17	I/O	–	–	A	SPI0_NPCS0	I/O	1	PIO, I, PU, ST
								B	RD1	I	1	
								C	QSPI0_IO1	I/O	2	
								D	I2SC1_DI0	I	2	
								E	FLEXCOM3_IO4	O	1	
								F	D12	I/O	2	
T16	L9	VDDIOP1	GPIO_IO	PA18	I/O	–	–	A	SPI0_NPCS1	O	1	PIO, I, PU, ST
								B	RK1	I/O	1	
								C	QSPI0_IO2	I/O	2	
								D	I2SC1_DO0	O	2	
								E	SDMMC1_DAT0	I/O	1	
								F	D13	I/O	2	
T15	P12	VDDIOP1	GPIO_IO	PA19	I/O	–	–	A	SPI0_NPCS2	O	1	PIO, I, PU, ST
								B	RF1	I/O	1	
								C	QSPI0_IO3	I/O	2	
								D	TIOA0	I/O	1	
								E	SDMMC1_DAT1	I/O	1	
								F	D14	I/O	2	
P9	H9	VDDIOP1	GPIO_IO	PA20	I/O	–	–	A	SPI0_NPCS3	O	1	PIO, I, PU, ST
								D	TIOB0	I/O	1	
								E	SDMMC1_DAT2	I/O	1	
								F	D15	I/O	2	
P10	G9	VDDIOP1	GPIO_IO	PA21	I/O	–	–	A	IRQ	I	2	PIO, I, PU, ST
								B	PCK2	O	3	
								D	TCLK0	I	1	
								E	SDMMC1_DAT3	I/O	1	
								F	NANDRDY	I	2	
T17	K10	VDDIOP1	GPIO_QSPI	PA22	I/O	–	–	A	FLEXCOM1_IO2	I/O	1	PIO, I, PU, ST
								B	D0	I/O	1	
								C	TCK	I	4	
								D	SPI1_SPCK	I/O	2	
								E	SDMMC1_CK	I/O	1	
								F	QSPI0_SCK	O	3	

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
T14	G10	VDDIOP1	GPIO	PA23	I/O	–	–	A	FLEXCOM1_IO1	I/O	1	PIO, I, PU, ST
								B	D1	I/O	1	
								C	TDI	I	4	
								D	SPI1_MOSI	I/O	2	
								F	QSPI0_CS	O	3	
R17	P13	VDDIOP1	GPIO_IO	PA24	I/O	–	–	A	FLEXCOM1_IO0	I/O	1	PIO, I, PU, ST
								B	D2	I/O	1	
								C	TDO	O	4	
								D	SPI1_MISO	I/O	2	
								F	QSPI0_IO0	I/O	3	
R16	H10	VDDIOP1	GPIO_IO	PA25	I/O	–	–	A	FLEXCOM1_IO3	O	1	PIO, I, PU, ST
								B	D3	I/O	1	
								C	TMS	I	4	
								D	SPI1_NPCS0	I/O	2	
								F	QSPI0_IO1	I/O	3	
P17	L10	VDDIOP1	GPIO_IO	PA26	I/O	–	–	A	FLEXCOM1_IO4	O	1	PIO, I, PU, ST
								B	D4	I/O	1	
								C	NTRST	I	4	
								D	SPI1_NPCS1	O	2	
								F	QSPI0_IO2	I/O	3	
R15	P14	VDDIOP1	GPIO_IO	PA27	I/O	–	–	A	TIOA1	I/O	2	PIO, I, PU, ST
								B	D5	I/O	1	
								C	SPI0_NPCS2	O	2	
								D	SPI1_NPCS2	O	2	
								E	SDMMC1_RSTN	O	1	
								F	QSPI0_IO3	I/O	3	
R14	N12	VDDIOP1	GPIO	PA28	I/O	–	–	A	TIOB1	I/O	2	PIO, I, PU, ST
								B	D6	I/O	1	
								C	SPI0_NPCS3	O	2	
								D	SPI1_NPCS3	O	2	
								E	SDMMC1_CMD	I/O	1	
								F	CLASSD_L0	O	1	
P14	M12	VDDIOP1	GPIO	PA29	I/O	–	–	A	TCLK1	I	2	PIO, I, PU, ST
								B	D7	I/O	1	
								C	SPI0_NPCS1	O	2	
								E	SDMMC1_WP	I	1	
								F	CLASSD_L1	O	1	
R13	N11	VDDIOP1	GPIO	PA30	I/O	–	–	B	NWE/NANDWE	O	1	PIO, I, PU, ST
								C	SPI0_NPCS0	I/O	2	
								D	PWMH0	O	1	
								E	SDMMC1_CD	I	1	

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
								F	CLASSD_L2	O	1	
P13	M11	VDDIOP1	GPIO	PA31	I/O	–	–	B	NCS3	O	1	PIO, I, PU, ST
								C	SPI0_MISO	I/O	2	
								D	PWML0	O	1	
								F	CLASSD_L3	O	1	
F5	E6	VDDIOP0	GPIO	PB0	I/O	–	–	B	A21/NANDALE	O	1	PIO, I, PU, ST
								C	SPI0_MOSI	I/O	2	
								D	PWMH1	O	1	
C8	D6	VDDIOP0	GPIO	PB1	I/O	–	–	B	A22/NANDCLE	O	1	PIO, I, PU, ST
								C	SPI0_SPCK	I/O	2	
								D	PWML1	O	1	
								F	CLASSD_R0	O	1	
C7	C6	VDDIOP0	GPIO	PB2	I/O	–	–	B	NRD/NANDOE	O	1	PIO, I, PU, ST
								D	PWMFI0	I	1	
								F	CLASSD_R1	O	1	
B8	C5	VDDIOP0	GPIO	PB3	I/O	–	–	A	URXD4	I	1	PIO, I, PU, ST
								B	D8	I/O	1	
								C	IRQ	I	3	
								D	PWMEXTRG1	I	1	
								F	CLASSD_R2	O	1	
B7	D5	VDDIOP0	GPIO	PB4	I/O	–	–	A	UTXD4	O	1	PIO, I, PU, ST
								B	D9	I/O	1	
								C	FIQ	I	4	
								F	CLASSD_R3	O	1	
A10	D7	VDDIOP0	GPIO_QSPI	PB5	I/O	–	–	A	TCLK2	I	1	PIO, I, PU, ST
								B	D10	I/O	1	
								C	PWMH2	O	1	
								D	QSPI1_SCK	O	2	
								F	GTSUCOMP	O	3	
A9	C8	VDDIOP0	GPIO	PB6	I/O	–	–	A	TIOA2	I/O	1	PIO, I, PU, ST
								B	D11	I/O	1	
								C	PWML2	O	1	
								D	QSPI1_CS	O	2	
								F	GTXER	O	3	
D5	D9	VDDIOP0	GPIO_IO	PB7	I/O	–	–	A	TIOB2	I/O	1	PIO, I, PU, ST
								B	D12	I/O	1	
								C	PWMH3	O	1	
								D	QSPI1_IO0	I/O	2	
								F	GRXCK	I	3	
E5	C7	VDDIOP0	GPIO_IO	PB8	I/O	–	–	A	TCLK3	I	1	PIO, I, PU, ST
								B	D13	I/O	1	

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
								C	PWML3	O	1	
								D	QSPI1_IO1	I/O	2	
								F	GCRS	I	3	
C6	C9	VDDIOP0	GPIO_IO	PB9	I/O	–	–	A	TIOA3	I/O	1	PIO, I, PU, ST
								B	D14	I/O	1	
								C	PWMFI1	I	1	
								D	QSPI1_IO2	I/O	2	
								F	GCOL	I	3	
A8	F6	VDDIOP0	GPIO_IO	PB10	I/O	–	–	A	TIOB3	I/O	1	PIO, I, PU, ST
								B	D15	I/O	1	
								C	PWMEXTRG2	I	1	
								D	QSPI1_IO3	I/O	2	
								F	GRX2	I	3	
A7	B9	VDDIOP0	GPIO	PB11	I/O	–	–	A	LCDDAT0	O	1	PIO, I, PU, ST
								B	A0/NBS0	O	1	
								C	URXD3	I	3	
								D	PDMIC_DAT		2	
								F	GRX3	I	3	
B6	B8	VDDIOP0	GPIO	PB12	I/O	–	–	A	LCDDAT1	O	1	PIO, I, PU, ST
								B	A1	O	1	
								C	UTXD3	O	3	
								D	PDMIC_CLK		2	
								F	GTX2	O	3	
C5	B7	VDDIOP0	GPIO	PB13	I/O	–	–	A	LCDDAT2	O	1	PIO, I, PU, ST
								B	A2	O	1	
								C	PCK1	O	3	
								F	GTX3	O	3	
A6	G6	VDDIOP0	GPIO_QSPI	PB14	I/O	–	–	A	LCDDAT3	O	1	PIO, I, PU, ST
								B	A3	O	1	
								C	TK1	I/O	2	
								D	I2SC1_MCK	O	1	
								E	QSPI1_SCK	O	3	
								F	GTXCK	I/O	3	
E4	B5	VDDIOP0	GPIO	PB15	I/O	–	–	A	LCDDAT4	O	1	PIO, I, PU, ST
								B	A4	O	1	
								C	TF1	I/O	2	
								D	I2SC1_CK	I/O	1	
								E	QSPI1_CS	O	3	
								F	GTXEN	O	3	
B5	C4	VDDIOP0	GPIO_IO	PB16	I/O	–	–	A	LCDDAT5	O	1	PIO, I, PU, ST
								B	A5	O	1	

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
								C	TD1	O	2	
								D	I2SC1_WS	I/O	1	
								E	QSPI1_IO0	I/O	3	
								F	GRXDV	I	3	
C4	A5	VDDIOP0	GPIO_IO	PB17	I/O	–	–	A	LCDDAT6	O	1	PIO, I, PU, ST
								B	A6	O	1	
								C	RD1	I	2	
								D	I2SC1_DI0	I	1	
								E	QSPI1_IO1	I/O	3	
								F	GRXER	I	3	
A5	B4	VDDIOP0	GPIO_IO	PB18	I/O	–	–	A	LCDDAT7	O	1	PIO, I, PU, ST
								B	A7	O	1	
								C	RK1	I/O	2	
								D	I2SC1_DO0	O	1	
								E	QSPI1_IO2	I/O	3	
								F	GRX0	I	3	
B4	A6	VDDIOP0	GPIO_IO	PB19	I/O	–	–	A	LCDDAT8	O	1	PIO, I, PU, ST
								B	A8	O	1	
								C	RF1	I/O	2	
								D	TIOA3	I/O	2	
								E	QSPI1_IO3	I/O	3	
								F	GRX1	I	3	
A4	A4	VDDIOP0	GPIO	PB20	I/O	–	–	A	LCDDAT9	O	1	PIO, I, PU, ST
								B	A9	O	1	
								C	TK0	I/O	1	
								D	TIOB3	I/O	2	
								E	PCK1	O	4	
								F	GTX0	O	3	
D3	A3	VDDIOP0	GPIO	PB21	I/O	–	–	A	LCDDAT10	O	1	PIO, I, PU, ST
								B	A10	O	1	
								C	TF0	I/O	1	
								D	TCLK3	I	2	
								E	FLEXCOM3_IO2	I/O	3	
								F	GTX1	O	3	
C3	D3	VDDIOP0	GPIO	PB22	I/O	–	–	A	LCDDAT11	O	1	PIO, I, PU, ST
								B	A11	O	1	
								C	TD0	O	1	
								D	TIOA2	I/O	2	
								E	FLEXCOM3_IO1	I/O	3	
								F	GMDC	O	3	
B3	B2	VDDIOP0	GPIO	PB23	I/O	–	–	A	LCDDAT12	O	1	PIO, I, PU, ST

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
								B	A12	O	1	
								C	RD0	I	1	
								D	TIOB2	I/O	2	
								E	FLEXCOM3_IO0	I/O	3	
								F	GMDIO	I/O	3	
E2	E3	VDDIOP0	GPIO	PB24	I/O	–	–	A	LCDDAT13	O	1	PIO, I, PU, ST
								B	A13	O	1	
								C	RK0	I/O	1	
								D	TCLK2	I	2	
								E	FLEXCOM3_IO3	O	3	
								F	ISC_D10	I	3	
A3	E2	VDDIOP0	GPIO	PB25	I/O	–	–	A	LCDDAT14	O	1	PIO, I, PU, ST
								B	A14	O	1	
								C	RF0	I/O	1	
								E	FLEXCOM3_IO4	O	3	
								F	ISC_D11	I	3	
G3	D4	VDDIOP0	GPIO	PB26	I/O	–	–	A	LCDDAT15	O	1	PIO, I, PU, ST
								B	A15	O	1	
								C	URXD0	I	1	
								D	PDMIC_DAT		1	
								F	ISC_D0	I	3	
F4	C3	VDDIOP0	GPIO	PB27	I/O	–	–	A	LCDDAT16	O	1	PIO, I, PU, ST
								B	A16	O	1	
								C	UTXD0	O	1	
								D	PDMIC_CLK		1	
								F	ISC_D1	I	3	
D2	D2	VDDIOP0	GPIO	PB28	I/O	–	–	A	LCDDAT17	O	1	PIO, I, PU, ST
								B	A17	O	1	
								C	FLEXCOM0_IO0	I/O	1	
								D	TIOA5	I/O	2	
								F	ISC_D2	I	3	
G8	B3	VDDIOP0	GPIO	PB29	I/O	–	–	A	LCDDAT18	O	1	PIO, I, PU, ST
								B	A18	O	1	
								C	FLEXCOM0_IO1	I/O	1	
								D	TIOB5	I/O	2	
								F	ISC_D3	I	3	
C2	F3	VDDIOP0	GPIO	PB30	I/O	–	–	A	LCDDAT19	O	1	PIO, I, PU, ST
								B	A19	O	1	
								C	FLEXCOM0_IO2	I/O	1	
								D	TCLK5	I	2	
								F	ISC_D4	I	3	

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
G7	A2	VDDIOP0	GPIO	PB31	I/O	–	–	A	LCDDAT20	O	1	PIO, I, PU, ST
								B	A20	O	1	
								C	FLEXCOM0_IO3	O	1	
								D	TWD0	I/O	1	
								F	ISC_D5	I	3	
N10	L13	VDDIOP1	GPIO	PC0	I/O	–	–	A	LCDDAT21	O	1	PIO, I, PU, ST
								B	A23	O	1	
								C	FLEXCOM0_IO4	O	1	
								D	TWCK0	I/O	1	
								F	ISC_D6	I	3	
N11	H11	VDDIOP1	GPIO	PC1	I/O	–	–	A	LCDDAT22	O	1	PIO, I, PU, ST
								B	A24	O	1	
								C	CANTX0	O	1	
								D	SPI1_SPCK	I/O	1	
								E	I2SC0_CK	I/O	1	
								F	ISC_D7	I	3	
N9	L11	VDDIOP1	GPIO	PC2	I/O	–	–	A	LCDDAT23	O	1	PIO, I, PU, ST
								B	A25	O	1	
								C	CANRX0	I	1	
								D	SPI1_MOSI	I/O	1	
								E	I2SC0_MCK	O	1	
								F	ISC_D8	I	3	
M10	F13	VDDIOP1	GPIO	PC3	I/O	–	–	A	LCDPWM	O	1	PIO, I, PU, ST
								B	NWAIT	I	1	
								C	TIOA1	I/O	1	
								D	SPI1_MISO	I/O	1	
								E	I2SC0_WS	I/O	1	
								F	ISC_D9	I	3	
N15	G14	VDDIOP1	GPIO	PC4	I/O	–	–	A	LCDDISP	O	1	PIO, I, PU, ST
								B	NWR1/NBS1	O	1	
								C	TIOB1	I/O	1	
								D	SPI1_NPCS0	I/O	1	
								E	I2SC0_DI0	I	1	
								F	ISC_PCK	I	3	
M16	J14	VDDIOP1	GPIO	PC5	I/O	–	–	A	LCDVSYNC	O	1	PIO, I, PU, ST
								B	NCS0	O	1	
								C	TCLK1	I	1	
								D	SPI1_NPCS1	O	1	
								E	I2SC0_DO0	O	1	
								F	ISC_VSYNC	I	3	
L11	J13	VDDIOP1	GPIO	PC6	I/O	–	–	A	LCDHSYNC	O	1	PIO, I, PU, ST

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
								B	NCS1	O	1	
								C	TWD1	I/O	1	
								D	SPI1_NPCS2	O	1	
								F	ISC_HSYNC	I	3	
M15	F14	VDDIOP1	GPIO_CLK	PC7	I/O	–	–	A	LCDPCK	O	1	PIO, I, PU, ST
								B	NCS2	O	1	
								C	TWCK1	I/O	1	
								D	SPI1_NPCS3	O	1	
								E	URXD1	I	2	
								F	ISC_MCK	O	3	
M13	K13	VDDIOP1	GPIO	PC8	I/O	–	–	A	LCDDEN	O	1	PIO, I, PU, ST
								B	NANDRDY	I	1	
								C	FIQ	I	1	
								D	PCK0	O	3	
								E	UTXD1	O	2	
								F	ISC_FIELD	I	3	
B2	–	VDDISC	GPIO	PC9	I/O	–	–	A	FIQ	I	3	PIO, I, PU, ST
								B	GTSUCOMP	O	1	
								C	ISC_D0	I	1	
								D	TIOA4	I/O	2	
G4	–	VDDISC	GPIO	PC10	I/O	–	–	A	LCDDAT2	O	2	PIO, I, PU, ST
								B	GTXCK	I/O	1	
								C	ISC_D1	I	1	
								D	TIOB4	I/O	2	
								E	CANTX0	O	2	
A2	–	VDDISC	GPIO	PC11	I/O	–	–	A	LCDDAT3	O	2	PIO, I, PU, ST
								B	GTXEN	O	1	
								C	ISC_D2	I	1	
								D	TCLK4	I	2	
								E	CANRX0	I	2	
								F	A0/NBS0	O	2	
A1	–	VDDISC	GPIO	PC12	I/O	–	–	A	LCDDAT4	O	2	PIO, I, PU, ST
								B	GRXDV	I	1	
								C	ISC_D3	I	1	
								D	URXD3	I	1	
								E	TK0	I/O	2	
								F	A1	O	2	
B1	–	VDDISC	GPIO	PC13	I/O	–	–	A	LCDDAT5	O	2	PIO, I, PU, ST
								B	GRXER	I	1	
								C	ISC_D4	I	1	
								D	UTXD3	O	1	

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
								E	TF0	I/O	2	
								F	A2	O	2	
G5	–	VDDISC	GPIO	PC14	I/O	–	–	A	LCDDAT6	O	2	PIO, I, PU, ST
								B	GRX0	I	1	
								C	ISC_D5	I	1	
								E	TD0	O	2	
								F	A3	O	2	
G2	–	VDDISC	GPIO	PC15	I/O	–	–	A	LCDDAT7	O	2	PIO, I, PU, ST
								B	GRX1	I	1	
								C	ISC_D6	I	1	
								E	RD0	I	2	
								F	A4	O	2	
G6	–	VDDISC	GPIO	PC16	I/O	–	–	A	LCDDAT10	O	2	PIO, I, PU, ST
								B	GTX0	O	1	
								C	ISC_D7	I	1	
								E	RK0	I/O	2	
								F	A5	O	2	
C1	–	VDDISC	GPIO	PC17	I/O	–	–	A	LCDDAT11	O	2	PIO, I, PU, ST
								B	GTX1	O	1	
								C	ISC_D8	I	1	
								E	RF0	I/O	2	
								F	A6	O	2	
G9	–	VDDISC	GPIO	PC18	I/O	–	–	A	LCDDAT12	O	2	PIO, I, PU, ST
								B	GMDC	O	1	
								C	ISC_D9	I	1	
								E	FLEXCOM3_IO2	I/O	2	
								F	A7	O	2	
D1	–	VDDISC	GPIO	PC19	I/O	–	–	A	LCDDAT13	O	2	PIO, I, PU, ST
								B	GMDIO	I/O	1	
								C	ISC_D10	I	1	
								E	FLEXCOM3_IO1	I/O	2	
								F	A8	O	2	
H4	–	VDDISC	GPIO	PC20	I/O	–	–	A	LCDDAT14	O	2	PIO, I, PU, ST
								B	GRXCK	I	1	
								C	ISC_D11	I	1	
								E	FLEXCOM3_IO0	I/O	2	
								F	A9	O	2	
E1	–	VDDISC	GPIO	PC21	I/O	–	–	A	LCDDAT15	O	2	PIO, I, PU, ST
								B	GTXER	O	1	
								C	ISC_PCK	I	1	
								E	FLEXCOM3_IO3	O	2	

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
								F	A10	O	2	
F1	–	VDDISC	GPIO	PC22	I/O	–	–	A	LCDDAT18	O	2	PIO, I, PU, ST
								B	GCRS	I	1	
								C	ISC_VSYNC	I	1	
								E	FLEXCOM3_IO4	O	2	
								F	A11	O	2	
H9	–	VDDISC	GPIO	PC23	I/O	–	–	A	LCDDAT19	O	2	PIO, I, PU, ST
								B	GCOL	I	1	
								C	ISC_HSYNC	I	1	
								F	A12	O	2	
G1	–	VDDISC	GPIO_CLK	PC24	I/O	–	–	A	LCDDAT20	O	2	PIO, I, PU, ST
								B	GRX2	I	1	
								C	ISC_MCK	O	1	
								F	A13	O	2	
H8	–	VDDISC	GPIO	PC25	I/O	–	–	A	LCDDAT21	O	2	PIO, I, PU, ST
								B	GRX3	I	1	
								C	ISC_FIELD	I	1	
								F	A14	O	2	
F7	–	VDDIOP2	GPIO	PC26	I/O	–	–	A	LCDDAT22	O	2	PIO, I, PU, ST
								B	GTX2	O	1	
								D	CANTX1	O	1	
								F	A15	O	2	
B10	–	VDDIOP2	GPIO	PC27	I/O	–	–	A	LCDDAT23	O	2	PIO, I, PU, ST
								B	GTX3	O	1	
								C	PCK1	O	2	
								D	CANRX1	I	1	
								E	TWD0	I/O	2	
								F	A16	O	2	
F6	–	VDDIOP2	GPIO	PC28	I/O	–	–	A	LCDPWM	O	2	PIO, I, PU, ST
								B	FLEXCOM4_IO0	I/O	1	
								C	PCK2	O	1	
								E	TWCK0	I/O	2	
								F	A17	O	2	
B9	–	VDDIOP2	GPIO	PC29	I/O	–	–	A	LCDDISP	O	2	PIO, I, PU, ST
								B	FLEXCOM4_IO1	I/O	1	
								F	A18	O	2	
E6	–	VDDIOP2	GPIO	PC30	I/O	–	–	A	LCDVSYNC	O	2	PIO, I, PU, ST
								B	FLEXCOM4_IO2	I/O	1	
								F	A19	O	2	
A11	–	VDDIOP2	GPIO	PC31	I/O	–	–	A	LCDHSYNC	O	2	PIO, I, PU, ST
								B	FLEXCOM4_IO3	O	1	

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
								C	URXD3	I	2	
								F	A20	O	2	
E7	–	VDDIOP2	GPIO_CLK	PD0	I/O	–	–	A	LCDPCK	O	2	PIO, I, PU, ST
								B	FLEXCOM4_IO4	O	1	
								C	UTXD3	O	2	
								D	GTSUCOMP	O	2	
								F	A23	O	2	
C9	–	VDDIOP2	GPIO	PD1	I/O	–	–	A	LCDDEN	O	2	PIO, I, PU, ST
								D	GRXCK	I	2	
								F	A24	O	2	
D8	–	VDDIOP2	GPIO_CLK	PD2	I/O	–	–	A	URXD1	I	1	PIO, I, PU, ST
								D	GTXER	O	2	
								E	ISC_MCK	O	2	
								F	A25	O	2	
J1	–	VDDANA	GPIO_AD	PD3	I/O	–	–	A	UTXD1	O	1	PIO, I, PU, ST
								B	FIQ	I	2	
								D	GCRS	I	2	
								E	ISC_D11	I	2	
								F	NWAIT	I	2	
H7	–	VDDANA	GPIO_AD	PD4	I/O	–	–	A	TWD1	I/O	2	PIO, I, PU, ST
								B	URXD2	I	1	
								D	GCOL	I	2	
								E	ISC_D10	I	2	
								F	NCS0	O	2	
H1	–	VDDANA	GPIO_AD	PD5	I/O	–	–	A	TWCK1	I/O	2	PIO, I, PU, ST
								B	UTXD2	O	1	
								D	GRX2	I	2	
								E	ISC_D9	I	2	
								F	NCS1	O	2	
J2	–	VDDANA	GPIO_AD	PD6	I/O	–	–	A	TCK	I	2	PIO, I, PU, ST
								B	PCK1	O	1	
								D	GRX3	I	2	
								E	ISC_D8	I	2	
								F	NCS2	O	2	
H6	H5	VDDANA	GPIO_AD	PD7	I/O	–	–	A	TDI	I	2	PIO, I, PU, ST
								C	UTMI_RXVAL	O	1	
								D	GTX2	O	2	
								E	ISC_D0	I	2	
								F	NWR1/NBS1	O	2	
K3	J2	VDDANA	GPIO_AD	PD8	I/O	–	–	A	TDO	O	2	PIO, I, PU, ST
								C	UTMI_RXERR	O	1	

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
								D	GTX3	O	2	
								E	ISC_D1	I	2	
								F	NANDRDY	I	2	
J4	G4	VDDANA	GPIO_AD	PD9	I/O	–	–	A	TMS	I	2	PIO, I, PU, ST
								C	UTMI_RXACT	O	1	
								D	GTXCK	I/O	2	
								E	ISC_D2	I	2	
J3	C2	VDDANA	GPIO_AD	PD10	I/O	–	–	A	NTRST	I	2	PIO, I, PU, ST
								C	UTMI_HDIS	O	1	
								D	GTXEN	O	2	
								E	ISC_D3	I	2	
K2	F2	VDDANA	GPIO_AD	PD11	I/O	–	–	A	TIOA1	I/O	3	PIO, I, PU, ST
								B	PCK2	O	2	
								C	UTMI_LS0	O	1	
								D	GRXDV	I	2	
								E	ISC_D4	I	2	
								F	ISC_MCK	O	4	
K9	K4	VDDANA	GPIO_AD	PD12	I/O	–	–	A	TIOB1	I/O	3	PIO, I, PU, ST
								B	FLEXCOM4_IO0	I/O	2	
								C	UTMI_LS1	O	1	
								D	GRXER	I	2	
								E	ISC_D5	I	2	
								F	ISC_D4	I	4	
N1	C1	VDDANA	GPIO_AD	PD13	I/O	–	–	A	TCLK1	I	3	PIO, I, PU, ST
								B	FLEXCOM4_IO1	I/O	2	
								C	UTMI_CDRCPSEL0	I	1	
								D	GRX0	I	2	
								E	ISC_D6	I	2	
								F	ISC_D5	I	4	
K5	H2	VDDANA	GPIO_AD	PD14	I/O	–	–	A	TCK	I	1	A, PU, ST
								B	FLEXCOM4_IO2	I/O	2	
								C	UTMI_CDRCPSEL1	I	1	
								D	GRX1	I	2	
								E	ISC_D7	I	2	
								F	ISC_D6	I	4	
K8	G2	VDDANA	GPIO_AD	PD15	I/O	–	–	A	TDI	I	1	PIO, I, PU, ST
								B	FLEXCOM4_IO3	O	2	
								C	UTMI_CDRCPDIVEN	I	1	
								D	GTX0	O	2	
								E	ISC_PCK	I	2	
								F	ISC_D7	I	4	

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
L1	J1	VDDANA	GPIO_AD	PD16	I/O	–	–	A	TDO	O	1	PIO, I, PU, ST
								B	FLEXCOM4_IO4	O	2	
								C	UTMI_CDRBISTEN	I	1	
								D	GTX1	O	2	
								E	ISC_VSYNC	I	2	
								F	ISC_D8	I	4	
K1	A1	VDDANA	GPIO_AD	PD17	I/O	–	–	A	TMS	I	1	A, PU, ST
								C	UTMI_CDRCPSELDIV	O	1	
								D	GMDC	O	2	
								E	ISC_HSYNC	I	2	
								F	ISC_D9	I	4	
J7	G3	VDDANA	GPIO_AD	PD18	I/O	–	–	A	NTRST	I	1	PIO, I, PU, ST
								D	GMDIO	I/O	2	
								E	ISC_FIELD	I	2	
								F	ISC_D10	I	4	
L8	K2	VDDANA	GPIO_AD	PD19	I/O	AD0	–	A	PCK0	O	1	PIO, I, PU, ST
								B	TWD1	I/O	3	
								C	URXD2	I	3	
								E	I2SC0_CK	I/O	2	
								F	ISC_D11	I	4	
L2	H1	VDDANA	GPIO_AD	PD20	I/O	AD1	–	A	TIOA2	I/O	3	PIO, I, PU, ST
								B	TWCK1	I/O	3	
								C	UTXD2	O	3	
								E	I2SC0_MCK	O	2	
								F	ISC_PCK	I	4	
P1	G1	VDDANA	GPIO_AD	PD21	I/O	AD2	–	A	TIOB2	I/O	3	PIO, I, PU, ST
								B	TWD0	I/O	4	
								C	FLEXCOM4_IO0	I/O	3	
								E	I2SC0_WS	I/O	2	
								F	ISC_VSYNC	I	4	
L6	F1	VDDANA	GPIO_AD	PD22	I/O	AD3	–	A	TCLK2	I	3	PIO, I, PU, ST
								B	TWCK0	I/O	4	
								C	FLEXCOM4_IO1	I/O	3	
								E	I2SC0_DI0	I	2	
								F	ISC_HSYNC	I	4	
T1	E1	VDDANA	GPIO_AD	PD23	I/O	AD4	–	A	URXD2	I	2	PIO, I, PU, ST
								C	FLEXCOM4_IO2	I/O	3	
								E	I2SC0_DO0	O	2	
								F	ISC_FIELD	I	4	
L4	–	VDDANA	GPIO_AD	PD24	I/O	AD5	–	A	UTXD2	O	2	PIO, I, PU, ST
								C	FLEXCOM4_IO3	O	3	

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
L5	–	VDDANA	GPIO_AD	PD25	I/O	AD6	–	A	SPI1_SPCK	I/O	3	PIO, I, PU, ST
								C	FLEXCOM4_IO4	O	3	
R1	–	VDDANA	GPIO_AD	PD26	I/O	AD7	–	A	SPI1_MOSI	I/O	3	PIO, I, PU, ST
								C	FLEXCOM2_IO0	I/O	2	
L7	–	VDDANA	GPIO_AD	PD27	I/O	AD8	–	A	SPI1_MISO	I/O	3	PIO, I, PU, ST
								B	TCK	I	3	
								C	FLEXCOM2_IO1	I/O	2	
L3	–	VDDANA	GPIO_AD	PD28	I/O	AD9	–	A	SPI1_NPCS0	I/O	3	PIO, I, PU, ST
								B	TDI	I	3	
								C	FLEXCOM2_IO2	I/O	2	
M2	–	VDDANA	GPIO_AD	PD29	I/O	AD10	–	A	SPI1_NPCS1	O	3	PIO, I, PU, ST
								B	TDO	O	3	
								C	FLEXCOM2_IO3	O	2	
								D	TIOA3	I/O	3	
								E	TWD0	I/O	3	
M9	–	VDDANA	GPIO_AD	PD30	I/O	AD11	–	A	SPI1_NPCS2	O	3	PIO, I, PU, ST
								B	TMS	I	3	
								C	FLEXCOM2_IO4	O	2	
								D	TIOB3	I/O	3	
								E	TWCK0	I/O	3	
M8	–	VDDANA	GPIO	PD31	I/O	–	–	A	ADTRG	I	1	PIO, I, PU, ST
								B	NTRST	I	3	
								C	IRQ	I	4	
								D	TCLK3	I	3	
								E	PCK0	O	2	
L9	L1	VDDANA	–	ADVREF	I	–	–	–	–	–	–	–
K4, J5	K3, L2	VDDANA	power	VDDANA	I	–	–	–	–	–	–	–
J6, M1	L3, K1	GNDANA	ground	GNDANA	I	–	–	–	–	–	–	–
J10, F11	K12, F12	VDDIODDR	DDR	DDR_VREF	–	–	–	–	–	–	–	–
L10, L14, J8, H10, G12, E11, E8	F10, E8, E9, E10, G12, H12, J12	VDDIODDR	power	VDDIODDR	I	–	–	–	–	–	–	–
K10, M14, J9, G10, H12, E10, F8	K11, J11, F9, C10, E11, F8, F11, G13, H13	GNDIODDR	ground	GNDIODDR	I	–	–	–	–	–	–	–
H2, U3, P7, L12, E9, D7	G7, H4, D14, E14, L5	VDDCORE	power	VDDCORE	I	–	–	–	–	–	–	–
E12, F12, J11, K11, K6, K7	G11, E12, E13, H3, H7, H8, J3	GNDCORE	ground	GNDCORE	I	–	–	–	–	–	–	–
D4, F3	F4, E4	VDDIOP0	power	VDDIOP0	I	–	–	–	–	–	–	–
E3, F2	E5, F5	GNDIOP0	ground	GNDIOP0	I	–	–	–	–	–	–	–
N12, P12	N9, N10	VDDIOP1	power	VDDIOP1	I	–	–	–	–	–	–	–
M12, P11	M9, M10	GNDIOP1	ground	GNDIOP1	I	–	–	–	–	–	–	–
D9	–	VDDIOP2	power	VDDIOP2	I	–	–	–	–	–	–	–

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
D6	–	GNDIOP2	ground	GNDIOP2	I	–	–	–	–	–	–	–
N8	J7	VDDSDMMC	power	VDDSDMMC	I	–	–	–	–	–	–	–
R8	J8	GNDSDMMC	ground	GNDSDMMC	I	–	–	–	–	–	–	–
H3	–	VDDISC	power	VDDISC	I	–	–	–	–	–	–	–
H5	–	GNDISC	ground	GNDISC	I	–	–	–	–	–	–	–
N13	M13	VDDFUSE	power	VDDFUSE	I	–	–	–	–	–	–	–
R5	P4	VDDPLLA	power	VDDPLLA	I	–	–	–	–	–	–	–
T5	L6	GNDPLLA	ground	GNDPLLA	I	–	–	–	–	–	–	–
M4	K6	VDDAUDIOPLL	power	VDDAUDIOPLL	I	–	–	–	–	–	–	–
T3	J6	GNDDPLL	ground	GNDDPLL	I	–	–	–	–	–	–	–
T4	H6	GNDAUDIOPLL	ground	GNDAUDIOPLL	I	–	–	–	–	–	–	–
T8	P1	VDDAUDIOPLL	–	CLK_AUDIO	–	–	–	–	–	–	–	–
U9	N5	VDDOSC	–	XIN	–	–	–	–	–	–	–	–
U8	P5	VDDOSC	–	XOUT	–	–	–	–	–	–	–	–
N6	M7	VDDOSC	–	VDDOSC	–	–	–	–	–	–	–	–
P5	N6	GNDOSC	power	GNDOSC	I	–	–	–	–	–	–	–
P6	M6	VDDUTMII	power	VDDUTMII	I	–	–	–	–	–	–	–
R7	–	VDDHSIC	power	VDDHSIC	I	–	–	–	–	–	–	–
M6	L7	GNDUTMII	power	GNDUTMII	I	–	–	–	–	–	–	–
U10	N7	VDDUTMII	–	HHSDPA	I	–	–	–	–	–	–	–
T10	P7	VDDUTMII	–	HHSDMA	–	–	–	–	–	–	–	–
U11	N8	VDDUTMII	–	HHSDPB	–	–	–	–	–	–	–	–
T11	P8	VDDUTMII	–	HHSDMB	–	–	–	–	–	–	–	–
T12	–	VDDHSIC	–	HHSDPDATC	–	–	–	–	–	–	–	–
U12	–	VDDHSIC	–	HHSDMSTRC		–	–	–	–	–	–	–
M7	K7	VDDUTMIC	power	VDDUTMIC	I	–	–	–	–	–	–	–
R6	G5	GNDUTMIC	power	GNDUTMIC	I	–	–	–	–	–	–	–
T6	P6	VDDUTMIC	–	VBG	–	–	–	–	–	–	–	–
R4	D1	VDDBU	–	TST	–	–	–	–	–	–	–	–
T7	J5	VDDBU	–	NRST	–	–	–	–	–	–	–	–
R3	N3	VDDBU	–	JTAGSEL	–	–	–	–	–	–	–	–
R2	N1	VDDBU	–	WKUP	–	–	–	–	–	–	–	–
N2	–	VDDBU	–	RXD	–	–	–	–	–	–	–	–
T2	B1	VDDBU	–	SHDN	–	–	–	–	–	–	–	–
P3	N4	VDDBU	–	PIOBU0	–	–	–	–	–	–	–	–
M3	L4	VDDBU	–	PIOBU1	–	–	–	–	–	–	–	–
P2	M3	VDDBU	–	PIOBU2	–	–	–	–	–	–	–	–
P4	M4	VDDBU	–	PIOBU3	–	–	–	–	–	–	–	–
N4	J4	VDDBU	–	PIOBU4	–	–	–	–	–	–	–	–
M5	M5	VDDBU	–	PIOBU5	–	–	–	–	–	–	–	–
N5	–	VDDBU	–	PIOBU6	–	–	–	–	–	–	–	–