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32-BIT ARM-BASED MICROPROCESSORS

SAMA5D2 Series
SAMA5D21 /22 /23 /24 /26 /27 /28

Introduction

The SAMA5D2 series is a high-performance, ultra-low-power ARM® Cortex®-A5 processor-based MPU running up to 500 MHz, with support for multiple memories such as DDR2, DDR3, DDR3L, LPDDR1, LPDDR2, LPDDR3, and QSPI Flash. The devices integrate powerful peripherals for connectivity and user interface applications, and offer advanced security functions (ARM TrustZone®, tamper detection, secure data storage, etc.), as well as high-performance crypto-processors AES, SHA and TRNG.

The SAMA5D2 series is delivered with a free Linux distribution and bare metal C examples.

Features

- ARM Cortex-A5 core
  - ARMv7-A architecture
  - ARM TrustZone
  - NEON™ Media Processing Engine
  - Up to 500 MHz
  - ETM/ETB 8 Kbytes
- Memory Architecture
  - Memory Management Unit
  - 32-Kbyte L1 data cache, 32-Kbyte L1 instruction cache
  - 128-Kbyte L2 cache configurable to be used as an internal SRAM
  - One 128-Kbyte scrambled internal SRAM
  - One 160-Kbyte internal ROM
    - 64-Kbyte scrambled and maskable ROM embedding boot loader/ Secure boot loader
    - 96-Kbyte unscrambled, unmaskable ROM for NAND Flash BCH ECC table
  - High-bandwidth scramblable 16-bit or 32-bit Double Data Rate (DDR) multiport dynamic RAM controller supporting up to 512 Mbyte 8-bank DDR2/DDR3 (DLL off only) / DDR3L (DLL off only) / LPDDR1/LPDDR2/LPDDR3, including “on-the-fly” encryption/decryption path
  - 8-bit SLC/MLC NAND controller, with up to 32-bit Error Correcting Code (PMECC)
- System running up to 166 MHz in typical conditions
  - Reset controller, shutdown controller, periodic interval timer, independent watchdog timer and secure Real-Time Clock (RTC) with clock calibration
  - One 600 to 1200 MHz PLL for the system and one 480 MHz PLL optimized for USB high speed
  - Digital fractional PLL for audio (11.2896 MHz and 12.288 MHz)
  - Internal low-power 12 MHz RC and 32 KHz typical RC
  - Selectable 32.768-Hz low-power oscillator and 8 to 24 MHz oscillator
  - 51 DMA Channels including two 16-channel 64-bit Central DMA Controllers
  - 64-bit Advanced Interrupt Controller (AIC)
  - 64-bit Secure Advanced Interrupt Controller (SAIC)
  - Three programmable external clock signals
- Low-Power Modes
  - Ultra Low-power mode with fast wakeup capability
  - Low-power Backup mode with 5-Kbyte SRAM and SleepWalking™ features
    - Wakeup from up to nine wakeup pins, UART reception, analog comparison
    - Fast wakeup capability

        - Extended Backup mode with DDR in Self-Refresh mode
- Peripherals
  - LCD TFT controller up to 1024x768, with four overlays, rotation, post-processing and alpha blending, 24-bit parallel RGB
  - ITU-R BT. 601/656/1120 Image Sensor Controller (ISC) supporting up to 5 M-pixel sensors with a parallel 12-bit interface for Raw Bayer, YCbCr, Monochrome and JPEG-compressed sensor interface
  - Two Synchronous Serial Controllers (SSC), two Inter-IC Sound Controllers (I^2SC), and one Stereo Class D amplifier
  - One Peripheral Touch Controller (PTC) with up to 8 X-lines and 8 Y-lines (64-channel capacitive touch)
  - One Pulse Density Modulation Interface Controller (PDMIC)
  - One USB high-speed device port (UDPHS) and one USB high-speed host port or two USB high-speed host ports (UHPHS)
  - One USB high-speed host port with a High-Speed Inter-Chip (HSIC) interface
  - One 10/100 Ethernet MAC (GMAC)
        - Energy efficiency support (IEEE 802.3az standard)
        - Ethernet AVB support with IEEE802.1AS time stamping
        - IEEE802.1Qav credit-based traffic-shaping hardware support
        - IEEE1588 Precision Time Protocol (PTP)
  - Two high-speed memory card hosts:
        - SDMMC0: SD 3.0, eMMC 4.51, 8 bits
        - SDMMC1: SD 2.0, eMMC 4.41, 4 bits only
  - Two master/slave Serial Peripheral Interfaces (SPI)
  - Two Quad Serial Peripheral Interfaces (QSPI)
  - Five FLEXCOMs (USART, SPI and TWI)
  - Five UARTs
  - Two master CAN-FD (MCAN) controllers with SRAM-based mailboxes, and time- and event-triggered transmission
  - One Rx only UART in backup area (RXLP)
  - One analog comparator (ACC) in backup area
  - Two 2-wire interfaces (TWIHS) up to 400 Kbits/s supporting the I^2C protocol and SMBUS (TWIHS)
  - Two 3-channel 32-bit Timer/Counters (TC), supporting basic PWM modes
  - One full-featured 4-channel 16-bit Pulse Width Modulation (PWM) controller
  - One 12-channel, 12-bit, Analog-to-Digital Converter (ADC) with Resistive TouchScreen capability
- Safety
  - Zero-power Power-On Reset (POR) cells
  - Main crystal clock failure detector
  - Write-protected registers
  - Integrity Check Monitor (ICM) based on SHA256
  - Memory Management Unit
  - Independent watchdog
- Security
  - 5 Kbytes of internal scrambled SRAM:
        - 1 Kbyte non-erasable on tamper detection
        - 4 Kbytes erasable on tamper detection
  - 256 bits of scrambled and erasable registers
  - Up to eight tamper pins for static or dynamic intrusion detections
  - Environmental monitors on specific versions: temperature, voltage, frequency and active die shield(1)
  - Secure Boot Loader(2)
  - On-the-fly AES encryption/decryption on DDR and QSPI memories (AESB)
  - RTC including time-stamping on security intrusions
  - Programmable fuse box with 544 fuse bits (including JTAG protection and BMS)

Note 1: For environmental monitors, refer to the document “SAMA5D23 and SAMA5D28 Environmental Monitors” (document no. 44036), available under Non-Disclosure Agreement (NDA). Contact a Microchip Sales Representative for details.

2: For secure boot strategies, refer to the document “SAMA5D2 Series Secure Boot Strategy” (document no. 44040), available under Non-Disclosure Agreement (NDA). Contact a Microchip Sales Representative for details.

- Hardware cryptography
  - SHA (SHA1, SHA224, SHA256, SHA384, SHA512): compliant with FIPS PUB 180-2
  - AES: 256-, 192-, 128-bit key algorithm, compliant with FIPS PUB 197

  - TDES: two-key or three-key algorithms, compliant with FIPS PUB 46-3
  - True Random Number Generator (TRNG) compliant with NIST Special Publication 800-22 Test Suite and FIPS PUBs 140-2 and 140-3
- Up to 128 I/Os
  - Fully programmable through set/clear registers
  - Multiplexing of up to eight peripheral functions per I/O line
  - Each I/O line can be assigned to a peripheral or used as a general purpose I/O
  - The PIO controller features a synchronous output providing up to 32 bits of data output in one write operation
- Packages
  - 289-ball LFBGA, 14 x 14 mm body, 0.8 mm pitch
  - 256-ball TFBGA, 8 x 8 mm body, 0.4 mm pitch
  - 196-ball TFBGA, 11 x 11 mm body, 0.75 mm pitch

1. Description

The SAMA5D2 Series is a high-performance, power-efficient embedded MPU based on the ARM Cortex-A5 processor. It integrates the ARM NEON SIMD engine for accelerated multimedia and signal processing, a configurable 128-Kbyte L2 cache, a floating point unit for high-precision computing and reliable performance, as well as high data bandwidth architecture. The device features an advanced user interface and connectivity peripherals. Advanced security is provided by powerful cryptographic accelerators, by the ARM TrustZone technology securing access to memories and sensitive peripherals, and by several hardware features that safeguard memory content, authenticate software reliability, detect physical attacks and prevent information leakage during code execution.

The SAMA5D2 features an internal multilayer bus architecture associated with 2 x 16 DMA channels and dedicated DMAs for the communication and interface peripherals required to ensure uninterrupted data transfers with minimal processor overhead. The device supports DDR2, DDR3, DDR3L, LPDDR1, LPDDR2, LPDDR3, and SLC/MLC NAND Flash memory up to 32-bit ECC.

The comprehensive peripheral set includes an LCD TFT controller with overlays for hardware-accelerated image composition, an image sensor controller, audio support through I^2S, SSC, a stereo Class D amplifier and a digital microphone. Connectivity peripherals include a 10/100 EMAC, USBs, CAN-FDs, FLEXCOMs, UARTs, SPIs and two QSPIs, SDIO/SD/e.MMCs, and TWIs/I^2C.

Protection of code and data is provided by automatic scrambling of memories and an Integrity Check Monitor (ICM) to detect any modification of the memory contents. The SAMA5D2 also supports execution of encrypted code (QSPI or one portion of the DDR) with an “on-the-fly” encryption-decryption process.

With its secure design architecture, cryptographic acceleration engines, and secure boot loader, the SAMA5D2 is the ideal solution for point-of-sale (POS), IoT and industrial applications requiring anti-cloning, data protection and secure communication transfer.

SAMA5D2 devices feature three software-selectable low-power modes: Idle, Ultra-low-power and Backup.

In Idle mode, the processor is stopped while all other functions can be kept running.

In Ultra-low-power-mode 0, the processor is stopped while all other functions are clocked at 512 Hz and interrupts or peripherals can be configured to wake up the system based on events, including partial asynchronous wakeup (SleepWalking).

In Ultra-low-power mode 1, all clocks and functions are stopped but some peripherals can be configured to wake up the system based on events, including partial asynchronous wakeup (SleepWalking).

In Backup mode, RTC and wakeup logic are active. The Backup mode can be extended to feature DDR in Self-refresh mode.

SAMA5D2 devices also include an Event System that allows peripherals to receive, react to and send events in Active and Idle modes without processor intervention.

2. Configuration Summary

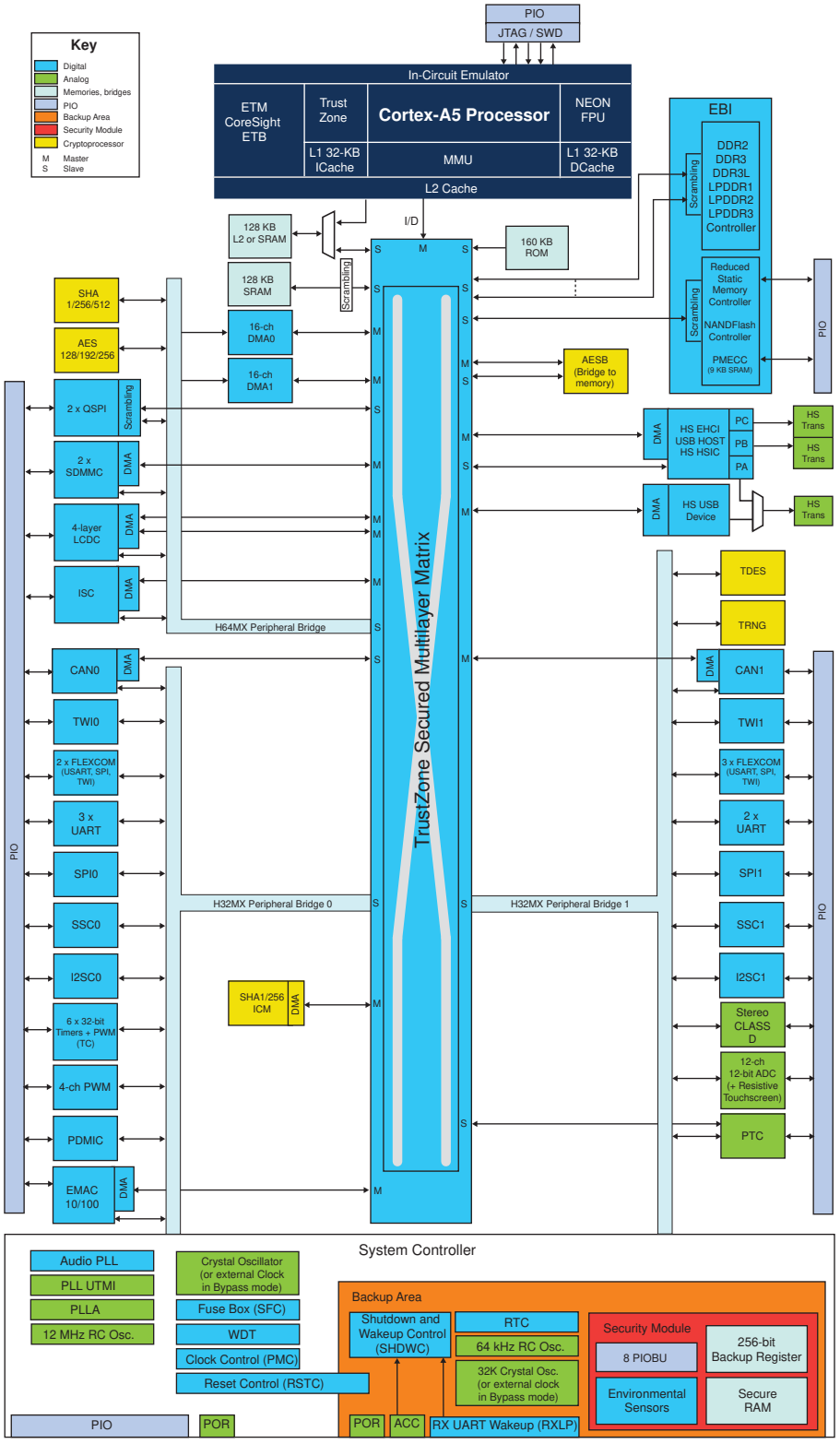
Table 2-1: SAMA5D2 Configuration Summary

Feature	SAMA5D21	SAMA5D22	SAMA5D23	SAMA5D24	SAMA5D26	SAMA5D27	SAMA5D28
Package	TFBGA196			TFBGA256	LFBGA289		
PIOs	72			105	128		
DDR Bus	16-bit			16/32-bit			
SMC	Up to 16-bit						
SRAM	128 Kbytes						
QSPI	2						
LCD	24-bit RGB						
Camera Interface (ISC)	1						
EMAC	1						
PTC	–	4 X-lines x 8 Y-lines		8 X-lines x 8 Y-lines	–	8 X-lines x 8 Y-lines	
CAN	–	1		–		2	
USB	2 (2 Hosts or 1 Host/1 Device)			3 (2 Hosts/ 1 HSIC, or 1 Host/ 1 Device/ 1 HSIC)	2 (2 Hosts or 1 Host/ 1 Device)	3 (2 Hosts/1 HSIC or 1 Host/1 Device/1 HSIC)	
UART/SPI/I^2C	9 / 6 / 6			10 / 7 / 7			
SDIO/SD/MMC	1			2			
I^2S/SSC/ Class D/PDM	2 / 2 / 1 / 1						
ADC Inputs	5			12			
Timers	5			6			
PWM	4 (PWM) + 5 (TC)			4 (PWM) + 6 (TC)			
Tamper Pins	6			2	8		
AESB	–	Yes			–	Yes	
Environmental Monitors, Die Shield	–		Yes	–			Yes

For information on device pin compatibility, see Section 6.2 “Pinouts”.

3. Block Diagram

Figure 3-1: SAMA5D2 Series Block Diagram



Note: Refer to Section 38. “DMA Controller (XDMAC)” for peripheral connections to DMA.

4. Signal Description

Table 4-1 gives details on signal names classified by peripheral.

Table 4-1: Signal Description List

Signal Name	Function	Type	Comments	Active Level
Clocks, Oscillators and PLLs				
XIN	Main Oscillator Input	Input	–	–
XOUT	Main Oscillator Output	Output	–	–
XIN32	Slow Clock Oscillator Input	Input	–	–
XOUT32	Slow Clock Oscillator Output	Output	–	–
CLK_AUDIO	Audio Clock	Output	–	–
VBG	Bias Voltage Reference for USB	Analog	–	–
PCK 0–2	Programmable Clock Output	Output	Reset State: - PIO Input - Internal Pull-up enabled - Schmitt Trigger enabled	–
Shutdown, Wakeup Logic				
SHDN	Shutdown Control	Output	–	–
PIOBU 0–7	Tamper or Wakeup Inputs	Input	–	–
WKUP	Wakeup Input	Input	–	–
ICE and JTAG				
TCK/SWCLK	Test Clock/Serial Wire Clock	Input	–	–
TDI	Test Data In	Input	–	–
TDO	Test Data Out	Output	–	–
TMS/SWDIO	Test Mode Select/Serial Wire Input/Output	I/O	–	–
JTAGSEL	JTAG Selection	Input	–	–
Reset/Test				
NRST	Microprocessor Reset	Input	–	Low
TST	Test Mode Select	Input	–	–
NTRST	Test Reset Signal	Input	–	–
Advanced Interrupt Controller - AIC				
IRQ	External Interrupt Input	Input	–	–
Secured Advanced Interrupt Controller - SAIC				
FIQ	Fast Interrupt Input	Input	–	–
PIO Controller				
PA0–PAxx	Parallel IO Controller	I/O	–	–
PB0–PBxx	Parallel IO Controller	I/O	–	–
PC0–PCxx	Parallel IO Controller	I/O	–	–
PD0–PDxx	Parallel IO Controller	I/O	–	–

Table 4-1: Signal Description List (Continued)

Signal Name	Function	Type	Comments	Active Level
External Bus Interface - EBI				
D[15:0]	Data Bus	I/O	–	–
A[25:0]	Address Bus	Output	–	–
NWAIT	External Wait Signal	Input	–	Low
Static Memory Controller - HSMC				
NCS0–NCS3	Chip Select Lines	Output	–	Low
NWR0–NWR1	Write Signal	Output	–	Low
NRD	Read Signal	Output	–	Low
NWE	Write Enable	Output	–	Low
NBS0–NBS1	Byte Mask Signal	Output	–	Low
NANDOE	NAND Flash Output Enable	Output	–	Low
NANDWE	NAND Flash Write Enable	Output	–	Low
DDR2/DDR3/LPDDR1/LPDDR2/LPDDR3 Controller				
DDR_CK, DDR_CLKN	DDR Differential Clock	Output	–	–
DDR_CKE	DDR Clock Enable	Output	When Backup Self-refresh mode is used, should be tied to GND using 100 KΩ pull-down	High
DDR_CS	DDR Controller Chip Select	Output	–	Low
DDR_BA[2:0]	Bank Select	Output	–	Low
DDR_WE	DDR Write Enable	Output	–	Low
DDR_RAS, DDR_CAS	Row and Column Signal	Output	–	Low
DDR_A[13:0]	DDR Address Bus	Output	–	–
DDR_D[31:0]	DDR Data Bus	I/O/-PD	–	–
DDR_DQS[3:0], DDR_DQSN[3:0]	Differential Data Strobe	I/O- PD	–	–
DDR_DQM[3:0]	Write Data Mask	Output	–	–
DDR_CAL	DDR/LPDDR Calibration	Input	–	–
DDR_VREF	DDR/LPDDR Reference	Input	–	–
DDR_RESETN	DDR3 Active Low Asynchronous Reset	Output	When Backup Self-refresh mode is used, should be tied to VDDIODDR using 100 KΩ pull-up	–
Secure Data Memory Card - SDMMCx [1:0]				
SDMMCx_CD	SDcard / e.MMC Card Detect	Input	–	–
SDMMCx_CMD	SDcard / e.MMC Command line	I/O	–	–
SDMMCx_WP	SDcard Connector Write Protect Signal	Input	–	–
SDMMCx_RSTN	e.MMC Reset Signal	Output	–	–
SDMMCx_1V8SEL	SDcard Signal Voltage Selection	Output	–	–

Table 4-1: Signal Description List (Continued)

Signal Name	Function	Type	Comments	Active Level
SDMMCx_CK	SDcard / e.MMC Clock Signal	Output	–	–
SDMMCx_DAT[7:0]	SDcard / e.MMC Data Lines	I/O	–	–
Flexible Serial Communication Controller - FLEXCOMx [4:0]				
FLEXCOMx_IO0	FLEXCOMx Transmit Data	I/O	–	–
FLEXCOMx_IO1	FLEXCOMx Receive Data	I/O	–	–
FLEXCOMx_IO2	FLEXCOMx Serial Clock	I/O	–	–
FLEXCOMx_IO3	FLEXCOMx Clear To Send / Peripheral Chip Select	I/O	–	–
FLEXCOMx_IO4	FLEXCOMx Request To Send / Peripheral Chip Select	Output	–	–
Universal Asynchronous Receiver Transmitter - UARTx [4..0]				
UTXDx	UARTx Transmit Data	Output	–	–
URXDx	UARTx Receive Data	Input	–	–
Inter-IC Sound Controller - I2SCx [1..0]				
I2SCx_MCK	Master Clock	Output	–	–
I2SCx_CK	Serial Clock	I/O	–	–
I2SCx_WS	I^2S Word Select	I/O	–	–
I2SCx_DI0	Serial Data Input	Input	–	–
I2SCx_DO0	Serial Data Output	Output	–	–
Synchronous Serial Controller - SSCx [1..0]				
TDx	SSC Transmit Data	Output	–	–
RDx	SSC Receive Data	Input	–	–
TKx	SSC Transmit Clock	I/O	–	–
RKx	SSC Receive Clock	I/O	–	–
TFx	SSC Transmit Frame Sync	I/O	–	–
RFx	SSC Receive Frame Sync	I/O	–	–
Timer/Counter - TCx [1..0]				
TCLK[5..0]	TC Channel y External Clock Input	Input	–	–
TIOA[5..0]	TC Channel y I/O Line A	I/O	–	–
TIOB[5..0]	TC Channel y I/O Line B	I/O	–	–
Quad IO SPI - QSPIx [1..0]				
QSPIx_SCK	QSPI Serial Clock	Output	–	–
QSPIx_CS	QSPI Chip Select	Output	–	–
QSPIx_IO[0..3]	QSPI I/O QIO0 is QMOSI Master Out - Slave In QIO1 is QMISO Master In - Slave Out	I/O	–	–

Table 4-1: Signal Description List (Continued)

Signal Name	Function	Type	Comments	Active Level
Serial Peripheral Interface - SPIx [1..0]				
SPIx_MISO	Master In Slave Out	I/O	–	–
SPIx_MOSI	Master Out Slave In	I/O	–	–
SPIx_SPCK	SPI Serial Clock	I/O	–	–
SPIx_NPCS0	SPI Peripheral Chip Select 0	I/O	–	Low
SPIx_NPCS[3..1]	SPI Peripheral Chip Select	Output	–	Low
Two-wire Interface - TWIx [1..0]				
TWDx	Two-wire Serial Data	I/O	–	–
TWCKx	Two-wire Serial Clock	I/O	–	–
Pulse Width Modulation Controller - PWM				
PWMH0–3	PWM Waveform Output High	Output	–	–
PWML0–3	PWM Waveform Output Low	Output	–	–
PWMFI0–1	PWM Fault Inputs	Input	–	–
PWMEXTRG1–2	PWM External Trigger	Input	–	–
USB Host High Speed Port - UHPHS				
HHSDPA	USB Host Port A High Speed Data +	Analog	–	–
HHSDMA	USB Host Port A High Speed Data -	Analog	–	–
HHSDPB	USB Host Port B High Speed Data +	Analog	–	–
HHSDMB	USB Host Port B High Speed Data -	Analog	–	–
USB Device High Speed Port - UDPHS				
DHSDP	USB Device High Speed Data +	Analog	–	–
DHSDM	USB Device High Speed Data -	Analog	–	–
USB High-Speed Inter-Chip Port - HSIC				
HHSTROBE	USB High-Speed Inter-Chip Strobe	I/O	–	–
HHDATA	USB High-Speed Inter-Chip Data	I/O	–	–
Ethernet 10/100 - GMAC				
GREFCK	Reference Clock	Input	–	–
GTXCK	Transmit Clock	Input	–	–
GRXCK	Receive Clock	Input	–	–
GTXEN	Transmit Enable	Output	–	–
GTX0–GTX3	Transmit Data	Output	–	–
GTXER	Transmit Coding Error	Output	–	–
GRXDV	Receive Data Valid	Input	–	–
GRX0–GRX3	Receive Data	Input	–	–
GRXER	Receive Error	Input	–	–
GCRS	Carrier Sense	Input	–	–

Table 4-1: Signal Description List (Continued)

Signal Name	Function	Type	Comments	Active Level
GCOL	Collision Detected	Input	–	–
GMDC	Management Data Clock	Output	–	–
GMDIO	Management Data Input/Output	I/O	–	–
GTSUCOMP	TSU timer comparison valid	Output	–	–
LCD Controller - LCDC				
LCDDAT[23:0]	LCD Data Bus	Output	–	–
LCDVSYNC	LCD Vertical Synchronization	Output	–	–
LCDHSYNC	LCD Horizontal Synchronization	Output	–	–
LCDPCK	LCD Pixel Clock	Output	–	–
LCDDEN	LCD Data Enable	Output	–	–
LCDPWM	LCDPWM for Contrast Control	Output	–	–
LCDDISP	LCD Display ON/OFF	Output	–	–
Touchscreen Analog-to-Digital Converter - ADC				
AD0–11	12 Analog Inputs	Analog	–	–
ADTRG	ADC Trigger	Input	–	–
ADVREF	ADC Reference	Analog	–	–
Secure Box Module - SBM				
PIOBU0–7	Tamper I/Os	I/O	–	–
Image Sensor Controller - ISC				
ISC_D0–ISC_D11	Image Sensor Data	Input	–	–
ISC_HSYNC	Image Sensor Horizontal Synchro	Input	–	–
ISC_VSYNC	Image Sensor Vertical Synchro	Input	–	–
ISC_PCK	Image Sensor Pixel clock	Input	–	–
ISC_MCK	Image Sensor Main clock	Output	–	–
ISC_FIELD	Field identification signal	Input	–	–
Audio Class Amplifier - CLASSD				
CLASSD_L0	CLASSD Left Output L0	Output	–	–
CLASSD_L1	CLASSD Left Output L1	Output	–	–
CLASSD_L2	CLASSD Left Output L2	Output	–	–
CLASSD_L3	CLASSD Left Output L3	Output	–	–
CLASSD_R0	CLASSD Right Output R0	Output	–	–
CLASSD_R1	CLASSD Right Output R1	Output	–	–
CLASSD_R2	CLASSD Right Output R2	Output	–	–
CLASSD_R3	CLASSD Right Output R3	Output	–	–

Table 4-1: Signal Description List (Continued)

Signal Name	Function	Type	Comments	Active Level
Control Area Network - CAN				
CANRXx	CAN Receive	Input	–	–
CANTXx	CAN Transmit	Output	–	–
Peripheral Touch Controller (PTC)				
PTC_X[7..0]	X-lines	I/O	–	–
PTC_Y[7..0]	Y-lines	I	–	–
Pulse Density Modulation Interface Controller - PDMIC				
PDMIC_DAT	PDM Data	Input	–	–
PDMIC_CLK	PDM Clock	Output	–	–

5. Safety and Security Features

5.1 Design for Safety and IEC60730 Class B Certification

5.1.1 Background Information

The IEC 60730 standard encompasses all aspects of appliance design. Annex H of the standard covers the aspects most relevant to microcontrollers. It details the tests and diagnostics which are intended to ensure safe operation of embedded control hardware and software. IEC 60730 defines three classifications for electronic control functions:

- Class A - Control functions which are not intended to be relied upon for safety of the equipment
- Class B - Control functions intended to prevent unsafe operation of the controlled equipment
- Class C - Control functions intended to prevent special hazards such as explosions

Specific design techniques have been used in the SAMA5D2 to ease compliance with the IEC 60730 Class B Certification and to resolve general-purpose safety concerns. This allows reduced software development and code size as well as savings on external hardware circuitry, since built-in self-tests are already embedded in the MPU. Table 5-1 gives the list of peripherals which incorporate these techniques, and details whether these features are applicable for the IEC 60730 Class B Certification or for general-purpose safety considerations.

5.2 Design for Security

The SAMA5D2 embeds peripherals with security features to prevent counterfeiting, to secure external communication, and to authenticate the system.

Table 5-2 provides the list of peripherals and an overview of their security function. For more information, see the sections on each peripheral.

5.3 Safety and IEC 60730 Features

Table 5-1: Safety and IEC 60730 Features List

Peripheral	Component	Fault/Error/Feature	Requirements for Class B IEC 60730[1]	General Safety
PMC	Clock	CPU clock monitoring - Overclocking detection	–	X
		32.768 kHz crystal oscillator frequency monitoring - Abnormal frequency deviation	X	X
		Main crystal oscillator - Crystal failure detection	X	X
PIOC	I/O Periphery	Programmable configuration lock (active until next V_{DDCORE} reset) to protect against further software modifications (intentional or unintentional)	–	X
		Digital I/O - Plausibility check	X	–
ADCC		Analog I/O and ADC converter - Plausibility check	X	–
ICM (SHA)	Memory and Internal Data Path	All internal and external memories such as QSPI, DDR, and all memories on SMC	X	–
NAND Flash Controller ECC		Non-volatile memory - Mutiple error detection (2 to 32)	–	X
System Controller	Supply Monitor	Power supplies - VDDCORE, VDDIO, VDDANA, VDDBU abnormal levels	–	X
WDT, RSTC	Watchdog	Watchdog can be fed by an internal always ON clock - Program counter stuck at faults.	X	X
		Watchdog configuration can be locked (write-protected) - Errant writes (Programming errors, errors introduced by system or hardware failures)	–	X
		Watchdog overflow generates a system reset	X	X
Cortex MMU	Memory Management Unit	Cortex-A5 Memory Management Unit	–	X
MATRIX, AIC, RTC, SYSC, RXLP, ACC, PMC, PIO, MPDDRC, SMC, CLASSD, SSC, TWI, UART, SPI, FLEXCOM, QSPI, TC, PDMIC, ADC	Peripherals	Configuration, Interrupt Enable/Disable, Control registers can be independently write-protected - Errant writes (Programming errors, errors introduced by system or hardware failures)	–	X

Table 5-1: Safety and IEC 60730 Features List (Continued)

Peripheral	Component	Fault/Error/Feature	Requirements for Class B IEC 60730[1]	General Safety
PWM, PIO	PWM	Fault inputs can be configured to put the PWM outputs in Safe mode - Programming errors, errors introduced by system or hardware failures	–	X
		PIO controller can lock the PWM I/O - Programming errors, errors introduced by system or hardware failures	–	X
		Fault inputs can be external (IO) or internal (ADC, TIMER, ACC, etc.) - Programming errors, errors introduced by system or hardware failures	–	X

Note 1: Class B IEC 60730 Requirements. Annex H - Table H.1 (H.11.12.7 of edition 3).

5.4 Security Features

Table 5-2: Security Features

Peripheral	Function	Description	Comments
TrustZone	Security Enclave	Partition secure/non-secure world	ARM technology
Cortex MMU	Memory Management Unit	Cortex-A5 Memory Management Unit	–
PIO	I/O Control/ Peripheral Access	When a peripheral is not selected (PIO-controlled), I/O lines have no access to the peripheral.	–
	Freeze	Capability to freeze either the functional part or the physical part of the configuration.	Once the freeze command is issued, no modifications to the current configuration are possible. Only a hardware reset allows a change to the configuration.
Classical Atmel Software Crypto LIbrary (CASCL)	Cryptography	Software ECC (Asymmetric key algorithm, elliptic curves)	Software library(1)
		Software RSA (Asymmetric key algorithm)	
TDES, TRNG		Hardware-accelerated Triple DES	FIPS-compliant(3)
		True Random Number Generator	
AES, SHA		Hardware-accelerated AES up to 256 bits	
		SHA up to 512 and HMAC-SHA	
	Secure Boot	Code encrypted/decrypted, Trusted Code Authentication	Hardware SHA (HMAC) + Software RSA or AES Hardware (CMAC)
AESB	AES on-the-fly	On-the-fly encryption/decryption for DDR and QSPI memories	AES128
Memories	Scrambling	On-the-fly scrambling/unscrambling for memories	All internal and external memories such as QSPI, DDR, and all memories on SMC
ICM	Memory Integrity Check Monitoring	Uses a hardware Secure Hash Algorithm (up to SHA256)	More robust than CRC. All internal and external memories such as QSPI, DDR, and all memories on SMC can be monitored

Table 5-2: Security Features (Continued)

Peripheral	Function	Description	Comments
SECUMOD	JTAG	JTAG entry monitor	These tamper pins (JTAG, test, PIOBUs, monitors, etc.) can be configured to immediately erase Backup memories (BUSRAM4KB and BUREG256b), or generate an interrupt or a wakeup signal.
	Test	Test entry monitor	
	Active Shield(2)	Die Active Shield	
	Voltage Monitoring(2)	VDDBU monitoring	
		VDDCORE monitoring	
	Temperature Monitoring(2)	Temperature monitoring	
	Frequency Monitoring(2)	32.768 kHz crystal oscillator monitoring	
		CPU clock monitoring	
	IO Tamper Pin	8 tamper detection pins. Active and Dynamic modes supported.	
	Secure Backup SRAM	5 Kbytes scrambled and non-imprinting avoiding data persistance	4 Kbytes erasable on tamper detection
	Secure Backup Registers	256-bit register bank, scrambled	Erasable on tamper detection
RTC	RTC	Timestamping of tamper events. Protection against bad configuration (invalid entry for date and time are impossible)	All events are logged in the RTC. Timestamping gives the source of the reset/erase memory/interruption
		RTC robustness against glitch attack on 32 kHz crystal oscillator	–
Secure Fuse	JTAG Access Control	Disable JTAG access by fuse bit	–
	Secure Debug Disable	JTAG debug allowed in Normal mode only, not in Secure mode	TrustZone

Note 1: A PCI-certified Atmel Software Crypto Library (ASCL) is available under NDA.

2: Available on SAMA5D23 and SAMA5D28 only. For environmental monitors, refer to the document "*SAMA5D23 and SAMA5D28 Environmental Monitors*" (document no. 44036), available under Non-Disclosure Agreement (NDA). Contact a Microchip sales representative for details.

3: Refer to the sections on each peripheral for details on FIPS compliancy.

6. Package and Pinout

6.1 Packages

The SAMA5D2 is available in the packages listed in Table 6-1.

Table 6-1: SAMA5D2 Packages

Package Name	Pin Count	Ball Pitch
LFBGA289	289	0.8 mm
TFBGA256	256	0.4 mm
TFBGA196	196	0.75 mm

The package mechanical characteristics are described in Section 67. “Mechanical Characteristics”.

6.2 Pinouts

Pinouts are provided in

- Table 6-2 “Pin Description”
- Table 6-3 “Pin Description (SAMA5D23 pins different from those in Table 6-2 “Pin Description”)”
- Table 6-4 “Pin Description (SAMA5D28B/C pins different from those in Table 6-2 “Pin Description”)”.

Note: I/Os for each peripheral are grouped into IO sets, listed in the column ‘IO Set’ in the pinout tables below. For all peripherals, it is mandatory to use I/Os that belong to the same IO set. The timings are not guaranteed when IOs from different IO sets are mixed.

Table 6-2: Pin Description

289-pin BGA	256-pin BGA	196-pin BGA	Power Rail	I/O Type	Primary		Alternate		PIO peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1][2]
					Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
U11	R10	–	VDDSDMMC	GPIO_EMMC	PA0	I/O	–	–	A	SDMMC0_CK	I/O	1	PIO, I, PU, ST
									B	QSPI0_SCK	O	1	
									F	D0	I/O	2	
P10	R9	–	VDDSDMMC	GPIO_EMMC	PA1	I/O	–	–	A	SDMMC0_CMD	I/O	1	PIO, I, PU, ST
									B	QSPI0_CS	O	1	
									F	D1	I/O	2	
T11	U11	–	VDDSDMMC	GPIO_EMMC	PA2	I/O	–	–	A	SDMMC0_DAT0	I/O	1	PIO, I, PU, ST
									B	QSPI0_IO0	I/O	1	
									F	D2	I/O	2	
R10	P10	–	VDDSDMMC	GPIO_EMMC	PA3	I/O	–	–	A	SDMMC0_DAT1	I/O	1	PIO, I, PU, ST
									B	QSPI0_IO1	I/O	1	
									F	D3	I/O	2	
U12	P11	–	VDDSDMMC	GPIO_EMMC	PA4	I/O	–	–	A	SDMMC0_DAT2	I/O	1	PIO, I, PU, ST
									B	QSPI0_IO2	I/O	1	
									F	D4	I/O	2	
T12	V11	–	VDDSDMMC	GGPIO_EMMC	PA5	I/O	–	–	A	SDMMC0_DAT3	I/O	1	PIO, I, PU, ST
									B	QSPI0_IO3	I/O	1	
									F	D5	I/O	2	

Table 6-2: Pin Description (Continued)

289-pin BGA	256-pin BGA	196-pin BGA	Power Rail	I/O Type	Primary		Alternate		PIO peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1][2]
					Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
R12	U12	–	VDDSDMMC	GPIO_EMMC	PA6	I/O	–	–	A	SDMMC0_DAT4	I/O	1	PIO, I, PU, ST
									B	QSPI1_SCK	O	1	
									D	TIOA5	I/O	1	
									E	FLEXCOM2_IO0	I/O	1	
									F	D6	I/O	2	
T13	V12	–	VDDSDMMC	GPIO_EMMC	PA7	I/O	–	–	A	SDMMC0_DAT5	I/O	1	PIO, I, PU, ST
									B	QSPI1_IO0	I/O	1	
									D	TIOB5	I/O	1	
									E	FLEXCOM2_IO1	I/O	1	
									F	D7	I/O	2	
N10	N11	–	VDDSDMMC	GPIO_EMMC	PA8	I/O	–	–	A	SDMMC0_DAT6	I/O	1	PIO, I, PU, ST
									B	QSPI1_IO1	I/O	1	
									D	TCLK5	I	1	
									E	FLEXCOM2_IO2	I/O	1	
									F	NWE/NANDWE	O	2	
N11	P12	–	VDDSDMMC	GPIO_EMMC	PA9	I/O	–	–	A	SDMMC0_DAT7	I/O	1	PIO, I, PU, ST
									B	QSPI1_IO2	I/O	1	
									D	TIOA4	I/O	1	
									E	FLEXCOM2_IO3	O	1	
									F	NCS3	O	2	
U13	U13	–	VDDSDMMC	GPIO_EMMC	PA10	I/O	–	–	A	SDMMC0_RSTN	O	1	PIO, I, PU, ST
									B	QSPI1_IO3	I/O	1	
									D	TIOB4	I/O	1	
									E	FLEXCOM2_IO4	O	1	
									F	A21/NANDALE	O	2	
P15	R14	–	VDDIOP1	GPIO	PA11	I/O	–	–	A	SDMMC0_1V8SEL	O	1	PIO, I, PU, ST
									B	QSPI1_CS	O	1	
									D	TCLK4	I	1	
									F	A22/NANDCLE	O	2	
N15	N13	–	VDDIOP1	GPIO	PA12	I/O	–	–	A	SDMMC0_WP	I	1	PIO, I, PU, ST
									B	IRQ	I	1	
									F	NRD/NANDOE	O	2	
P16	P14	–	VDDIOP1	GPIO	PA13	I/O	–	–	A	SDMMC0_CD	I	1	PIO, I, PU, ST
									E	FLEXCOM3_IO1	I/O	1	
									F	D8	I/O	2	

Table 6-2: Pin Description (Continued)

289-pin BGA	256-pin BGA	196-pin BGA	Power Rail	I/O Type	Primary		Alternate		PIO peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1][2]
					Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
M14	P17	–	VDDIOP1	GPIO_QSPI	PA14	I/O	–	–	A	SPI0_SPCK	I/O	1	PIO, I, PU, ST
									B	TK1	I/O	1	
									C	QSPI0_SCK	O	2	
									D	I2SC1_MCK	O	2	
									E	FLEXCOM3_IO2	I/O	1	
									F	D9	I/O	2	
N16	R18	–	VDDIOP1	GPIO	PA15	I/O	–	–	A	SPI0_MOSI	I/O	1	PIO, I, PU, ST
									B	TF1	I/O	1	
									C	QSPI0_CS	O	2	
									D	I2SC1_CK	I/O	2	
									E	FLEXCOM3_IO0	I/O	1	
									F	D10	I/O	2	
M10	N15	–	VDDIOP1	GPIO_IO	PA16	I/O	–	–	A	SPI0_MISO	I/O	1	PIO, I, PU, ST
									B	TD1	O	1	
									C	QSPI0_IO0	I/O	2	
									D	I2SC1_WS	I/O	2	
									E	FLEXCOM3_IO3	O	1	
									F	D11	I/O	2	
N17	P18	–	VDDIOP1	GPIO_IO	PA17	I/O	–	–	A	SPI0_NPCS0	I/O	1	PIO, I, PU, ST
									B	RD1	I	1	
									C	QSPI0_IO1	I/O	2	
									D	I2SC1_DI0	I	2	
									E	FLEXCOM3_IO4	O	1	
									F	D12	I/O	2	
U14	M9	L9	VDDIOP1	GPIO_IO	PA18	I/O	–	–	A	SPI0_NPCS1	O	1	PIO, I, PU, ST
									B	RK1	I/O	1	
									C	QSPI0_IO2	I/O	2	
									D	I2SC1_DO0	O	2	
									E	SDMMC1_DAT0	I/O	1	
									F	D13	I/O	2	
T14	V13	N9	VDDIOP1	GPIO_IO	PA19	I/O	–	–	A	SPI0_NPCS2	O	1	PIO, I, PU, ST
									B	RF1	I/O	1	
									C	QSPI0_IO3	I/O	2	
									D	TIOA0	I/O	1	
									E	SDMMC1_DAT1	I/O	1	
									F	D14	I/O	2	

Table 6-2: Pin Description (Continued)

289-pin BGA	256-pin BGA	196-pin BGA	Power Rail	I/O Type	Primary		Alternate		PIO peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1][2]
					Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
P12	L9	M9	VDDIOP1	GPIO_IO	PA20	I/O	–	–	A	SPI0_NPCS3	O	1	PIO, I, PU, ST
									D	TIOB0	I/O	1	
									E	SDMMC1_DAT2	I/O	1	
									F	D15	I/O	2	
R13	M10	M10	VDDIOP1	GPIO_IO	PA21	I/O	–	–	A	IRQ	I	2	PIO, I, PU, ST
									B	PCK2	O	3	
									D	TCLK0	I	1	
									E	SDMMC1_DAT3	I/O	1	
									F	NANDRDY	I	2	
U15	V14	P9	VDDIOP1	GPIO_QSPI	PA22	I/O	–	–	A	FLEXCOM1_IO2	I/O	1	PIO, I, PU, ST
									B	D0	I/O	1	
									C	TCK	I	4	
									D	SPI1_SPCK	I/O	2	
									E	SDMMC1_CK	I/O	1	
									F	QSPI0_SCK	O	3	
U16	U14	P10	VDDIOP1	GPIO	PA23	I/O	–	–	A	FLEXCOM1_IO1	I/O	1	PIO, I, PU, ST
									B	D1	I/O	1	
									C	TDI	I	4	
									D	SPI1_MOSI	I/O	2	
									F	QSPI0_CS	O	3	
T15	R13	N10	VDDIOP1	GPIO_IO	PA24	I/O	–	–	A	FLEXCOM1_IO0	I/O	1	PIO, I, PU, ST
									B	D2	I/O	1	
									C	TDO	O	4	
									D	SPI1_MISO	I/O	2	
									F	QSPI0_IO0	I/O	3	
U17	U15	L10	VDDIOP1	GPIO_IO	PA25	I/O	–	–	A	FLEXCOM1_IO3	O	1	PIO, I, PU, ST
									B	D3	I/O	1	
									C	TMS	I	4	
									D	SPI1_NPCS0	I/O	2	
									F	QSPI0_IO1	I/O	3	
P13	L10	P11	VDDIOP1	GPIO_IO	PA26	I/O	–	–	A	FLEXCOM1_IO4	O	1	PIO, I, PU, ST
									B	D4	I/O	1	
									C	NTRST	I	4	
									D	SPI1_NPCS1	O	2	
									F	QSPI0_IO2	I/O	3	

Table 6-2: Pin Description (Continued)

289-pin BGA	256-pin BGA	196-pin BGA	Power Rail	I/O Type	Primary		Alternate		PIO peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1][2]
					Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
T16	V17	P12	VDDIOP1	GPIO_IO	PA27	I/O	–	–	A	TIOA1	I/O	2	PIO, I, PU, ST
									B	D5	I/O	1	
									C	SPI0_NPCS2	O	2	
									D	SPI1_NPCS2	O	2	
									E	SDMMC1_RSTN	O	1	
									F	QSPI0_IO3	I/O	3	
R16	U16	M11	VDDIOP1	GPIO	PA28	I/O	–	–	A	TIOB1	I/O	2	PIO, I, PU, ST
									B	D6	I/O	1	
									C	SPI0_NPCS3	O	2	
									D	SPI1_NPCS3	O	2	
									E	SDMMC1_CMD	I/O	1	
									F	CLASSD_L0	O	1	
T17	U17	N11	VDDIOP1	GPIO	PA29	I/O	–	–	A	TCLK1	I	2	PIO, I, PU, ST
									B	D7	I/O	1	
									C	SPI0_NPCS1	O	2	
									E	SDMMC1_WP	I	1	
									F	CLASSD_L1	O	1	
R15	V18	N12	VDDIOP1	GPIO	PA30	I/O	–	–	B	NWE/NANDWE	O	1	PIO, I, PU, ST
									C	SPI0_NPCS0	I/O	2	
									D	PWMH0	O	1	
									E	SDMMC1_CD	I	1	
									F	CLASSD_L2	O	1	
R17	U18	M12	VDDIOP1	GPIO	PA31	I/O	–	–	B	NCS3	O	1	PIO, I, PU, ST
									C	SPI0_MISO	I/O	2	
									D	PWML0	O	1	
									F	CLASSD_L3	O	1	
J8	G9	A6	VDDIOP0	GPIO	PB0	I/O	–	–	B	A21/NANDALE	O	1	PIO, I, PU, ST
									C	SPI0_MOSI	I/O	2	
									D	PWMH1	O	1	
A8	A7	A5	VDDIOP0	GPIO	PB1	I/O	–	–	B	A22/NANDCLE	O	1	PIO, I, PU, ST
									C	SPI0_SPCK	I/O	2	
									D	PWML1	O	1	
									F	CLASSD_R0	O	1	
A7	B7	B6	VDDIOP0	GPIO	PB2	I/O	–	–	B	NRD/NANDOE	O	1	PIO, I, PU, ST
									D	PWMFI0	I	1	
									F	CLASSD_R1	O	1	

Table 6-2: Pin Description (Continued)

289-pin BGA	256-pin BGA	196-pin BGA	Power Rail	I/O Type	Primary		Alternate		PIO peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1][2]
					Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
A6	B6	B5	VDDIOP0	GPIO	PB3	I/O	–	–	A	URXD4	I	1	PIO, I, PU, ST
									B	D8	I/O	1	
									C	IRQ	I	3	
									D	PWMEXTRG1	I	1	
									F	CLASSD_R2	O	1	
B6	A6	A4	VDDIOP0	GPIO	PB4	I/O	–	–	A	UTXD4	O	1	PIO, I, PU, ST
									B	D9	I/O	1	
									C	FIQ	I	4	
									F	CLASSD_R3	O	1	
B7	D7	D6	VDDIOP0	GPIO_QSPI	PB5	I/O	–	–	A	TCLK2	I	1	PIO, I, PU, ST
									B	D10	I/O	1	
									C	PWMH2	O	1	
									D	QSPI1_SCK	O	2	
									F	GTSUCOMP	O	3	
C7	B5	A3	VDDIOP0	GPIO	PB6	I/O	–	–	A	TIOA2	I/O	1	PIO, I, PU, ST
									B	D11	I/O	1	
									C	PWML2	O	1	
									D	QSPI1_CS	O	2	
									F	GTXER	O	3	
C6	A5	B4	VDDIOP0	GPIO_IO	PB7	I/O	–	–	A	TIOB2	I/O	1	PIO, I, PU, ST
									B	D12	I/O	1	
									C	PWMH3	O	1	
									D	QSPI1_IO0	I/O	2	
									F	GRXCK	I	3	
A5	E7	A2	VDDIOP0	GPIO_IO	PB8	I/O	–	–	A	TCLK3	I	1	PIO, I, PU, ST
									B	D13	I/O	1	
									C	PWML3	O	1	
									D	QSPI1_IO1	I/O	2	
									F	GCRS	I	3	
A4	F6	B3	VDDIOP0	GPIO_IO	PB9	I/O	–	–	A	TIOA3	I/O	1	PIO, I, PU, ST
									B	D14	I/O	1	
									C	PWMFI1	I	1	
									D	QSPI1_IO2	I/O	2	
									F	GCOL	I	3	

Table 6-2: Pin Description (Continued)

289-pin BGA	256-pin BGA	196-pin BGA	Power Rail	I/O Type	Primary		Alternate		PIO peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1][2]
					Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
H8	D6	A1	VDDIOP0	GPIO_IO	PB10	I/O	–	–	A	TIOB3	I/O	1	PIO, I, PU, ST
									B	D15	I/O	1	
									C	PWMEXTRG2	I	1	
									D	QSPI1_IO3	I/O	2	
									F	GRX2	I	3	
B5	A4	B1	VDDIOP0	GPIO	PB11	I/O	–	–	A	LCDDAT0	O	1	PIO, I, PU, ST
									B	A0/NBS0	O	1	
									C	URXD3	I	3	
									D	PDMIC_DAT		2	
									F	GRX3	I	3	
D6	B3	B2	VDDIOP0	GPIO	PB12	I/O	–	–	A	LCDDAT1	O	1	PIO, I, PU, ST
									B	A1	O	1	
									C	UTXD3	O	3	
									D	PDMIC_CLK		2	
									F	GTX2	O	3	
B4	A3	C1	VDDIOP0	GPIO	PB13	I/O	–	–	A	LCDDAT2	O	1	PIO, I, PU, ST
									B	A2	O	1	
									C	PCK1	O	3	
									F	GTX3	O	3	
C5	B4	D5	VDDIOP0	GPIO_QSPI	PB14	I/O	–	–	A	LCDDAT3	O	1	PIO, I, PU, ST
									B	A3	O	1	
									C	TK1	I/O	2	
									D	I2SC1_MCK	O	1	
									E	QSPI1_SCK	O	3	
									F	GTXCK	I/O	3	
H7	G8	E5	VDDIOP0	GPIO	PB15	I/O	–	–	A	LCDDAT4	O	1	PIO, I, PU, ST
									B	A4	O	1	
									C	TF1	I/O	2	
									D	I2SC1_CK	I/O	1	
									E	QSPI1_CS	O	3	
									F	GTXEN	O	3	
D5	E5	C5	VDDIOP0	GPIO_IO	PB16	I/O	–	–	A	LCDDAT5	O	1	PIO, I, PU, ST
									B	A5	O	1	
									C	TD1	O	2	
									D	I2SC1_WS	I/O	1	
									E	QSPI1_IO0	I/O	3	
									F	GRXDV	I	3	

Table 6-2: Pin Description (Continued)

289-pin BGA	256-pin BGA	196-pin BGA	Power Rail	I/O Type	Primary		Alternate		PIO peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1][2]
					Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
C4	G7	C2	VDDIOP0	GPIO_IO	PB17	I/O	–	–	A	LCDDAT6	O	1	PIO, I, PU, ST
									B	A6	O	1	
									C	RD1	I	2	
									D	I2SC1_DI0	I	1	
									E	QSPI1_IO1	I/O	3	
									F	GRXER	I	3	
A3	A2	D4	VDDIOP0	GPIO_IO	PB18	I/O	–	–	A	LCDDAT7	O	1	PIO, I, PU, ST
									B	A7	O	1	
									C	RK1	I/O	2	
									D	I2SC1_DO0	O	1	
									E	QSPI1_IO2	I/O	3	
									F	GRX0	I	3	
D4	H7	C4	VDDIOP0	GPIO_IO	PB19	I/O	–	–	A	LCDDAT8	O	1	PIO, I, PU, ST
									B	A8	O	1	
									C	RF1	I/O	2	
									D	TIOA3	I/O	2	
									E	QSPI1_IO3	I/O	3	
									F	GRX1	I	3	
B3	A1	C3	VDDIOP0	GPIO	PB20	I/O	–	–	A	LCDDAT9	O	1	PIO, I, PU, ST
									B	A9	O	1	
									C	TK0	I/O	1	
									D	TIOB3	I/O	2	
									E	PCK1	O	4	
									F	GTX0	O	3	
A2	D2	D1	VDDIOP0	GPIO	PB21	I/O	–	–	A	LCDDAT10	O	1	PIO, I, PU, ST
									B	A10	O	1	
									C	TF0	I/O	1	
									D	TCLK3	I	2	
									E	FLEXCOM3_IO2	I/O	3	
									F	GTX1	O	3	
C3	G5	D2	VDDIOP0	GPIO	PB22	I/O	–	–	A	LCDDAT11	O	1	PIO, I, PU, ST
									B	A11	O	1	
									C	TD0	O	1	
									D	TIOA2	I/O	2	
									E	FLEXCOM3_IO1	I/O	3	
									F	GMDC	O	3	