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32-BIT ARM-BASED MICROPROCESSORS

SAMA5D4 Series
SAMA5D41 /42 /43 /44

Description

The SAMA5D4 Series is a high-performance, power-efficient Arm® Cortex®-A5 processor-based MPU capable of running at up to 600 MHz. It integrates the Arm NEON™ SIMD engine for accelerated signal processing, multimedia and graphics, as well as a 128 KB L2-Cache for high system performance. The device features the Arm TrustZone® enabling a strong security perimeter for critical software, as well as several hardware security features. The device also features advanced user interface and connectivity peripherals.

The SAMA5D4 devices have three software-selectable low-power modes: Idle, Ultra-low-power, and Backup. In Idle mode, the processor is stopped while all other functions can be kept running at normal operating bus frequency. In Ultra-low-power mode, the processor is stopped while all other functions can be kept running at minimum operating bus frequency. In Backup mode, only the real-time clock, real-time timer, backup SRAM, backup registers, and wakeup logic are running.

The SAMA5D4 features an internal multi-layer bus architecture associated with 32 DMA channels to sustain the high bandwidth required by the processor and the high-speed peripherals. The device supports DDR2/LPDDR/LPDDR2 and SLC/MLC NAND Flash memory with 24-bit ECC.

The comprehensive peripheral set includes a 720p hardware video decoder, an LCD controller with overlays for hardware-accelerated image composition, a resistive touchscreen function, and a CMOS sensor interface. Connectivity peripherals include a dual 10/100 Ethernet MAC with IEEE1588, three HS USB ports, UARTs, SPIs and I2Cs.

Security features include an “on-the-fly” encryption-decryption process from the external DDR memory, tamper detection pins, secure storage of critical data, an integrity check monitor (ICM) to detect modification of the memory contents and a secure boot. The product also includes a dedicated coprocessor for public key cryptography such as RSA and elliptic curves algorithms (ECC), as well as AES, 3DES, SHA function and TRNG. These features protect the system against counterfeiting, safeguard sensitive data, authenticate safe programs and secure external data transfers.

The SAMA5D4 series is optimized for control panel/HMI applications needing video playback and applications that require high levels of connectivity in the industrial and consumer market. Its security features make the SAMA5D4 well suited for secure gateways or for the IoT.

Features

- Arm Cortex-A5 Core
  - Armv7-A Thumb2® instruction set
  - Arm TrustZone
  - NEON Media Processing Engine
  - 945 MIPS @ 600 MHz in worst conditions
- Memory Architecture
  - Memory Management Unit
  - 32 Kbyte Data Cache, 32 Kbyte Instruction Cache
  - 128 Kbyte L2 Cache
  - One 128 Kbyte scrambled internal ROM single-cycle access at system speed, embedding Microchip boot loader/Microchip Secure boot loader
  - One 128 Kbyte scrambled internal SRAM, single-cycle access at system speed
  - High-bandwidth scramblable 16-bit or 32-bit Double Data Rate Multi-port Dynamic RAM Controller supporting 512 Mbyte 8-bank DDR2/LPDDR/LPDDR2, including partial areas “on-the-fly” AES encryption/decryption

  - EBI (External Bus interface) supporting:
    - 16-bit NAND Flash controller, including 24-bit error correction code (PMECC) for 8-bit NAND Flash
    - Independent Static Memory Controller (SMC) with datapath scrambling
- System running up to 200 MHz in worst conditions
  - Power-on Reset Cells, Reset Controller, Shutdown Controller, Periodic Interval Timer, Watchdog Timer and secure Real-time Clock
  - Internal regulator
  - One 600–1200 MHz PLL for the System and one PLL at 480 MHz optimized for USB High Speed
  - Internal Low-power 12 MHz RC Oscillator
  - Low-power 32 kHz RC Oscillator
  - Selectable 32.768 KHz Low-power oscillator and 12 MHz Oscillator
  - Two 64-bit, 16-channel DMA Controllers
  - 64-bit Advanced Interrupt Controller
  - 64-bit Secure Advanced Interrupt Controller
  - Three Programmable External Clock Signals
  - Programmable fuse box with 512 fuse bits available for customer, including JTAG protection
- Three Low-power Modes: Idle, Ultra-low-power, and Backup
- Peripherals
  - Video Decoder (VDEC) supporting formats MPEG-4, H.264, H.263, VP8 and JPEG, and image postprocessing
  - LCD TFT Controller with 4 overlays up to 2048x2048 or up to 720p in video format, with rotation and alpha blending
  - ITU-R BT. 601/656 Image Sensor Interface (ISI)
  - One High-Speed USB Device, Three High-Speed USB Host with On-chip Transceiver
  - Two 10/100 Mbps Ethernet MAC Controllers with IEEE 1588 v2 support
  - Software Modem Interface (SMD)
  - Two high-speed memory card hosts (eMMC 4.3 and SD 2.0)
  - Three Master/Slave Serial Peripheral Interfaces (SPI)
  - Five USARTs, two UARTs, one DBGU
  - Two Synchronous Serial Controllers (SSC)
  - Four Two-wire Interfaces up to 400 Kbits/s supporting I2C protocol and SMBUS (TWI)
  - Three 3-channel 32-bit Timer/Counters (TC)
  - One 4-channel 16-bit PWM Controller
  - One 5-channel 10-bit Analog-to-Digital Converter with Resistive Touchscreen function
- Safety
  - Internal and external memory integrity monitoring, with Integrity Check Monitor (ICM) based on SHA256
  - Power-on Reset Cells
  - Main Crystal Clock Failure Detector
  - Independent Watchdog
  - Register Write Protection
  - Memory Management Unit
- Security
  - 512 bits of scrambled and erasable registers(1)
  - 8 Kbytes of internal scrambled RAM with non-imprinting support, 6 Kbytes are erasable(1)
  - 8 PIOBU tamper pins for static or dynamic intrusion detections(1)
  - Microchip secure boot(2)

Note:

1: This feature is described in the document “Secure Box Module (SBM)”, Literature No. 11254. This document is available under Non-Disclosure Agreement (NDA). Contact a Microchip Sales Representative for further details.

2: For secure boot strategies, refer to the application note “SAMA5D4x Secure Boot Strategy”, Literature No. 11295. This document is available under Non-Disclosure Agreement (NDA). Contact a Microchip Sales Representative for further details.

- Cryptography
  - True Random Number Generator (TRNG), compliant with NIST special publication 800-22 test suite and FIPS PBUs 140-2 and 140-3
  - SHA: Supports Secure Hash Algorithm (SHA1, SHA224, SHA256, SHA384, SHA512) compliant with FIPS publications 180-2
  - AES: 256-bit, 192-bit, 128-bit Key Algorithm, compliant with FIPS PUB 197 specifications
  - Advanced Encryption Standard Bridge (AESB): AES 128 that includes Automatic Bridge Mode for automatic DDR port Encryption/Decryption
  - TDES: Two-key or Three-key Algorithms, compliant with FIPS PUB 46-3 specifications
  - Public Key Coprocessor (CPKCC) and associated Classical Public Key Cryptography Library (CPKCL) for RSA, DSA, ECC GF(2^n), ECC GF(p)[(1)]
- Up to 152 I/Os
  - Five Parallel Input/Output Controllers with slew rate control on high-speed I/Os
  - Input Change Interrupt capability on each I/O Line, selectable Schmitt Trigger input
  - Individually Programmable Open-drain, Pull-up and Pull-down Resistor, Synchronous Output, Filtering
- Packages
  - 361-ball stubless TFBGA, 16x16 mm body, pitch 0.8 mm
  - 289-ball stubless LFBGA, 14x14 mm body, pitch 0.8 mm

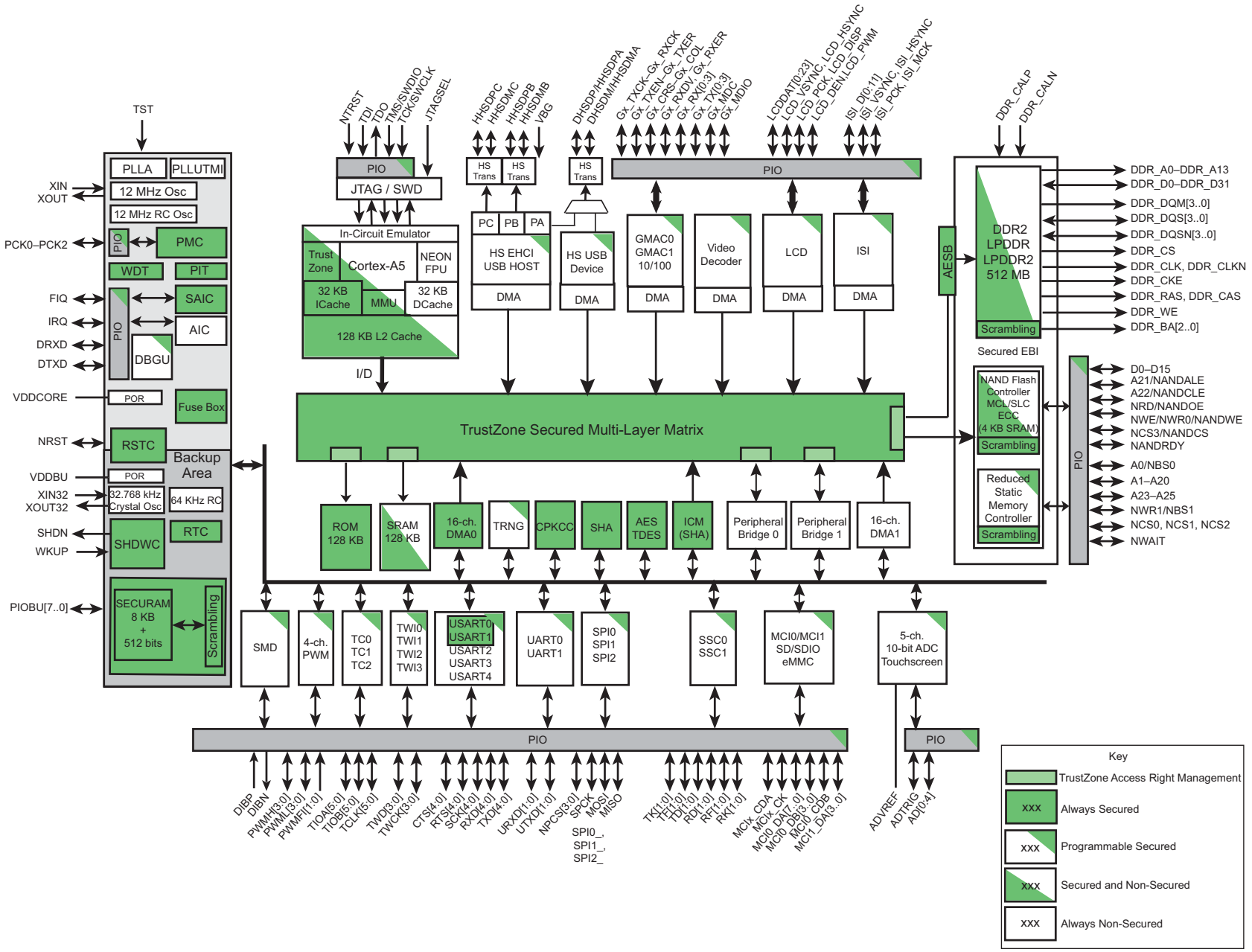
- SAMA5D4 Series Devices

Device	Package	Video Decoder	DDR Datapath
SAMA5D44	TFBGA361	X	32 bits
SAMA5D43	LFBGA289	X	16 bits
SAMA5D42	TFBGA361	–	32 bits
SAMA5D41	LFBGA289	–	16 bits

Note 1: CPKCC and CPKCL are described in the application note “Using CPKCL Version 02.05.01.xx on SAMA5D4”, Literature No. 11247. This document is available under Non-Disclosure Agreement (NDA). Contact a Microchip Sales Representative for further details.

1. Block Diagram

Figure 1-1: Block Diagram



2. Signal Description

Table 2-1 gives details on signal names classified by peripheral.

Table 2-1: Signal Description List

Signal Name	Function	Type	Active Level
Clocks, Oscillators and PLLs			
XIN	Main Oscillator Input	Input	–
XOUT	Main Oscillator Output	Output	–
XIN32	Slow Clock Oscillator Input	Input	–
XOUT32	Slow Clock Oscillator Output	Output	–
VBG	Bias Voltage Reference for USB	Analog	–
PCK0–PCK2	Programmable Clock Output	Output	–
Shutdown, Wakeup Logic			
SHDN	Shutdown Control	Output	–
WKUP	Wakeup Input	Input	–
ICE and JTAG			
TCK/SWCLK	Test Clock/Serial Wire Clock	Input	–
TDI	Test Data In	Input	–
TDO	Test Data Out	Output	–
TMS/SWDIO	Test Mode Select/Serial Wire Input/Output	I/O	–
JTAGSEL	JTAG Selection	Input	–
Reset/Test			
NRST	Microprocessor Reset	Input	Low
TST	Test Mode Select	Input	–
NTRST	Test Reset Signal	Input	–
Debug Unit - DBGU			
DRXD	Debug Receive Data	Input	–
DTXD	Debug Transmit Data	Output	–
Advanced Interrupt Controller - AIC			
IRQ	External Interrupt Input	Input	–
Secured Advanced Interrupt Controller - SAIC			
FIQ	Fast Interrupt Input	Input	–
PIO Controller - PIOA - PIOB - PIOC - PIOD - PIOE			
PA0–PAxx	Parallel IO Controller A	I/O	–
PB0–PBxx	Parallel IO Controller B	I/O	–
PC0–PCxx	Parallel IO Controller C	I/O	–
PD8–PDxx	Parallel IO Controller D	I/O	–
PE0–PExx	Parallel IO Controller E	I/O	–

Table 2-1: Signal Description List (Continued)

Signal Name	Function	Type	Active Level
External Bus Interface - EBI			
D0–D15	Data Bus	I/O	–
A0–A25	Address Bus	Output	–
NWAIT	External Wait Signal	Input	Low
Static Memory Controller - SMC			
NCS0–NCS3	Chip Select Lines	Output	Low
NWR0–NWR1	Write Signal	Output	Low
NRD	Read Signal	Output	Low
NWE	Write Enable	Output	Low
NBS0–NBS1	Byte Mask Signal	Output	Low
NANDOE	NAND Flash Output Enable	Output	Low
NANDWE	NAND Flash Write Enable	Output	Low
DDR2/LPDDR2 Controller			
DDR_CK,DDR_CKN	DDR2 Differential Clock	Output	–
DDR_CKE	DDR2 Clock Enable	Output	High
DDR_CS	DDR2 Controller Chip Select	Output	Low
DDR_BA[2..0]	Bank Select	Output	Low
DDR_WE	DDR2 Write Enable	Output	Low
DDR_RAS, DDR_CAS	Row and Column Signal	Output	Low
DDR_A[13..0]	DDR2 Address Bus	Output	–
DDR_D[31..0]	DDR2 Data Bus	I/O/-PD	–
DDR_DQS[3..0], DDR_DQSN[3..0]	Differential Data Strobe	I/O-PD	–
DDR_DQM[3..0]	Write Data Mask	Output	–
DDR_CALP, DDR_CALN	DDR2/LPDDR2 Calibration	Input	–
DDR_VREF	DDR2/LPDDR2 Reference	Input	–
High Speed Multimedia Card Interface - HSMCIx [1..0]			
MCI0_CK, MCI1_CK	Multimedia Card Clock	I/O	–
MCI0_CDA, MCI0_CDB, MCI1_CDA	Multimedia Card Command	I/O	–
MCI0_DA[7..0]	Multimedia Card 0 Data slot A	I/O	–
MCI0_DB[3..0]	Multimedia Card 0 Data slot B	I/O	–
MCI1_DA[3..0]	Multimedia Card 1 Data	I/O	–
Universal Synchronous Asynchronous Receiver Transmitter - USARTx [4..0]			
SCKx	USARTx Serial Clock	I/O	–
TXDx	USARTx Transmit Data	Output	–
RXDx	USARTx Receive Data	Input	–
RTSx	USARTx Request To Send	Output	–

Table 2-1: Signal Description List (Continued)

Signal Name	Function	Type	Active Level
CTSx	USARTx Clear To Send	Input	–
Universal Asynchronous Receiver Transmitter - UARTx [1..0]			
UTXDx	UARTx Transmit Data	Output	–
URXDx	UARTx Receive Data	Input	–
Synchronous Serial Controller - SSCx [1..0]			
TDx	SSC Transmit Data	Output	–
RDx	SSC Receive Data	Input	–
TKx	SSC Transmit Clock	I/O	–
RKx	SSC Receive Clock	I/O	–
TFx	SSC Transmit Frame Sync	I/O	–
RFx	SSC Receive Frame Sync	I/O	–
Timer/Counter - TCx [8..0]			
TCLKx	TC Channel x External Clock Input	Input	–
TIOAx	TC Channel x I/O Line A	I/O	–
TIOBx	TC Channel x I/O Line B	I/O	–
Serial Peripheral Interface - SPIx [2..0]			
SPIx_MISO	Master In Slave Out	I/O	–
SPIx_MOSI	Master Out Slave In	I/O	–
SPIx_SPCK	SPI Serial Clock	I/O	–
SPIx_NPCS0	SPI Peripheral Chip Select 0	I/O	Low
SPIx_NPCS[3..1]	SPI Peripheral Chip Select	Output	Low
Two-wire Interface - TWIx [3..0]			
TWDx	Two-wire Serial Data	I/O	–
TWCKx	Two-wire Serial Clock	I/O	–
Pulse Width Modulation Controller - PWM			
PWMH0–3	PWM Waveform Output High	–	Output
PWML0–3	PWM Waveform Output Low	–	Output
PWMFI0–1	PWM Fault Inputs	–	Input
USB Host High Speed Port - UHPHS			
HHSDPA	USB Host Port A High Speed Data +	Analog	–
HHSDMA	USB Host Port A High Speed Data -	Analog	–
HHSDPB	USB Host Port B High Speed Data +	Analog	–
HHSDMB	USB Host Port B High Speed Data -	Analog	–
HHSDPC	USB Host Port C High Speed Data +	Analog	–
HHSDMC	USB Host Port C High Speed Data -	Analog	–
USB Device High Speed Port - UDPHS			

Table 2-1: Signal Description List (Continued)

Signal Name	Function	Type	Active Level
DHSDP	USB Device High Speed Data +	Analog	–
DHSDM	USB Device High Speed Data -	Analog	–
Ethernet 10/100 - GMACx [1..0]			
GxTXCK	Transmit Clock or Reference Clock	Input	–
GxRXCK	Receive Clock	Input	–
GxTXEN	Transmit Enable	Output	–
GxTX0–3	Transmit Data	Output	–
GxTXER	Transmit Coding Error	Output	–
GxRXDV	Receive Data Valid	Input	–
GxRX0–3	Receive Data	Input	–
GxRXER	Receive Error	Input	–
GxCRS	Carrier Sense and Data Valid	Input	–
GxCOL	Collision Detect	Input	–
GxMDC	Management Data Clock	Output	–
GxMDIO	Management Data Input/Output	I/O	–
LCD Controller - LCDC			
LCDDAT0–23	LCD Data Bus	Output	–
LCDVSYNC	LCD Vertical Synchronization	Output	–
LCDHSYNC	LCD Horizontal Synchronization	Output	–
LCDPCK	LCD Pixel Clock	Output	–
LCDDEN	LCD Data Enable	Output	–
LCDPWM	LCDPWM for Contrast Control	Output	–
LCDDISP	LCD Display ON/OFF	Output	–
Touchscreen Analog-to-Digital Converter - ADC			
AD0–4	4 Analog Inputs	Analog	–
ADTRG	ADC Trigger	Input	–
ADVREF	ADC Reference	Analog	–
Secure Box Module - SBM			
PIOBU0–7	Secured I/Os	I/O	–
Image Sensor Interface - ISI			
ISI_D0–ISI_D11	Image Sensor Data	Input	–
ISI_HSYNC	Image Sensor Horizontal Synchro	Input	–
ISI_VSYNC	Image Sensor Vertical Synchro	Input	–
ISI_PCK	Image Sensor Data clock	Input	–
Software Modem Device - SMD			
DIBN	Software Modem Signal	I/O	–

Table 2-1: Signal Description List (Continued)

Signal Name	Function	Type	Active Level
DIBP	Software Modem Signal	I/O	–

3. Package and Pinout

The SAMA5D4 product is available in two packages:

- 361-ball TFBGA
- 289-ball LFBGA

The pinouts are provided in the following Section 3.1 “361-ball TFBGA Package Pinout” and Section 3.2 “289-ball LFBGA Package Pinout”.

The package mechanical characteristics are described in Section 57. “Mechanical Characteristics”.

3.1 361-ball TFBGA Package Pinout

Table 3-1: TFBGA361 Pin Description

			Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State[1]
Pin	Power Rail	I/O Type	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
A7	VDDIOP	GPIO	PA0	I/O	–	–	LCDDAT0	O	–	–	TMS	I	TMS, PU, ST
F6	VDDIOP	GPIO	PA1	I/O	–	–	LCDDAT1	O	–	–	–	–	PIO, I, PU, ST
E6	VDDIOP	GPIO_CLK	PA2	I/O	–	–	LCDDAT2	O	G1_TXCK	I	–	–	PIO, I, PU, ST
C6	VDDIOP	GPIO_CLK	PA3	I/O	–	–	LCDDAT3	O	G1_RXCK	I	–	–	PIO, I, PU, ST
D6	VDDIOP	GPIO	PA4	I/O	–	–	LCDDAT4	O	G1_TXEN	O	–	–	PIO, I, PU, ST
B6	VDDIOP	GPIO	PA5	I/O	–	–	LCDDAT5	O	G1_TXER	O	–	–	PIO, I, PU, ST
A6	VDDIOP	GPIO	PA6	I/O	–	–	LCDDAT6	O	G1_CRS	I	–	–	PIO, I, PU, ST
E5	VDDIOP	GPIO	PA7	I/O	–	–	LCDDAT7	O	–	–	–	–	PIO, I, PU, ST
A5	VDDIOP	GPIO	PA8	I/O	–	–	LCDDAT8	O	–	–	TCK	I	TCK, PU
F4	VDDIOP	GPIO	PA9	I/O	–	–	LCDDAT9	O	G1_COL	I	–	–	PIO, I, PU, ST
F5	VDDIOP	GPIO	PA10	I/O	–	–	LCDDAT10	O	G1_RXDV	I	–	–	PIO, I, PU, ST
D5	VDDIOP	GPIO	PA11	I/O	–	–	LCDDAT11	O	G1_RXER	I	–	–	PIO, I, PU, ST
G5	VDDIOP	GPIO	PA12	I/O	–	–	LCDDAT12	O	G1_RX0	I	–	–	PIO, I, PU, ST
C5	VDDIOP	GPIO	PA13	I/O	–	–	LCDDAT13	O	G1_RX1	I	–	–	PIO, I, PU, ST
E4	VDDIOP	GPIO	PA14	I/O	–	–	LCDDAT14	O	G1_TX0	O	–	–	PIO, I, PU, ST
B5	VDDIOP	GPIO	PA15	I/O	–	–	LCDDAT15	O	G1_TX1	O	–	–	PIO, I, PU, ST
H6	VDDIOP	GPIO	PA16	I/O	–	–	LCDDAT16	O	–	–	NTRST	I	NTRST, PU, ST
D4	VDDIOP	GPIO	PA17	I/O	–	–	LCDDAT17	O	–	–	–	–	PIO, O, LOW
G4	VDDIOP	GPIO	PA18	I/O	–	–	LCDDAT18	O	G1_RX2	I	–	–	PIO, O, LOW
C4	VDDIOP	GPIO	PA19	I/O	–	–	LCDDAT19	O	G1_RX3	I	–	–	PIO, O, LOW
A3	VDDIOP	GPIO	PA20	I/O	–	–	LCDDAT20	O	G1_TX2	O	–	–	PIO, I, PU, ST
B4	VDDIOP	GPIO	PA21	I/O	–	–	LCDDAT21	O	G1_TX3	O	–	–	PIO, I, PU, ST
B3	VDDIOP	GPIO	PA22	I/O	–	–	LCDDAT22	O	G1_MDC	O	–	–	PIO, I, PU, ST
A4	VDDIOP	GPIO	PA23	I/O	–	–	LCDDAT23	O	G1_MDIO	I/O	–	–	PIO, I, PU, ST
H5	VDDIOP	GPIO_CLK	PA24	I/O	–	–	LCDPWM	O	PCK0	O	–	–	PIO, I, PU, ST
F3	VDDIOP	GPIO	PA25	I/O	–	–	LCDDISP	O	TD0	O	–	–	PIO, I, PU, ST
E3	VDDIOP	GPIO	PA26	I/O	–	–	LCDVSYNC	O	PWMH0	O	SPI1_NPCS1	O	PIO, I, PU, ST
H4	VDDIOP	GPIO	PA27	I/O	–	–	LCDHSYNC	O	PWML0	O	SPI1_NPCS2	O	PIO, I, PU, ST
G3	VDDIOP	GPIO_CLK2	PA28	I/O	–	–	LCDPCK	O	PWMH1	O	SPI1_NPCS3	O	PIO, I, PU, ST
J5	VDDIOP	GPIO	PA29	I/O	–	–	LCDDEN	O	PWML1	O	–	–	PIO, I, PU, ST
D3	VDDIOP	GPIO	PA30	I/O	–	–	TWD0	I/O	–	–	–	–	PIO, I, PU, ST
J4	VDDIOP	GPIO	PA31	I/O	–	–	TWCK0	O	–	–	–	–	PIO, I, PU, ST
C3	VDDIOP	GPIO_CLK	PB0	I/O	–	–	G0_TXCK	I	–	–	–	–	PIO, I, PU, ST
A2	VDDIOP	GPIO_CLK	PB1	I/O	–	–	G0_RXCK	I	SCK2	I/O	ISI_PCK	I	PIO, I, PU, ST
B2	VDDIOP	GPIO	PB2	I/O	–	–	G0_TXEN	O	–	–	–	–	PIO, I, PU, ST
C2	VDDIOP	GPIO	PB3	I/O	–	–	G0_TXER	O	CTS2	I	ISI_VSYNC	I	PIO, I, PU, ST

Table 3-1: TFBGA361 Pin Description (Continued)

Pin	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State[1]
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
J3	VDDIOP	GPIO	PB4	I/O	–	–	G0_CRS	I	RXD2	I	ISI_HSYNC	I	PIO, I, PU, ST
H2	VDDIOP	GPIO	PB5	I/O	–	–	G0_COL	I	TXD2	O	PCK2	O	PIO, I, PU, ST
G2	VDDIOP	GPIO	PB6	I/O	–	–	G0_RXDV	I	–	–	–	–	PIO, I, PU, ST
H3	VDDIOP	GPIO	PB7	I/O	–	–	G0_RXER	I	–	–	–	–	PIO, I, PU, ST
F2	VDDIOP	GPIO	PB8	I/O	–	–	G0_RX0	I	–	–	–	–	PIO, I, PU, ST
J2	VDDIOP	GPIO	PB9	I/O	–	–	G0_RX1	I	–	–	–	–	PIO, I, PU, ST
F1	VDDIOP	GPIO_CLK	PB10	I/O	–	–	G0_RX2	I	PCK2	O	PWML1	O	PIO, I, PU, ST
K4	VDDIOP	GPIO	PB11	I/O	–	–	G0_RX3	I	RTS2	O	PWMH1	O	PIO, I, PU, ST
D2	VDDIOP	GPIO	PB12	I/O	–	–	G0_TX0	O	–	–	–	–	PIO, I, PU, ST
K3	VDDIOP	GPIO	PB13	I/O	–	–	G0_TX1	O	–	–	–	–	PIO, I, PU, ST
A1	VDDIOP	GPIO	PB14	I/O	–	–	G0_TX2	O	SPI2_NPCS1	O	PWMH0	O	PIO, I, PU, ST
E2	VDDIOP	GPIO	PB15	I/O	–	–	G0_TX3	O	SPI2_NPCS2	O	PWML0	O	PIO, I, PU, ST
B1	VDDIOP	GPIO	PB16	I/O	–	–	G0_MDC	O	–	–	–	–	PIO, I, PU, ST
K5	VDDIOP	GPIO	PB17	I/O	–	–	G0_MDIO	I/O	–	–	–	–	PIO, I, PU, ST
K2	VDDIOP	GPIO	PB18	I/O	–	–	SPI1_MISO	I/O	D8	I/O	–	–	PIO, I, PU, ST
C1	VDDIOP	GPIO	PB19	I/O	–	–	SPI1_MOSI	I/O	D9	I/O	–	–	PIO, I, PU, ST
D1	VDDIOP	GPIO_CLK	PB20	I/O	–	–	SPI1_SPCK	I/O	D10	I/O	–	–	PIO, I, PU, ST
L3	VDDIOP	GPIO	PB21	I/O	–	–	SPI1_NPCS0	I/O	D11	I/O	–	–	PIO, I, PU, ST
G1	VDDIOP	GPIO	PB22	I/O	–	–	SPI1_NPCS1	O	D12	I/O	–	–	PIO, I, PU, ST
H1	VDDIOP	GPIO	PB23	I/O	–	–	SPI1_NPCS2	O	D13	I/O	–	–	PIO, I, PU, ST
E1	VDDIOP	GPIO	PB24	I/O	–	–	DRXD	I	D14	I/O	TDI	I	TDI, PU, ST
J1	VDDIOP	GPIO	PB25	I/O	–	–	DTXD	O	D15	I/O	TDO	O	TDO, ST
M5	VDDIOP	GPIO_CLK	PB26	I/O	–	–	PCK0	O	RK0	I/O	PWMH0	O	PIO, I, PU, ST
L2	VDDIOP	GPIO	PB27	I/O	–	–	SPI1_NPCS3	O	TK0	I/O	PWML0	O	PIO, I, PU, ST
K1	VDDIOP	GPIO	PB28	I/O	–	–	SPI2_NPCS3	O	TD0	O	PWMH1	O	PIO, I, PU, ST
M3	VDDIOP	GPIO	PB29	I/O	–	–	TWD2	I/O	RD0	I	PWML1	O	PIO, O, LOW
M4	VDDIOP	GPIO	PB30	I/O	–	–	TWCK2	O	RF0	I/O	–	–	PIO, O, LOW
L1	VDDIOP	GPIO	PB31	I/O	–	–	–	–	TF0	I/O	–	–	PIO, I, PU, ST
V4	VDDIOM	GPIO	PC0	I/O	–	–	SPI0_MISO	I/O	PWMH2	O	ISI_D8	I	PIO, I, PU, ST
P8	VDDIOM	GPIO	PC1	I/O	–	–	SPI0_MOSI	I/O	PWML2	O	ISI_D9	I	PIO, I, PU, ST
V5	VDDIOM	GPIO_CLK	PC2	I/O	–	–	SPI0_SPCK	I/O	PWMH3	O	ISI_D10	I	PIO, I, PU, ST
R8	VDDIOM	GPIO	PC3	I/O	–	–	SPI0_NPCS0	I/O	PWML3	O	ISI_D11	I	PIO, I, PU, ST
W5	VDDIOM	MCI_CLK	PC4	I/O	–	–	SPI0_NPCS1	O	MCI0_CK	I/O	PCK1	O	PIO, I, PU, ST
T8	VDDIOM	GPIO	PC5	I/O	–	–	D0	I/O	MCI0_CDA	I/O	–	–	PIO, I, PU, ST
W6	VDDIOM	GPIO	PC6	I/O	–	–	D1	I/O	MCI0_DA0	I/O	–	–	PIO, I, PU, ST
R19	VDDIOM	GPIO	PC7	I/O	–	–	D2	I/O	MCI0_DA1	I/O	–	–	PIO, I, PU, ST
N15	VDDIOM	GPIO	PC8	I/O	–	–	D3	I/O	MCI0_DA2	I/O	–	–	PIO, I, PU, ST

Table 3-1: TFBGA361 Pin Description (Continued)

Pin	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State(1)
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
U8	VDDIOM	GPIO	PC9	I/O	–	–	D4	I/O	MCI0_DA3	I/O	–	–	PIO, I, PU, ST
V6	VDDIOM	GPIO	PC10	I/O	–	–	D5	I/O	MCI0_DA4	I/O	–	–	PIO, I, PU, ST
V7	VDDIOM	GPIO	PC11	I/O	–	–	D6	I/O	MCI0_DA5	I/O	–	–	PIO, I, PU, ST
W7	VDDIOM	GPIO	PC12	I/O	–	–	D7	I/O	MCI0_DA6	I/O	–	–	PIO, I, PU, ST
V8	VDDIOM	GPIO	PC13	I/O	–	–	NRD/NANDOE	O	MCI0_DA7	I/O	–	–	PIO, I, PU, ST
U9	VDDIOM	GPIO	PC14	I/O	–	–	NWE/NANDWE	O	–	–	–	–	PIO, I, PU, ST
W8	VDDIOM	GPIO	PC15	I/O	–	–	NCS3	O	–	–	–	–	PIO, I, PU, ST
V9	VDDIOM	GPIO	PC16	I/O	–	–	NANDRDY	I	–	–	–	–	PIO, I, PU, ST
W9	VDDIOM	GPIO	PC17	I/O	–	–	A21/NANDALE	O	–	–	–	–	A21
V10	VDDIOM	GPIO	PC18	I/O	–	–	A22/NANDCLE	O	–	–	–	–	A22
U14	VDDIOM	GPIO	PC19	I/O	–	–	ISI_D0	I	TK1	I/O	–	–	PIO, I, PU, ST
V11	VDDIOM	GPIO	PC20	I/O	–	–	ISI_D1	I	TF1	I/O	–	–	PIO, I, PU, ST
U15	VDDIOM	GPIO	PC21	I/O	–	–	ISI_D2	I	TD1	O	–	–	PIO, I, PU, ST
T15	VDDIOM	GPIO	PC22	I/O	–	–	ISI_D3	I	RF1	I/O	–	–	PIO, I, PU, ST
U16	VDDIOM	GPIO	PC23	I/O	–	–	ISI_D4	I	RD1	I	–	–	PIO, I, PU, ST
T16	VDDIOM	GPIO	PC24	I/O	–	–	ISI_D5	I	RK1	I	PCK1	O	PIO, I, PU, ST
V17	VDDIOM	GPIO	PC25	I/O	–	–	ISI_D6	I	TWD3	I/O	URXD1	I	PIO, I, PU, ST
R16	VDDIOM	GPIO	PC26	I/O	–	–	ISI_D7	I	TWCK3	O	UTXD1	O	PIO, I, PU, ST
U12	VDDANA	GPIO_ANA	PC27	I/O	AD0	–	–	I	SPI0_NPCS1	O	PWML0	O	PIO, I, PU, ST
T11	VDDANA	GPIO_ANA	PC28	I/O	AD1	–	–	I	SPI0_NPCS2	O	PWML1	O	PIO, I, PU, ST
R13	VDDANA	GPIO_ANA	PC29	I/O	AD2	–	–	I	SPI0_NPCS3	O	PWMFI0	O	PIO, I, PU, ST
T12	VDDANA	GPIO_ANA	PC30	I/O	AD3	–	–	I	–	–	PWMH0	O	PIO, I, PU, ST
T13	VDDANA	GPIO_ANA	PC31	I/O	AD4	–	–	I	–	–	PWMH1	I	PIO, I, PU, ST
M1	VDDIOP	GPIO_CLK	PD8	I/O	–	–	PCK0	O	–	–	–	–	PIO, I, PU, ST
M2	VDDIOP	GPIO	PD9	I/O	–	–	FIQ	I	–	–	–	–	PIO, I, PU, ST
N2	VDDIOP	GPIO	PD10	I/O	–	–	CTS0	I	–	–	–	–	PIO, I, PU, ST
N3	VDDIOP	GPIO	PD11	I/O	–	–	RTS0	O	SPI2_MISO	I/O	–	–	PIO, I, PU, ST
N1	VDDIOP	GPIO	PD12	I/O	–	–	RXD0	I	–	–	–	–	PIO, O, PD
P3	VDDIOP	GPIO	PD13	I/O	–	–	TXD0	O	SPI2_MOSI	I/O	–	–	PIO, I, PU, ST
P2	VDDIOP	GPIO	PD14	I/O	–	–	CTS1	I	–	–	–	–	PIO, I, PU, ST
N4	VDDIOP	GPIO	PD15	I/O	–	–	RTS1	O	SPI2_SPCK	I/O	–	–	PIO, I, PU, ST
R2	VDDIOP	GPIO	PD16	I/O	–	–	RXD1	I	–	–	–	–	PIO, O, PD
R3	VDDIOP	GPIO	PD17	I/O	–	–	TXD1	O	SPI2_NPCS0	I/O	–	–	PIO, I, PU, ST
T9	VDDANA	GPIO	PD18	I/O	–	–	–	–	–	–	–	–	PIO, I, PU, ST
P11	VDDANA	GPIO	PD19	I/O	–	–	–	–	–	–	–	–	PIO, I, PU, ST
T10	VDDANA	GPIO	PD20	I/O	–	–	–	–	–	–	–	–	PIO, I, PU, ST
P10	VDDANA	GPIO	PD21	I/O	–	–	–	–	–	–	–	–	PIO, I, PU, ST

Table 3-1: TFBGA361 Pin Description (Continued)

Pin	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State[1]
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
U11	VDDANA	GPIO	PD22	I/O	–	–	–	–	–	–	–	–	PIO, I, PU, ST
R10	VDDANA	GPIO	PD23	I/O	–	–	–	–	–	–	–	–	PIO, I, PU, ST
U10	VDDANA	GPIO	PD24	I/O	–	–	–	–	–	–	–	–	PIO, I, PU, ST
R11	VDDANA	GPIO	PD25	I/O	–	–	–	–	–	–	–	–	PIO, I, PU, ST
U13	VDDANA	GPIO	PD26	I/O	–	–	–	–	–	–	–	–	PIO, I, PU, ST
T14	VDDANA	GPIO	PD27	I/O	–	–	–	–	–	–	–	–	PIO, I, PU, ST
R1	VDDIOP	GPIO_CLK	PD28	I/O	–	–	SCK0	I/O	–	–	–	–	PIO, I, PU, ST
P1	VDDIOP	GPIO_CLK	PD29	I/O	–	–	SCK1	I/O	–	–	–	–	PIO, I, PU, ST
N5	VDDIOP	GPIO	PD30	I/O	–	–	–	–	–	–	–	–	PIO, I, PU, ST
P5	VDDIOP	GPIO_CLK	PD31	I/O	–	–	SPI0_NPCS2	O	PCK1	O	–	–	PIO, I, PU, ST
W19	VDDIOM	MCI_CLK	PE0	I/O	–	–	A0/NBS0	O	MCI0_CDB	I/O	CTS4	I	O, High
U17	VDDIOM	EBI	PE1	I/O	–	–	A1	O	MCI0_DB0	I/O	–	–	O, High
T17	VDDIOM	EBI	PE2	I/O	–	–	A2	O	MCI0_DB1	I/O	–	–	A2, LOW
P16	VDDIOM	EBI	PE3	I/O	–	–	A3	O	MCI0_DB2	I/O	–	–	A3, LOW
U18	VDDIOM	EBI	PE4	I/O	–	–	A4	O	MCI0_DB3	I/O	–	–	A4, LOW
R17	VDDIOM	EBI	PE5	I/O	–	–	A5	O	CTS3	I	–	–	A5, LOW
V19	VDDIOM	EBI	PE6	I/O	–	–	A6	O	TIOA3	I/O	–	–	PIO, O, LOW
U19	VDDIOM	EBI	PE7	I/O	–	–	A7	O	TIOB3	I/O	PWMFI1	I	A7, LOW
T19	VDDIOM	EBI	PE8	I/O	–	–	A8	O	TCLK3	I	PWML3	O	A8, LOW
T18	VDDIOM	EBI	PE9	I/O	–	–	A9	O	TIOA2	I/O	–	–	A9, LOW
N14	VDDIOM	EBI	PE10	I/O	–	–	A10	O	TIOB2	I/O	–	–	A10, LOW
R18	VDDIOM	EBI	PE11	I/O	–	–	A11	O	TCLK2	I	–	–	A11, LOW
P17	VDDIOM	EBI	PE12	I/O	–	–	A12	O	TIOA1	I/O	PWMH2	O	A12, LOW
P18	VDDIOM	EBI	PE13	I/O	–	–	A13	O	TIOB1	I/O	PWML2	O	A13, LOW
N17	VDDIOM	EBI	PE14	I/O	–	–	A14	O	TCLK1	I	PWMH3	O	A14, LOW
N18	VDDIOM	EBI	PE15	I/O	–	–	A15	O	SCK3	I/O	TIOA0	I/O	A15, LOW
M15	VDDIOM	EBI	PE16	I/O	–	–	A16	O	RXD3	I	TIOB0	I/O	A16, LOW
N19	VDDIOM	EBI	PE17	I/O	–	–	A17	O	TXD3	O	TCLK0	I	A17, LOW
P19	VDDIOM	EBI	PE18	I/O	–	–	A18	O	TIOA5	I/O	MCI1_CK	I/O	A18, LOW
N16	VDDIOM	EBI	PE19	I/O	–	–	A19	O	TIOB5	I/O	MCI1_CDA	I/O	A19, LOW
M14	VDDIOM	EBI	PE20	I/O	–	–	A20	O	TCLK5	I	MCI1_DA0	I/O	A20, LOW
M18	VDDIOM	EBI	PE21	I/O	–	–	A23	O	TIOA4	I/O	MCI1_DA1	I/O	A23, LOW
M19	VDDIOM	EBI	PE22	I/O	–	–	A24	O	TIOB4	I/O	MCI1_DA2	I/O	A24, LOW
L18	VDDIOM	EBI	PE23	I/O	–	–	A25	O	TCLK4	I	MCI1_DA3	I/O	A25, LOW
L19	VDDIOM	EBI	PE24	I/O	–	–	NCS0	O	RTS3	O	–	–	NCS0, HIGH
M17	VDDIOM	EBI	PE25	I/O	–	–	NCS1	O	SCK4	I/O	IRQ	I	NCS1, HIGH
L15	VDDIOM	EBI	PE26	I/O	–	–	NCS2	O	RXD4	I	A18	O	NCS2, HIGH

Table 3-1: TFBGA361 Pin Description (Continued)

Pin	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State[1]
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
M16	VDDIOM	EBI	PE27	I/O	–	–	NWR1/NBS1	O	TXD4	O	–	–	PIO, I, PD
L17	VDDIOM	EBI	PE28	I/O	–	–	NWAIT	I	RTS4	O	A19	O	PIO, I, PD
V1	VDDIOP	DIB	PE29	I/O	–	–	DIBP	O	URXD0	I	TWD1	I/O	PIO, O, LOW
U2	VDDIOP	DIB	PE30	I/O	–	–	DIBN	O	UTXD0	O	TWCK1	O	PIO, O, LOW
L4	VDDIOP	GPIO	PE31	I/O	–	–	ADTRG	I	–	–	–	–	PIO, O, LOW
H10 G10 K10 J10 K9 J9 H9 G9 E7 A8 D7 B7 C7 E9 A10 B9 D8 A9	–	Not connected	–	–	–	–	–	–	–	–	–	–	–
P4	VDDBU	SYSC	TST	I	–	–	–	–	–	–	–	–	I, PD, ST
W12	VDDIOP	CLOCK	XIN	I	–	–	–	–	–	–	–	–	I
V12	VDDIOP	CLOCK	XOUT	O	–	–	–	–	–	–	–	–	O
W2	VDDBU	CLOCK	XIN32	I	–	–	–	–	–	–	–	–	I
W3	VDDBU	CLOCK	XOUT32	O	–	–	–	–	–	–	–	–	O
T2	VDDBU	SYSC	SHDN	O	–	–	–	–	–	–	–	–	O, PU
V3	VDDBU	SYSC	WKUP	I	–	–	–	–	–	–	–	–	I, ST
U3	VDDBU	PIOBU	PIOBU0	I	–	–	–	–	–	–	–	–	I, PU
T3	VDDBU	PIOBU	PIOBU1	I	–	–	–	–	–	–	–	–	I, PU
T4	VDDBU	PIOBU	PIOBU2	I	–	–	–	–	–	–	–	–	I, PU
U4	VDDBU	PIOBU	PIOBU3	I	–	–	–	–	–	–	–	–	I, PU
P6	VDDBU	PIOBU	PIOBU4	I	–	–	–	–	–	–	–	–	I, PU
T5	VDDBU	PIOBU	PIOBU5	I	–	–	–	–	–	–	–	–	I, PU
R4	VDDBU	PIOBU	PIOBU6	I	–	–	–	–	–	–	–	–	I, PU
U5	VDDBU	PIOBU	PIOBU7	I	–	–	–	–	–	–	–	–	I, PU
R5 U6 R6 T6 R7 U7 P7 T7	–	Not connected	–	–	–	–	–	–	–	–	–	–	–

Table 3-1: TFBGA361 Pin Description (Continued)

Pin	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State[1]
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
T1	VDDBU	RST	NRST	I	–	–	–	–	–	–	–	–	I
V2	VDDBU	SYSC	JTAGSEL	I	–	–	–	–	–	–	–	–	I, PD
F15	VDDIODDR	DDR_IO	DDR_A0	O	–	–	–	–	–	–	–	–	O, LOW
F16	VDDIODDR	DDR_IO	DDR_A1	O	–	–	–	–	–	–	–	–	O, LOW
E17	VDDIODDR	DDR_IO	DDR_A2	O	–	–	–	–	–	–	–	–	O, LOW
G15	VDDIODDR	DDR_IO	DDR_A3	O	–	–	–	–	–	–	–	–	O, LOW
B18	VDDIODDR	DDR_IO	DDR_A4	O	–	–	–	–	–	–	–	–	O, LOW
C16	VDDIODDR	DDR_IO	DDR_A5	O	–	–	–	–	–	–	–	–	O, LOW
E15	VDDIODDR	DDR_IO	DDR_A6	O	–	–	–	–	–	–	–	–	O, LOW
F17	VDDIODDR	DDR_IO	DDR_A7	O	–	–	–	–	–	–	–	–	O, LOW
F18	VDDIODDR	DDR_IO	DDR_A8	O	–	–	–	–	–	–	–	–	O, LOW
D19	VDDIODDR	DDR_IO	DDR_A9	O	–	–	–	–	–	–	–	–	O, LOW
E18	VDDIODDR	DDR_IO	DDR_A10	O	–	–	–	–	–	–	–	–	O, LOW
D18	VDDIODDR	DDR_IO	DDR_A11	O	–	–	–	–	–	–	–	–	O, LOW
C18	VDDIODDR	DDR_IO	DDR_A12	O	–	–	–	–	–	–	–	–	O, LOW
D16	VDDIODDR	DDR_IO	DDR_A13	O	–	–	–	–	–	–	–	–	O, LOW
L14	VDDIODDR	DDR_IO	DDR_D0	I/O	–	–	–	–	–	–	–	–	I, HiZ
K16	VDDIODDR	DDR_IO	DDR_D1	I/O	–	–	–	–	–	–	–	–	I, HiZ
K15	VDDIODDR	DDR_IO	DDR_D2	I/O	–	–	–	–	–	–	–	–	I, HiZ
K14	VDDIODDR	DDR_IO	DDR_D3	I/O	–	–	–	–	–	–	–	–	I, HiZ
J18	VDDIODDR	DDR_IO	DDR_D4	I/O	–	–	–	–	–	–	–	–	I, HiZ
J17	VDDIODDR	DDR_IO	DDR_D5	I/O	–	–	–	–	–	–	–	–	I, HiZ
J15	VDDIODDR	DDR_IO	DDR_D6	I/O	–	–	–	–	–	–	–	–	I, HiZ
H19	VDDIODDR	DDR_IO	DDR_D7	I/O	–	–	–	–	–	–	–	–	I, HiZ
H18	VDDIODDR	DDR_IO	DDR_D8	I/O	–	–	–	–	–	–	–	–	I, HiZ
J14	VDDIODDR	DDR_IO	DDR_D9	I/O	–	–	–	–	–	–	–	–	I, HiZ
G18	VDDIODDR	DDR_IO	DDR_D10	I/O	–	–	–	–	–	–	–	–	I, HiZ
H17	VDDIODDR	DDR_IO	DDR_D11	I/O	–	–	–	–	–	–	–	–	I, HiZ
H15	VDDIODDR	DDR_IO	DDR_D12	I/O	–	–	–	–	–	–	–	–	I, HiZ
H14	VDDIODDR	DDR_IO	DDR_D13	I/O	–	–	–	–	–	–	–	–	I, HiZ
G16	VDDIODDR	DDR_IO	DDR_D14	I/O	–	–	–	–	–	–	–	–	I, HiZ
E19	VDDIODDR	DDR_IO	DDR_D15	I/O	–	–	–	–	–	–	–	–	I, HiZ
E14	VDDIODDR	DDR_IO	DDR_D16	I/O	–	–	–	–	–	–	–	–	I, HiZ
E13	VDDIODDR	DDR_IO	DDR_D17	I/O	–	–	–	–	–	–	–	–	I, HiZ
H13	VDDIODDR	DDR_IO	DDR_D18	I/O	–	–	–	–	–	–	–	–	I, HiZ
F13	VDDIODDR	DDR_IO	DDR_D19	I/O	–	–	–	–	–	–	–	–	I, HiZ
B15	VDDIODDR	DDR_IO	DDR_D20	I/O	–	–	–	–	–	–	–	–	I, HiZ

Table 3-1: TFBGA361 Pin Description (Continued)

Pin	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State[1]
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
A14	VDDIODDR	DDR_IO	DDR_D21	I/O	–	–	–	–	–	–	–	–	I, HiZ
D12	VDDIODDR	DDR_IO	DDR_D22	I/O	–	–	–	–	–	–	–	–	I, HiZ
B14	VDDIODDR	DDR_IO	DDR_D23	I/O	–	–	–	–	–	–	–	–	I, HiZ
B13	VDDIODDR	DDR_IO	DDR_D24	I/O	–	–	–	–	–	–	–	–	I, HiZ
G12	VDDIODDR	DDR_IO	DDR_D25	I/O	–	–	–	–	–	–	–	–	I, HiZ
B12	VDDIODDR	DDR_IO	DDR_D26	I/O	–	–	–	–	–	–	–	–	I, HiZ
C12	VDDIODDR	DDR_IO	DDR_D27	I/O	–	–	–	–	–	–	–	–	I, HiZ
F11	VDDIODDR	DDR_IO	DDR_D28	I/O	–	–	–	–	–	–	–	–	I, HiZ
C11	VDDIODDR	DDR_IO	DDR_D29	I/O	–	–	–	–	–	–	–	–	I, HiZ
D11	VDDIODDR	DDR_IO	DDR_D30	I/O	–	–	–	–	–	–	–	–	I, HiZ
B11	VDDIODDR	DDR_IO	DDR_D31	I/O	–	–	–	–	–	–	–	–	I, HiZ
L16	VDDIODDR	DDR_IO	DDR_DQM0	O	–	–	–	–	–	–	–	–	O, LOW
J16	VDDIODDR	DDR_IO	DDR_DQM1	O	–	–	–	–	–	–	–	–	O, LOW
D13	VDDIODDR	DDR_IO	DDR_DQM2	O	–	–	–	–	–	–	–	–	O, LOW
F12	VDDIODDR	DDR_IO	DDR_DQM3	O	–	–	–	–	–	–	–	–	O, LOW
J19	VDDIODDR	DDR_IO	DDR_DQS0	I/O	–	–	–	–	–	–	–	–	O, LOW
F19	VDDIODDR	DDR_IO	DDR_DQS1	I/O	–	–	–	–	–	–	–	–	O, LOW
A15	VDDIODDR	DDR_IO	DDR_DQS2	I/O	–	–	–	–	–	–	–	–	O, LOW
A12	VDDIODDR	DDR_IO	DDR_DQS3	I/O	–	–	–	–	–	–	–	–	O, LOW
K19	VDDIODDR	DDR_IO	DDR_DQSN0	I/O	–	–	–	–	–	–	–	–	O, HIGH
G19	VDDIODDR	DDR_IO	DDR_DQSN1	I/O	–	–	–	–	–	–	–	–	O, HIGH
A16	VDDIODDR	DDR_IO	DDR_DQSN2	I/O	–	–	–	–	–	–	–	–	O, HIGH
A13	VDDIODDR	DDR_IO	DDR_DQSN3	I/O	–	–	–	–	–	–	–	–	O, HIGH
B16	VDDIODDR	DDR_IO	DDR_CS	O	–	–	–	–	–	–	–	–	O, LOW
A18	VDDIODDR	DDR_IO	DDR_CLK	O	–	–	–	–	–	–	–	–	O
A19	VDDIODDR	DDR_IO	DDR_CLKN	O	–	–	–	–	–	–	–	–	O
D15	VDDIODDR	DDR_IO	DDR_CKE	O	–	–	–	–	–	–	–	–	O, LOW
B17	VDDIODDR	DDR_IO	DDR_RAS	O	–	–	–	–	–	–	–	–	O, LOW
A17	VDDIODDR	DDR_IO	DDR_CAS	O	–	–	–	–	–	–	–	–	O, LOW
E16	VDDIODDR	DDR_IO	DDR_WE	O	–	–	–	–	–	–	–	–	O, LOW
C15	VDDIODDR	DDR_IO	DDR_BA0	O	–	–	–	–	–	–	–	–	O, LOW
D14	VDDIODDR	DDR_IO	DDR_BA1	O	–	–	–	–	–	–	–	–	O, LOW
G13	VDDIODDR	DDR_IO	DDR_BA2	O	–	–	–	–	–	–	–	–	O, LOW
C19	VDDIODDR	Reference	DDR_CALN	I	–	–	–	–	–	–	–	–	I
B19	GNDIODDR	Reference	DDR_CALP	I	–	–	–	–	–	–	–	–	I
K12	VDDIODDR/2	Reference	DDR_VREF	I	–	–	–	–	–	–	–	–	I
W11	VBG	VBG	VBG	I	–	–	–	–	–	–	–	–	I

Table 3-1: TFBGA361 Pin Description (Continued)

Pin	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State[1]
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
R12	VDDANA	Reference	ADCVREF	I	–	–	–	–	–	–	–	–	I
W16	VDDUTMII	USBHS	HHSDPC	I/O	–	–	–	–	–	–	–	–	O, PD
V16	VDDUTMII	USBHS	HHSDMC	I/O	–	–	–	–	–	–	–	–	O, PD
W15	VDDUTMII	USBHS	HHSDPB	I/O	–	–	–	–	–	–	–	–	O, PD
V15	VDDUTMII	USBHS	HHSDMB	I/O	–	–	–	–	–	–	–	–	O, PD
W14	VDDUTMII	USBHS	HHSDPA	I/O	DHSDP	I/O	–	–	–	–	–	–	O, PD
V14	VDDUTMII	USBHS	HHSDMA	I/O	DHSDM	I/O	–	–	–	–	–	–	O, PD
W4	VDDBU	Power supply	VDDBU	I	–	–	–	–	–	–	–	–	I
W1	GNDBU	Ground	GNDBU	I	–	–	–	–	–	–	–	–	I
G8 N9	VDDCORE	Power supply	VDDCORE	I	–	–	–	–	–	–	–	–	I
B10 D9 D10 F9 H8 J8 J12 K11 L8 L10 L12 M9 M10 M11 V18 W18	GNDCORE	Ground	GNDCORE	I	–	–	–	–	–	–	–	–	I
J7 J11 K7 K8 L9 L11 N10	VCCCORE	Power supply	VCCCORE	I	–	–	–	–	–	–	–	–	I
C14 D17 E10 E12 F14 H12 H16 K13 K17 M13	VDDIODDR	Power supply	VDDIODDR	I	–	–	–	–	–	–	–	–	I

Table 3-1: TFBGA361 Pin Description (Continued)

Pin	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State[1]
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
C13 C17 E11 F10 G11 G14 G17 J13 K18 L13	GNDIODDR	Ground	GNDIODDR	I	–	–	–	–	–	–	–	–	I
M8 N7 P15 R9	VDDIOM	Power supply	VDDIOM	I	–	–	–	–	–	–	–	–	I
M7 M12 N8 P9	GNDIOM	Ground	GNDIOM	I	–	–	–	–	–	–	–	–	I
B8 C8 E8 F8	GNDIOP	Ground	GNDIOP	I	–	–	–	–	–	–	–	–	I
H7 K6 L5 M6	VDDIOP	Power supply	VDDIOP	I	–	–	–	–	–	–	–	–	I
F7 G6 G7 J6 L6 N6	GNDIOP	Ground	GNDIOP	I	–	–	–	–	–	–	–	–	I
V13	VDDUTMIC	Power supply	VDDUTMIC	I	–	–	–	–	–	–	–	–	I
W13 W17	VDDUTMII	Power supply	VDDUTMII	I	–	–	–	–	–	–	–	–	I
P13	GNDUTMI	Ground	GNDUTMI	I	–	–	–	–	–	–	–	–	I
W10	VDDPLLA	Power supply	VDDPLLA	I	–	–	–	–	–	–	–	–	I
L7	GNDPLL	Ground	GNDPLL	I	–	–	–	–	–	–	–	–	I
P14	VDDOSC	Power supply	VDDOSC	I	–	–	–	–	–	–	–	–	I
N13	GNDOSC	Ground	GNDOSC	I	–	–	–	–	–	–	–	–	I
A11	GNDIOP	Ground	GNDIOP	I	–	–	–	–	–	–	–	–	I
C9 N11 P12	VDDANA	Power supply	VDDANA	I	–	–	–	–	–	–	–	–	I
C10 H11 N12	GNDANA	Ground	GNDANA	I	–	–	–	–	–	–	–	–	I
R14	VDDFUSE	Power supply	VDDFUSE	I	–	–	–	–	–	–	–	–	I
R15	GNDFUSE	Ground	GNDFUSE	I	–	–	–	–	–	–	–	–	I

Table 3-1: TFBGA361 Pin Description (Continued)

Pin	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State[1]
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
U1	–	Not connected	–	–	–	–	–	–	–	–	–	–	–

Note 1: The GPIOs' reset state is not guaranteed during the powerup phase. During this phase, the GPIOs are in input pullup mode and they take their reset value only after VDDCORE POR reset has been released. If a GPIO must be at level zero at powerup, it is recommended to connect an external pulldown to guarantee this state.

3.2 289-ball LFBGA Package Pinout

In this package, the DDRC datapath is reduced to 16 bits.

Table 3-2: LFBGA289 Pin Description

Pin	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State[1]
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
C5	VDDIOP	GPIO	PA0	I/O	–	–	LCDDAT0	O	–	–	TMS	I	TMS, PU, ST
F6	VDDIOP	GPIO	PA1	I/O	–	–	LCDDAT1	O	–	–	–	–	PIO, I, PU, ST
F5	VDDIOP	GPIO_CLK	PA2	I/O	–	–	LCDDAT2	O	G1_TXCK	I	–	–	PIO, I, PU, ST
B5	VDDIOP	GPIO_CLK	PA3	I/O	–	–	LCDDAT3	O	G1_RXCK	I	–	–	PIO, I, PU, ST
E5	VDDIOP	GPIO	PA4	I/O	–	–	LCDDAT4	O	G1_TXEN	O	–	–	PIO, I, PU, ST
A5	VDDIOP	GPIO	PA5	I/O	–	–	LCDDAT5	O	G1_TXER	O	–	–	PIO, I, PU, ST
A4	VDDIOP	GPIO	PA6	I/O	–	–	LCDDAT6	O	G1_CRS	I	–	–	PIO, I, PU, ST
E4	VDDIOP	GPIO	PA7	I/O	–	–	LCDDAT7	O	–	–	–	–	PIO, I, PU, ST
B4	VDDIOP	GPIO	PA8	I/O	–	–	LCDDAT8	O	–	–	TCK	I	TCK, PU
D4	VDDIOP	GPIO	PA9	I/O	–	–	LCDDAT9	O	G1_COL	I	–	–	PIO, I, PU, ST
C4	VDDIOP	GPIO	PA10	I/O	–	–	LCDDAT10	O	G1_RXDV	I	–	–	PIO, I, PU, ST
A3	VDDIOP	GPIO	PA11	I/O	–	–	LCDDAT11	O	G1_RXER	I	–	–	PIO, I, PU, ST
F4	VDDIOP	GPIO	PA12	I/O	–	–	LCDDAT12	O	G1_RX0	I	–	–	PIO, I, PU, ST
F3	VDDIOP	GPIO	PA13	I/O	–	–	LCDDAT13	O	G1_RX1	I	–	–	PIO, I, PU, ST
D3	VDDIOP	GPIO	PA14	I/O	–	–	LCDDAT14	O	G1_TX0	O	–	–	PIO, I, PU, ST
B3	VDDIOP	GPIO	PA15	I/O	–	–	LCDDAT15	O	G1_TX1	O	–	–	PIO, I, PU, ST
G3	VDDIOP	GPIO	PA16	I/O	–	–	LCDDAT16	O	–	–	NTRST	I	NTRST, PU, ST
E3	VDDIOP	GPIO	PA17	I/O	–	–	LCDDAT17	O	–	–	–	–	PIO, O, LOW
C3	VDDIOP	GPIO	PA18	I/O	–	–	LCDDAT18	O	G1_RX2	I	–	–	PIO, O, LOW
A2	VDDIOP	GPIO	PA19	I/O	–	–	LCDDAT19	O	G1_RX3	I	–	–	PIO, O, LOW
G5	VDDIOP	GPIO	PA20	I/O	–	–	LCDDAT20	O	G1_TX2	O	–	–	PIO, I, PU, ST
A1	VDDIOP	GPIO	PA21	I/O	–	–	LCDDAT21	O	G1_TX3	O	–	–	PIO, I, PU, ST
D2	VDDIOP	GPIO	PA22	I/O	–	–	LCDDAT22	O	G1_MDC	O	–	–	PIO, I, PU, ST
E2	VDDIOP	GPIO	PA23	I/O	–	–	LCDDAT23	O	G1_MDIO	I/O	–	–	PIO, I, PU, ST
G4	VDDIOP	GPIO_CLK	PA24	I/O	–	–	LCDPWM	O	PCK0	O	–	–	PIO, I, PU, ST
C2	VDDIOP	GPIO	PA25	I/O	–	–	LCDDISP	O	TD0	O	–	–	PIO, I, PU, ST
B2	VDDIOP	GPIO	PA26	I/O	–	–	LCDVSYNC	O	PWMH0	O	SPI1_NPCS1	O	PIO, I, PU, ST

Table 3-2: LFBGA289 Pin Description (Continued)

Pin	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State(1)
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
H3	VDDIOP	GPIO	PA27	I/O	–	–	LCDHSYNC	O	PWML0	O	SPI1_NPCS2	O	PIO, I, PU, ST
F2	VDDIOP	GPIO_CLK2	PA28	I/O	–	–	LCDPCK	O	PWMH1	O	SPI1_NPCS3	O	PIO, I, PU, ST
B1	VDDIOP	GPIO	PA29	I/O	–	–	LCDDEN	O	PWML1	O	–	–	PIO, I, PU, ST
C1	VDDIOP	GPIO	PA30	I/O	–	–	TWD0	I/O	–	–	–	–	PIO, I, PU, ST
H5	VDDIOP	GPIO	PA31	I/O	–	–	TWCK0	O	–	–	–	–	PIO, I, PU, ST
D1	VDDIOP	GPIO_CLK	PB0	I/O	–	–	G0_TXCK	I	–	–	–	–	PIO, I, PU, ST
H4	VDDIOP	GPIO_CLK	PB1	I/O	–	–	G0_RXCK	I	SCK2	I/O	ISI_PCK	I	PIO, I, PU, ST
G2	VDDIOP	GPIO	PB2	I/O	–	–	G0_TXEN	O	–	–	–	–	PIO, I, PU, ST
E1	VDDIOP	GPIO	PB3	I/O	–	–	G0_TXER	O	CTS2	I	ISI_VSYNC	I	PIO, I, PU, ST
F1	VDDIOP	GPIO	PB4	I/O	–	–	G0_CRS	I	RXD2	I	ISI_HSYNC	I	PIO, I, PU, ST
J3	VDDIOP	GPIO	PB5	I/O	–	–	G0_COL	I	TXD2	O	PCK2	O	PIO, I, PU, ST
H2	VDDIOP	GPIO	PB6	I/O	–	–	G0_RXDV	I	–	–	–	–	PIO, I, PU, ST
J5	VDDIOP	GPIO	PB7	I/O	–	–	G0_RXER	I	–	–	–	–	PIO, I, PU, ST
J2	VDDIOP	GPIO	PB8	I/O	–	–	G0_RX0	I	–	–	–	–	PIO, I, PU, ST
G1	VDDIOP	GPIO	PB9	I/O	–	–	G0_RX1	I	–	–	–	–	PIO, I, PU, ST
H1	VDDIOP	GPIO_CLK	PB10	I/O	–	–	G0_RX2	I	PCK2	O	PWML1	O	PIO, I, PU, ST
J4	VDDIOP	GPIO	PB11	I/O	–	–	G0_RX3	I	RTS2	O	PWMH1	O	PIO, I, PU, ST
J1	VDDIOP	GPIO	PB12	I/O	–	–	G0_TX0	O	–	–	–	–	PIO, I, PU, ST
K6	VDDIOP	GPIO	PB13	I/O	–	–	G0_TX1	O	–	–	–	–	PIO, I, PU, ST
K1	VDDIOP	GPIO	PB14	I/O	–	–	G0_TX2	O	SPI2_NPCS1	O	PWMH0	O	PIO, I, PU, ST
K2	VDDIOP	GPIO	PB15	I/O	–	–	G0_TX3	O	SPI2_NPCS2	O	PWML0	O	PIO, I, PU, ST
L1	VDDIOP	GPIO	PB16	I/O	–	–	G0_MDC	O	–	–	–	–	PIO, I, PU, ST
K3	VDDIOP	GPIO	PB17	I/O	–	–	G0_MDIO	I/O	–	–	–	–	PIO, I, PU, ST
L2	VDDIOP	GPIO	PB18	I/O	–	–	SPI1_MISO	I/O	D8	I/O	–	–	PIO, I, PU, ST
M1	VDDIOP	GPIO	PB19	I/O	–	–	SPI1_MOSI	I/O	D9	I/O	–	–	PIO, I, PU, ST
N1	VDDIOP	GPIO_CLK	PB20	I/O	–	–	SPI1_SPCK	I/O	D10	I/O	–	–	PIO, I, PU, ST
K4	VDDIOP	GPIO	PB21	I/O	–	–	SPI1_NPCS0	I/O	D11	I/O	–	–	PIO, I, PU, ST
P1	VDDIOP	GPIO	PB22	I/O	–	–	SPI1_NPCS1	O	D12	I/O	–	–	PIO, I, PU, ST
M2	VDDIOP	GPIO	PB23	I/O	–	–	SPI1_NPCS2	O	D13	I/O	–	–	PIO, I, PU, ST
R1	VDDIOP	GPIO	PB24	I/O	–	–	DRXD	I	D14	I/O	TDI	I	TDI, PU, ST
T1	VDDIOP	GPIO	PB25	I/O	–	–	DTXD	O	D15	I/O	TDO	O	TDO, ST
K5	VDDIOP	GPIO_CLK	PB26	I/O	–	–	PCK0	O	RK0	I/O	PWMH0	O	PIO, I, PU, ST
U1	VDDIOP	GPIO	PB27	I/O	–	–	SPI1_NPCS3	O	TK0	I/O	PWML0	O	PIO, I, PU, ST
K7	VDDIOP	GPIO	PB28	I/O	–	–	SPI2_NPCS3	O	TD0	O	PWMH1	O	PIO, I, PU, ST
L3	VDDIOP	GPIO	PB29	I/O	–	–	TWD2	I/O	RD0	I	PWML1	O	PIO, O, LOW
L4	VDDIOP	GPIO	PB30	I/O	–	–	TWCK2	O	RF0	I/O	–	–	PIO, O, LOW
U2	VDDIOP	GPIO	PB31	I/O	–	–	–	–	TF0	I/O	–	–	PIO, I, PU, ST

Table 3-2: LFBGA289 Pin Description (Continued)

Pin	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State[1]
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
U7	VDDIOM	GPIO	PC0	I/O	–	–	SPI0_MISO	I/O	PWMH2	O	ISI_D8	I	PIO, I, PU, ST
U9	VDDIOM	GPIO	PC1	I/O	–	–	SPI0_MOSI	I/O	PWML2	O	ISI_D9	I	PIO, I, PU, ST
U8	VDDIOM	GPIO_CLK	PC2	I/O	–	–	SPI0_SPCK	I/O	PWMH3	O	ISI_D10	I	PIO, I, PU, ST
M8	VDDIOM	GPIO	PC3	I/O	–	–	SPI0_NPCS0	I/O	PWML3	O	ISI_D11	I	PIO, I, PU, ST
U10	VDDIOM	MCI_CLK	PC4	I/O	–	–	SPI0_NPCS1	O	MCI0_CK	I/O	PCK1	O	PIO, I, PU, ST
N7	VDDIOM	GPIO	PC5	I/O	–	–	D0	I/O	MCI0_CDA	I/O	–	–	PIO, I, PU, ST
T7	VDDIOM	GPIO	PC6	I/O	–	–	D1	I/O	MCI0_DA0	I/O	–	–	PIO, I, PU, ST
G17	VDDIOM	GPIO	PC7	I/O	–	–	D2	I/O	MCI0_DA1	I/O	–	–	PIO, I, PU, ST
J13	VDDIOM	GPIO	PC8	I/O	–	–	D3	I/O	MCI0_DA2	I/O	–	–	PIO, I, PU, ST
P7	VDDIOM	GPIO	PC9	I/O	–	–	D4	I/O	MCI0_DA3	I/O	–	–	PIO, I, PU, ST
R7	VDDIOM	GPIO	PC10	I/O	–	–	D5	I/O	MCI0_DA4	I/O	–	–	PIO, I, PU, ST
U11	VDDIOM	GPIO	PC11	I/O	–	–	D6	I/O	MCI0_DA5	I/O	–	–	PIO, I, PU, ST
T8	VDDIOM	GPIO	PC12	I/O	–	–	D7	I/O	MCI0_DA6	I/O	–	–	PIO, I, PU, ST
U12	VDDIOM	GPIO	PC13	I/O	–	–	NRD/NANDOE	O	MCI0_DA7	I/O	–	–	PIO, I, PU, ST
R8	VDDIOM	GPIO	PC14	I/O	–	–	NWE/NANDWE	O	–	–	–	–	PIO, I, PU, ST
U13	VDDIOM	GPIO	PC15	I/O	–	–	NCS3	O	–	–	–	–	PIO, I, PU, ST
P8	VDDIOM	GPIO	PC16	I/O	–	–	NANDRDY	I	–	–	–	–	PIO, I, PU, ST
T9	VDDIOM	GPIO	PC17	I/O	–	–	A21/NANDALE	O	–	–	–	–	A21
T11	VDDIOM	GPIO	PC18	I/O	–	–	A22/NANDCLE	O	–	–	–	–	A22
T10	VDDIOM	GPIO	PC19	I/O	–	–	ISI_D0	I	TK1	I/O	–	–	PIO, I, PU, ST
N8	VDDIOM	GPIO	PC20	I/O	–	–	ISI_D1	I	TF1	I/O	–	–	PIO, I, PU, ST
P15	VDDIOM	GPIO	PC21	I/O	–	–	ISI_D2	I	TD1	O	–	–	PIO, I, PU, ST
N16	VDDIOM	GPIO	PC22	I/O	–	–	ISI_D3	I	RF1	I/O	–	–	PIO, I, PU, ST
P16	VDDIOM	GPIO	PC23	I/O	–	–	ISI_D4	I	RD1	I	–	–	PIO, I, PU, ST
N17	VDDIOM	GPIO	PC24	I/O	–	–	ISI_D5	I	RK1	I	PCK1	O	PIO, I, PU, ST
P17	VDDIOM	GPIO	PC25	I/O	–	–	ISI_D6	I	TWD3	I/O	URXD1	I	PIO, I, PU, ST
M17	VDDIOM	GPIO	PC26	I/O	–	–	ISI_D7	I	TWCK3	O	UTXD1	O	PIO, I, PU, ST
T12	VDDANA	GPIO_ANA	PC27	I/O	AD0	–	–	I	SPI0_NPCS1	O	PWML0	O	PIO, I, PU, ST
R13	VDDANA	GPIO_ANA	PC28	I/O	AD1	–	–	I	SPI0_NPCS2	O	PWML1	O	PIO, I, PU, ST
T13	VDDANA	GPIO_ANA	PC29	I/O	AD2	–	–	I	SPI0_NPCS3	O	PWMFI0	O	PIO, I, PU, ST
R14	VDDANA	GPIO_ANA	PC30	I/O	AD3	–	–	I	–	–	PWMH0	O	PIO, I, PU, ST
R15	VDDANA	GPIO_ANA	PC31	I/O	AD4	–	–	I	–	–	PWMH1	I	PIO, I, PU, ST
L7	VDDIOP	GPIO_CLK	PD8	I/O	–	–	PCK0	O	–	–	–	–	PIO, I, PU, ST
P2	VDDIOP	GPIO	PD9	I/O	–	–	FIQ	I	–	–	–	–	PIO, I, PU, ST
T2	VDDIOP	GPIO	PD10	I/O	–	–	CTS0	I	–	–	–	–	PIO, I, PU, ST
M3	VDDIOP	GPIO	PD11	I/O	–	–	RTS0	O	SPI2_MISO	I/O	–	–	PIO, I, PU, ST
N2	VDDIOP	GPIO	PD12	I/O	–	–	RXD0	I	–	–	–	–	PIO, O, PD

Table 3-2: LFBGA289 Pin Description (Continued)

Pin	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State[1]
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
M4	VDDIOP	GPIO	PD13	I/O	–	–	TXD0	O	SPI2_MOSI	I/O	–	–	PIO, I, PU, ST
K8	VDDIOP	GPIO	PD14	I/O	–	–	CTS1	I	–	–	–	–	PIO, I, PU, ST
N3	VDDIOP	GPIO	PD15	I/O	–	–	RTS1	O	SPI2_SPCK	I/O	–	–	PIO, I, PU, ST
L8	VDDIOP	GPIO	PD16	I/O	–	–	RXD1	I	–	–	–	–	PIO, I, PU, ST
P3	VDDIOP	GPIO	PD17	I/O	–	–	TXD1	O	SPI2_NPCS0	I/O	–	–	PIO, I, PU, ST
P9	VDDANA	GPIO	PD18	I/O	–	–	–	–	–	–	–	–	PIO, I, PU, ST
M10	VDDANA	GPIO	PD19	I/O	–	–	–	–	–	–	–	–	PIO, I, PU, ST
R9	VDDANA	GPIO	PD20	I/O	–	–	–	–	–	–	–	–	PIO, I, PU, ST
R10	VDDANA	GPIO	PD21	I/O	–	–	–	–	–	–	–	–	PIO, I, PU, ST
P10	VDDANA	GPIO	PD22	I/O	–	–	–	–	–	–	–	–	PIO, I, PU, ST
L11	VDDANA	GPIO	PD23	I/O	–	–	–	–	–	–	–	–	PIO, I, PU, ST
R11	VDDANA	GPIO	PD24	I/O	–	–	–	–	–	–	–	–	PIO, I, PU, ST
M11	VDDANA	GPIO	PD25	I/O	–	–	–	–	–	–	–	–	PIO, I, PU, ST
P11	VDDANA	GPIO	PD26	I/O	–	–	–	–	–	–	–	–	PIO, I, PU, ST
L12	VDDANA	GPIO	PD27	I/O	–	–	–	–	–	–	–	–	PIO, I, PU, ST
L9	VDDIOP	GPIO_CLK	PD28	I/O	–	–	SCK0	I/O	–	–	–	–	PIO, I, PU, ST
R2	VDDIOP	GPIO_CLK	PD29	I/O	–	–	SCK1	I/O	–	–	–	–	PIO, I, PU, ST
L5	VDDIOP	GPIO	PD30	I/O	–	–	–	–	–	–	–	–	PIO, I, PU, ST
L6	VDDIOP	GPIO_CLK	PD31	I/O	–	–	SPI0_NPCS2	O	PCK1	O	–	–	PIO, I, PU, ST
N14	VDDIOM	MCI_CLK	PE0	I/O	–	–	A0/NBS0	O	MCI0_CDB	I/O	CTS4	I	O, HIGH
N13	VDDIOM	EBI	PE1	I/O	–	–	A1	O	MCI0_DB0	I/O	–	–	O, HIGH
M16	VDDIOM	EBI	PE2	I/O	–	–	A2	O	MCI0_DB1	I/O	–	–	A2, LOW
M15	VDDIOM	EBI	PE3	I/O	–	–	A3	O	MCI0_DB2	I/O	–	–	A3, LOW
J16	VDDIOM	EBI	PE4	I/O	–	–	A4	O	MCI0_DB3	I/O	–	–	A4, LOW
L17	VDDIOM	EBI	PE5	I/O	–	–	A5	O	CTS3	I	–	–	A5, LOW
J17	VDDIOM	EBI	PE6	I/O	–	–	A6	O	TIOA3	I/O	–	–	PIO, O, LOW
K17	VDDIOM	EBI	PE7	I/O	–	–	A7	O	TIOB3	I/O	PWMFI1	I	A7, LOW
H16	VDDIOM	EBI	PE8	I/O	–	–	A8	O	TCLK3	I	PWML3	O	A8, LOW
L16	VDDIOM	EBI	PE9	I/O	–	–	A9	O	TIOA2	I/O	–	–	A9, LOW
L14	VDDIOM	EBI	PE10	I/O	–	–	A10	O	TIOB2	I/O	–	–	A10, LOW
H17	VDDIOM	EBI	PE11	I/O	–	–	A11	O	TCLK2	I	–	–	A11, LOW
L15	VDDIOM	EBI	PE12	I/O	–	–	A12	O	TIOA1	I/O	PWMH2	O	A12, LOW
G16	VDDIOM	EBI	PE13	I/O	–	–	A13	O	TIOB1	I/O	PWML2	O	A13, LOW
K12	VDDIOM	EBI	PE14	I/O	–	–	A14	O	TCLK1	I	PWMH3	O	A14, LOW
F16	VDDIOM	EBI	PE15	I/O	–	–	A15	O	SCK3	I/O	TIOA0	I/O	A15, LOW
K16	VDDIOM	EBI	PE16	I/O	–	–	A16	O	RXD3	I	TIOB0	I/O	A16, LOW
F17	VDDIOM	EBI	PE17	I/O	–	–	A17	O	TXD3	O	TCLK0	I	A17, LOW

Table 3-2: LFBGA289 Pin Description (Continued)

Pin	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State[1]
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
E16	VDDIOM	EBI	PE18	I/O	–	–	A18	O	TIOA5	I/O	MCI1_CK	I/O	A18, LOW
D16	VDDIOM	EBI	PE19	I/O	–	–	A19	O	TIOB5	I/O	MCI1_CDA	I/O	A19, LOW
E17	VDDIOM	EBI	PE20	I/O	–	–	A20	O	TCLK5	I	MCI1_DA0	I/O	A20, LOW
D17	VDDIOM	EBI	PE21	I/O	–	–	A23	O	TIOA4	I/O	MCI1_DA1	I/O	A23, LOW
C16	VDDIOM	EBI	PE22	I/O	–	–	A24	O	TIOB4	I/O	MCI1_DA2	I/O	A24, LOW
C17	VDDIOM	EBI	PE23	I/O	–	–	A25	O	TCLK4	I	MCI1_DA3	I/O	A25, LOW
K13	VDDIOM	EBI	PE24	I/O	–	–	NCS0	O	RTS3	O	–	–	NCS0, HIGH
B17	VDDIOM	EBI	PE25	I/O	–	–	NCS1	O	SCK4	I/O	IRQ	I	NCS1, HIGH
K14	VDDIOM	EBI	PE26	I/O	–	–	NCS2	O	RXD4	I	A18	O	NCS2, HIGH
K15	VDDIOM	EBI	PE27	I/O	–	–	NWR1/NBS1	O	TXD4	O	–	–	PIO, I, PU, ST
J10	VDDIOM	EBI	PE28	I/O	–	–	NWAIT	I	RTS4	O	A19	O	PIO, I, PU, ST
P6	VDDIOP	DIB	PE29	I/O	–	–	DIBP	O	URXD0	I	TWD1	I/O	PIO, O, LOW
N6	VDDIOP	DIB	PE30	I/O	–	–	DIBN	O	UTXD0	O	TWCK1	O	PIO, O, LOW
K9	VDDIOP	GPIO	PE31	I/O	–	–	ADTRG	I	–	–	–	–	PIO, O, LOW
R3	VDDBU	SYSC	TST	I	–	–	–	–	–	–	–	–	I, PD, ST
T15	VDDIOP	CLOCK	XIN	I	–	–	–	–	–	–	–	–	I
U15	VDDIOP	CLOCK	XOUT	O	–	–	–	–	–	–	–	–	O
U5	VDDBU	CLOCK	XIN32	I	–	–	–	–	–	–	–	–	I
T5	VDDBU	CLOCK	XOUT32	O	–	–	–	–	–	–	–	–	O
U4	VDDBU	SYSC	SHDN	O	–	–	–	–	–	–	–	–	O, PU
T4	VDDBU	SYSC	WKUP	I	–	–	–	–	–	–	–	–	I, ST
M5	VDDBU	PIOBU	PIOBU0	I	–	–	–	–	–	–	–	–	I, PU
R4	VDDBU	PIOBU	PIOBU1	I	–	–	–	–	–	–	–	–	I, PU
P4	VDDBU	PIOBU	PIOBU2	I	–	–	–	–	–	–	–	–	I, PU
R5	VDDBU	PIOBU	PIOBU3	I	–	–	–	–	–	–	–	–	I, PU
N5	VDDBU	PIOBU	PIOBU4	I	–	–	–	–	–	–	–	–	I, PU
P5	VDDBU	PIOBU	PIOBU5	I	–	–	–	–	–	–	–	–	I, PU
N4	VDDBU	PIOBU	PIOBU6	I	–	–	–	–	–	–	–	–	I, PU
R6	VDDBU	PIOBU	PIOBU7	I	–	–	–	–	–	–	–	–	I, PU
U3	VDDBU	PIOBU	NRST	I	–	–	–	–	–	–	–	–	I
T3	VDDBU	SYSC	JTAGSEL	I	–	–	–	–	–	–	–	–	I, PD
B12	VDDIODDR	DDR_IO	DDR_A0	O	–	–	–	–	–	–	–	–	O, LOW
A12	VDDIODDR	DDR_IO	DDR_A1	O	–	–	–	–	–	–	–	–	O, LOW
E15	VDDIODDR	DDR_IO	DDR_A2	O	–	–	–	–	–	–	–	–	O, LOW
G11	VDDIODDR	DDR_IO	DDR_A3	O	–	–	–	–	–	–	–	–	O, LOW
C13	VDDIODDR	DDR_IO	DDR_A4	O	–	–	–	–	–	–	–	–	O, LOW
D12	VDDIODDR	DDR_IO	DDR_A5	O	–	–	–	–	–	–	–	–	O, LOW

Table 3-2: LFBGA289 Pin Description (Continued)

Pin	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State[1]
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
C11	VDDIODDR	DDR_IO	DDR_A6	O	–	–	–	–	–	–	–	–	O, LOW
A14	VDDIODDR	DDR_IO	DDR_A7	O	–	–	–	–	–	–	–	–	O, LOW
F12	VDDIODDR	DDR_IO	DDR_A8	O	–	–	–	–	–	–	–	–	O, LOW
C14	VDDIODDR	DDR_IO	DDR_A9	O	–	–	–	–	–	–	–	–	O, LOW
G12	VDDIODDR	DDR_IO	DDR_A10	O	–	–	–	–	–	–	–	–	O, LOW
A13	VDDIODDR	DDR_IO	DDR_A11	O	–	–	–	–	–	–	–	–	O, LOW
B13	VDDIODDR	DDR_IO	DDR_A12	O	–	–	–	–	–	–	–	–	O, LOW
C10	VDDIODDR	DDR_IO	DDR_A13	O	–	–	–	–	–	–	–	–	O, LOW
J14	VDDIODDR	DDR_IO	DDR_D0	I/O	–	–	–	–	–	–	–	–	I, HiZ
B16	VDDIODDR	DDR_IO	DDR_D1	I/O	–	–	–	–	–	–	–	–	I, HiZ
J9	VDDIODDR	DDR_IO	DDR_D2	I/O	–	–	–	–	–	–	–	–	I, HiZ
J12	VDDIODDR	DDR_IO	DDR_D3	I/O	–	–	–	–	–	–	–	–	I, HiZ
A16	VDDIODDR	DDR_IO	DDR_D4	I/O	–	–	–	–	–	–	–	–	I, HiZ
A15	VDDIODDR	DDR_IO	DDR_D5	I/O	–	–	–	–	–	–	–	–	I, HiZ
H10	VDDIODDR	DDR_IO	DDR_D6	I/O	–	–	–	–	–	–	–	–	I, HiZ
B15	VDDIODDR	DDR_IO	DDR_D7	I/O	–	–	–	–	–	–	–	–	I, HiZ
G15	VDDIODDR	DDR_IO	DDR_D8	I/O	–	–	–	–	–	–	–	–	I, HiZ
H13	VDDIODDR	DDR_IO	DDR_D9	I/O	–	–	–	–	–	–	–	–	I, HiZ
C15	VDDIODDR	DDR_IO	DDR_D10	I/O	–	–	–	–	–	–	–	–	I, HiZ
D15	VDDIODDR	DDR_IO	DDR_D11	I/O	–	–	–	–	–	–	–	–	I, HiZ
H12	VDDIODDR	DDR_IO	DDR_D12	I/O	–	–	–	–	–	–	–	–	I, HiZ
H11	VDDIODDR	DDR_IO	DDR_D13	I/O	–	–	–	–	–	–	–	–	I, HiZ
B14	VDDIODDR	DDR_IO	DDR_D14	I/O	–	–	–	–	–	–	–	–	I, HiZ
H9	VDDIODDR	DDR_IO	DDR_D15	I/O	–	–	–	–	–	–	–	–	I, HiZ
A17	VDDIODDR	DDR_IO	DDR_DQM0	O	–	–	–	–	–	–	–	–	O, LOW
H14	VDDIODDR	DDR_IO	DDR_DQM1	O	–	–	–	–	–	–	–	–	O, LOW
H15	VDDIODDR	DDR_IO	DDR_DQS0	I/O	–	–	–	–	–	–	–	–	O, LOW
F15	VDDIODDR	DDR_IO	DDR_DQS1	I/O	–	–	–	–	–	–	–	–	O, LOW
J15	VDDIODDR	DDR_IO	DDR_DQSN0	I/O	–	–	–	–	–	–	–	–	O, HIGH
F14	VDDIODDR	DDR_IO	DDR_DQSN1	I/O	–	–	–	–	–	–	–	–	O, HIGH
C9	VDDIODDR	DDR_IO	DDR_CS	O	–	–	–	–	–	–	–	–	O, LOW
B10	VDDIODDR	DDR_IO	DDR_CLK	O	–	–	–	–	–	–	–	–	O
B11	VDDIODDR	DDR_IO	DDR_CLKN	O	–	–	–	–	–	–	–	–	O
D9	VDDIODDR	DDR_IO	DDR_CKE	O	–	–	–	–	–	–	–	–	O, LOW
A10	VDDIODDR	DDR_IO	DDR_RAS	O	–	–	–	–	–	–	–	–	O, LOW
A11	VDDIODDR	DDR_IO	DDR_CAS	O	–	–	–	–	–	–	–	–	O, LOW
C12	VDDIODDR	DDR_IO	DDR_WE	O	–	–	–	–	–	–	–	–	O, LOW