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ATSAMB11XR/ZR

Ultra-Low Power Bluetooth® Low Energy SiP/Module

Introduction

The ATSAMB11-XR2100A is an ultra-low power Bluetooth Low Energy (BLE) 4.2 System in a Package (SiP) with Integrated MCU, transceiver, modem, MAC, PA, Transmit/Receive (T/R) switch, and Power Management Unit (PMU). It is a standalone Cortex® -M0 applications processor with embedded Flash memory and BLE connectivity.

The Bluetooth SIG-qualified Bluetooth Low Energy protocol stack is stored in a dedicated ROM. The firmware includes L2CAP service layer protocols, Security Manager, Attribute protocol (ATT), Generic Attribute Profile (GATT), and the Generic Access Profile (GAP). Additionally, example applications are available for application profiles such as proximity, thermometer, heart rate and blood pressure, and many others.

The ATSAMB11-XR2100A provides a compact footprint and various embedded features, such as a 26 MHz crystal oscillator.

The ATSAMB11-ZR210CA is a fully certified module that contains the ATSAMB11-XR2100A and all external RF circuitry required, including a ceramic high-gain antenna. The user simply places the module into their PCB and provides power with a 32.768 kHz Real-Time Clock (RTC) or crystal, and an I/O path.

Microchip BluSDK Smart offers a comprehensive set of tools and reference applications for several Bluetooth SIG defined profiles and a custom profile. The BluSDK Smart will help the user quickly evaluate, design and develop BLE products with the ATSAMB11-XR2100A and ATSAMB11-ZR210CA.

The ATSAMB11-XR2100A and associated ATSAMB11-ZR210CA module have passed the Bluetooth SIG certification for interoperability with the Bluetooth Low Energy 4.2 specification.

Features

- 2.4 GHz Transceiver and Modem:
  - -92.5 dBm receiver sensitivity
  - -55 dBm to +3.5 dBm programmable TX output power
  - Integrated T/R switch
  - Single wire antenna connection (ATSAMB11-XR2100A)
  - Incorporated chip antenna (ATSAMB11-ZR210CA)
- Processor Features:
  - ARM® Cortex®-M0 32-bit processor
  - Serial Wire Debug (SWD) interface
  - Four-channel Direct Memory Access (DMA) controller
  - Watchdog timer
- Memory:

  - 128 KB embedded Random Access Memory (RAM)
  - 128 KB embedded ROM
  - 256 KB stacked Flash memory
- Hardware Security Accelerators:
  - Advanced Encryption Standard (AES)-128
  - Secure Hash Algorithm (SHA)-256
- Peripherals:
  - 23 digital and 4 mixed-signal General Purpose Input Outputs (GPIOs) with 96 kOhm internal programmable pull-up or down resistors and retention capability, and one wake-up GPIO with 96 kOhm internal pull-up resistor
  - Two Serial Peripheral Interface (SPI) Master/Slave
  - Two Inter-Integrated Circuit (I^2C) Master/Slave
  - Two UART
  - One SPI flash interface (used for accessing the internal stacked flash)
  - Three-axis quadrature decoder
  - Four Pulse Width Modulation (PWM) channels
  - Three General Purpose Timers and one Always-On (AON) sleep Timer
  - 4-channel, 11-bit Analog-to-Digital Converter (ADC)
- Clock:
  - Integrated 26 MHz RC oscillator
  - Integrated 2 MHz RC oscillator
  - 26 MHz crystal oscillator (XO)
  - 32.768 kHz Real Time Clock crystal oscillator (RTC XO)
- Ultra-Low Power:
  - 2.03 µA sleep current
  - 4.17 mA peak TX current (1)
  - 5.26 mA peak RX current
  - 16.4 µA average advertisement current (three channels, 1s interval) (2)
- Integrated Power Management:
  - 2.3V to 4.3V battery voltage range
  - 2.3V to 3.6V input range for I/O (limited by Flash memory)
  - Fully integrated Buck DC/DC converter
- Temperature Range:
  - -40°C to 85°C
- Package:
  - 49-pin FLGA SiP package 5.50 mm x 4.50 mm
  - 35-pin module package 10.541 mm x 7.503 mm

Note:

1. TX output power - 0 dBm.
2. Advertisement channels - 3 ; Advertising interval - 1 second ; Advertising event type - Connectable undirected; Advertisement data payload size - 31 octets.

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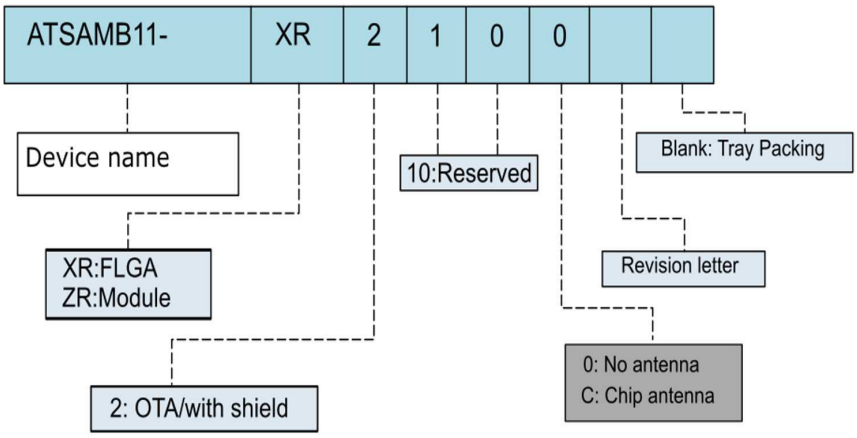
1. Ordering Information

Table 1-1. Ordering Details

Model Number	Ordering Code	Package	Description	Regulatory Information
ATSAMB11-XR2100A	ATSAMB11-XR2100A	5.5 mm x 4.5 mm	ATSAMB11 SiP tray	N/A
ATSAMB11-ZR210CA	ATSAMB11-ZR210CA	7.5 mm X 10.5 mm	ATSAMB11 module with chip antenna	FCC, ISED, CE

Figure 1-1. Marking information



2. Package Information

Table 2-1. ATSAMB11-XR2100A SiP 49 Package Information

Parameter	Value	Units	Tolerance
Package size	5.50 x 4.50	mm	±0.05 mm
Pad count	49		
Total thickness	1.40	mm	Max
Tolerance (maximum pad pitch)	0.40	mm	±0.05 mm
Pad width	0.21		
Exposed pad size	0.50 x 0.50		

Note: For drawing details, see Figure 18-1.

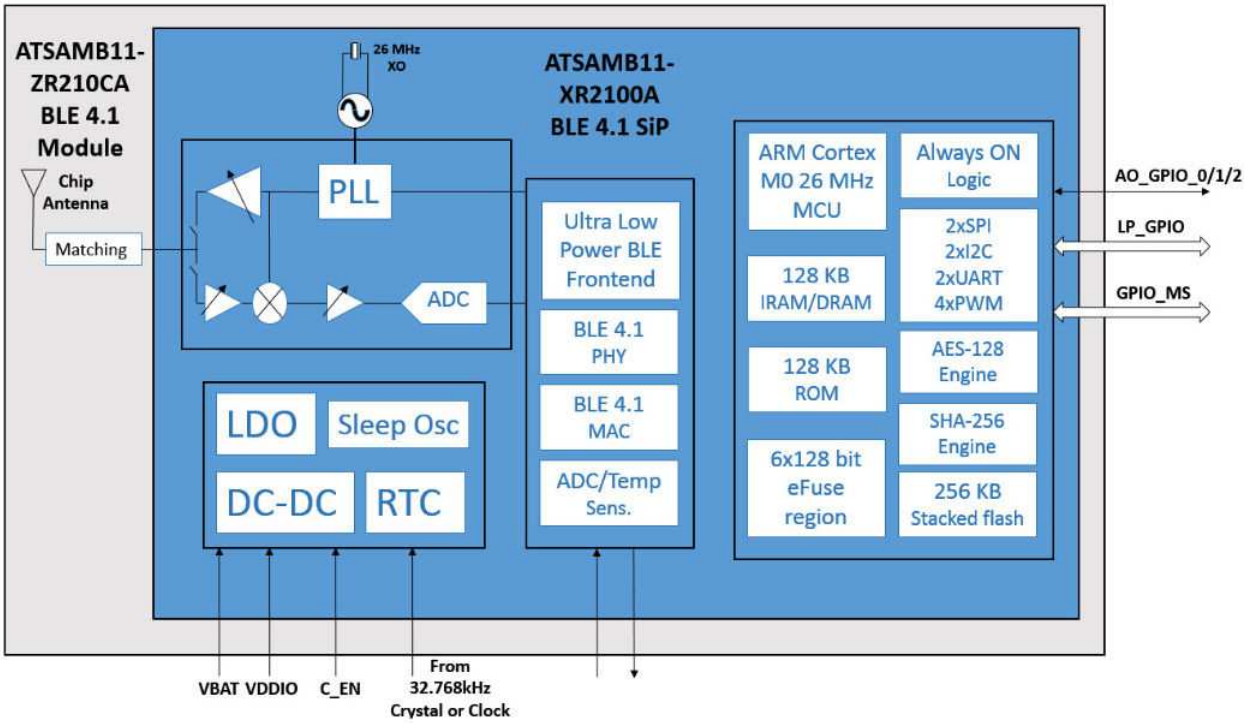
Table 2-2. ATSAMB11-ZR210CA Module Information

Parameter	Value	Units	Tolerance
Package size	7.503 x 10.541	mm	Untoleranced dimension
Pad count	35		
Total thickness	1.868	mm	Untoleranced dimensions
Pad pitch	0.61		
Pad width	0.406		
Exposed pad size	2.705 x 2.705		

Note: For drawing details, see Figure 18-2.

3. Block Diagram

Figure 3-1. Block Diagram



4. Pinout Information

The ATSAMB11-XR2100A is offered in an exposed pad 49-pin SiP package. This package has an exposed paddle that must be connected to the system board ground. The SiP package pin assignment is shown in the figure below. The colored shading is used to indicate the pin type as follows:

- Red – analog
- Green – digital I/O (switchable power domain)
- Blue – digital I/O (always-on power domain)
- Yellow – power
- Purple – PMU
- Shaded green/red – configurable mixed-signal GPIO (digital/analog)

The ATSAMB11-ZR210CA module is a castellated PCB with the ATSAMB11-XR2100A integrated with a matched chip antenna. The pins are identified in the pin description table. The ATSAMB11-XR2100A also contains a paddle pad on the bottom of the PCB, that must be soldered to the system ground.

Figure 4-1. ATSAMB11-XR2100A Pin Assignment

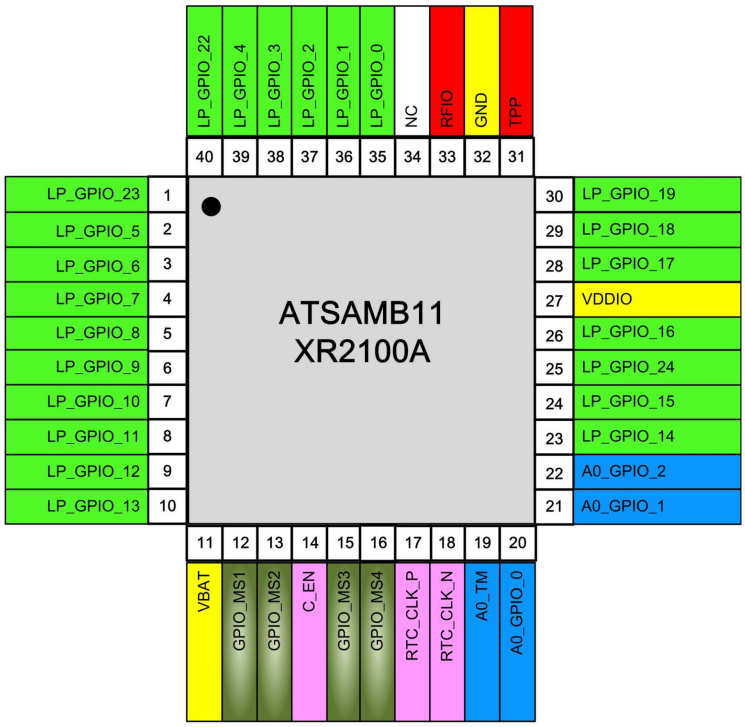
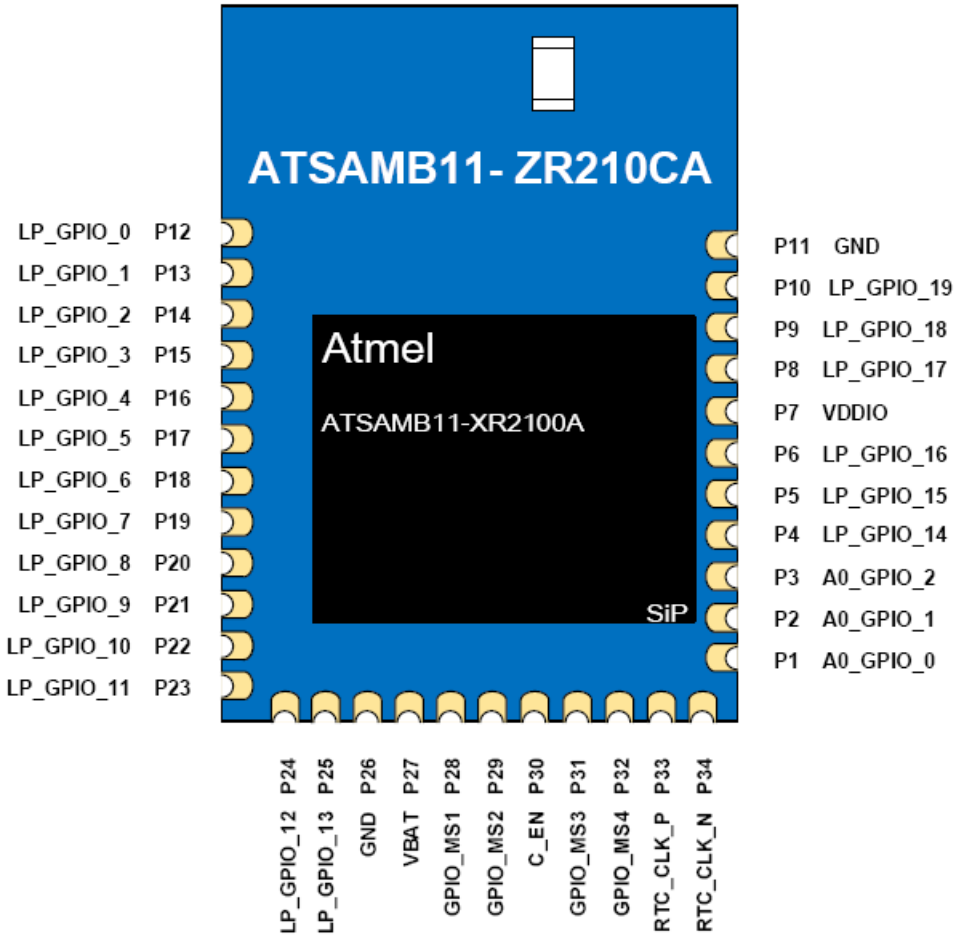


Figure 4-2. ATSAMB11-ZR210CA Pin Descriptions



The following table lists the pin assignments for both the ATSAMB11-XR2100A and the ATSAMB11-ZR210CA.

Table 4-1. ATSAMB11-XR2100A and ATSAMB11-ZR210CA Pin Description

ATSAMB11-XR2100A Pin #	ATSAMB11-ZR210CA Pin #	Pin Name	Pin Type	Description / Default Function
1	-	LP_GPIO_23	Digital I/O	GPIO with Programmable Pull Up/Down
2	17	LP_GPIO_5	Digital I/O	GPIO with Programmable Pull Up/Down
3	18	LP_GPIO_6	Digital I/O	GPIO with Programmable Pull Up/Down
4	19	LP_GPIO_7	Digital I/O	GPIO with Programmable Pull Up/Down
5	20	LP_GPIO_8(1)	Digital I/O	GPIO with Programmable Pull Up/Down

ATSAMB11-XR2100A Pin #	ATSAMB11-ZR210CA Pin #	Pin Name	Pin Type	Description / Default Function
6	21	LP_GPIO_9(1)	Digital I/O	GPIO with Programmable Pull Up/Down
7	22	LP_GPIO_10	Digital I/O	GPIO with Programmable Pull Up/Down
8	23	LP_GPIO_11	Digital I/O	GPIO with Programmable Pull Up/Down
9	24	LP_GPIO_12	Digital I/O	GPIO with Programmable Pull Up/Down
10	25	LP_GPIO_13	Digital I/O	GPIO with Programmable Pull Up/Down
11	27	VBAT	Power supply	Power supply pin for the DC/DC convertor
12	28	GPIO_MS1	Mixed Signal I/O	Configurable to be a GPIO digital and analog signal. Only analog input for ADC interface.
13	29	GPIO_MS2	Mixed Signal I/O	Configurable to be a GPIO digital and analog signal. Only analog input for ADC interface.
14	30	C_EN	Digital Input	Can be used to control the state of PMU. High level enables the module; low-level places module in Power-Down mode.
15	31	GPIO_MS3	Mixed Signal I/O	Configurable to be a GPIO digital and analog signal. Only analog input for ADC interface.
16	32	GPIO_MS4	Mixed Signal I/O	Configurable to be a GPIO digital and analog signal. Only analog input for ADC interface.
17	33	RTC_CLK_P	Analog	Crystal pin or External clock supply, see 32.768 kHz RTC Crystal Oscillator (RTC XO)
18	34	RTC_CLK_N	Analog	Crystal pin or External clock supply, see 32.768 kHz RTC Crystal Oscillator (RTC XO)
19	-	AO_TM	Digital Input	Always-On Test Mode. Connect to GND

ATSAMB11-XR2100A Pin #	ATSAMB11-ZR210CA Pin #	Pin Name	Pin Type	Description / Default Function
20	1	AO_GPIO_0	Always On Digital I/O, Programmable Pull-Up	To be held in logic '0' GND to allow the device to enter Ultra_Low_Power mode Can be used to Wake-up the device from Ultra_Low_Power mode.
21	2	AO_GPIO_1	Always On. Digital I/O, Programmable Pull- Up	GPIO with Programmable Pull Up
22	3	AO_GPIO_2	Always On. Digital I/O, Programmable Pull- Up	GPIO with Programmable Pull Up
23	4	LP_GPIO_14	Digital I/O	GPIO with Programmable Pull Up/Down
24	5	LP_GPIO_15	Digital I/O	GPIO with Programmable Pull Up/Down
25	-	LP_GPIO_24	Digital I/O	GPIO with Programmable Pull Up/Down
26	6	LP_GPIO_16	Digital I/O	GPIO with Programmable Pull Up/Down
27	7	VDDIO	Power supply	Power supply pin for the I/O pins. Can be less than or equal to voltage supplied at VBAT
28	8	LP_GPIO_17	Digital I/O	GPIO with Programmable Pull Up/Down
29	9	LP_GPIO_18	Digital I/O	GPIO with Programmable Pull Up/Down
30	10	LP_GPIO_19	Digital I/O	GPIO with Programmable Pull Up/Down
31	-	TPP		Do not connect
32	11, 26	GND	Ground	
33	-	RFIO	Analog I/O	RX input and TX output. Single-ended RF I/O; To be connected to antenna
34	-	NC		Do not connect
35	12	LP_GPIO_0	Digital I/O	SWD clock

ATSAMB11-XR2100A Pin #	ATSAMB11-ZR210CA Pin #	Pin Name	Pin Type	Description / Default Function
36	13	LP_GPIO_1	Digital I/O	SWD I/O
37	14	LP_GPIO_2	Digital I/O	GPIO with Programmable Pull Up/Down
38	15	LP_GPIO_3	Digital I/O	GPIO with Programmable Pull Up/Down
39	16	LP_GPIO_4	Digital I/O	GPIO with Programmable Pull Up/Down
40	-	LP_GPIO_22	Digital I/O	GPIO with Programmable Pull Up/Down
41 - 49	35	Paddle	Ground	Exposed paddle must be soldered to system ground

Note:

1. These GPIO pads are high-drive pads. Refer Table 17-3.

5. Device States

This section includes details on the description and controlling of the Device states.

5.1 Description of Device States

The ATSAMB11-XR2100A and the ATSAMB11-ZR210CA have multiple device states, depending on the state of the ARM processor and BLE subsystem.

Note: The ARM is required to be powered on, if the BLE subsystem is active.

- BLE_On_Transmit – Device is actively transmitting a BLE signal.
- BLE_On_Receive – Device is in active receive state.
- MCU_Only – Device has ARM processor powered-on and BLE subsystem powered-down.
- Ultra_Low_Power – BLE subsystem and ARM processor are powered-down.
- Power_Down – Device core supply off.

5.1.1 Controlling the Device States

The following pins are used to switch between the main device states:

- C_EN – used to enable PMU
- VDDIO – I/O supply voltage from an external power supply
- AO_GPIO_0 - can be used to control the device from entering/exiting Ultra_Low_Power mode

To be in the Power_Down state, the VDDIO supply must be turned on and the C_EN must be maintained at logic low (at GND level). To switch between the Power_Down state and the MCU_Only state, C_EN is to be maintained at logic high (VDDIO voltage level). Once the device is in the MCU_Only state, all other state transitions are controlled entirely by software. When VDDIO supply is turned off and C_EN is in logic low, the chip is powered off with no leakage.

When VDDIO supply is turned off, voltage cannot be applied to the ATSAMB11-XR2100A pins, as each pin contains an ESD diode from the pin to supply. This diode turns on, when a voltage higher than one diode-drop is supplied to the pin.

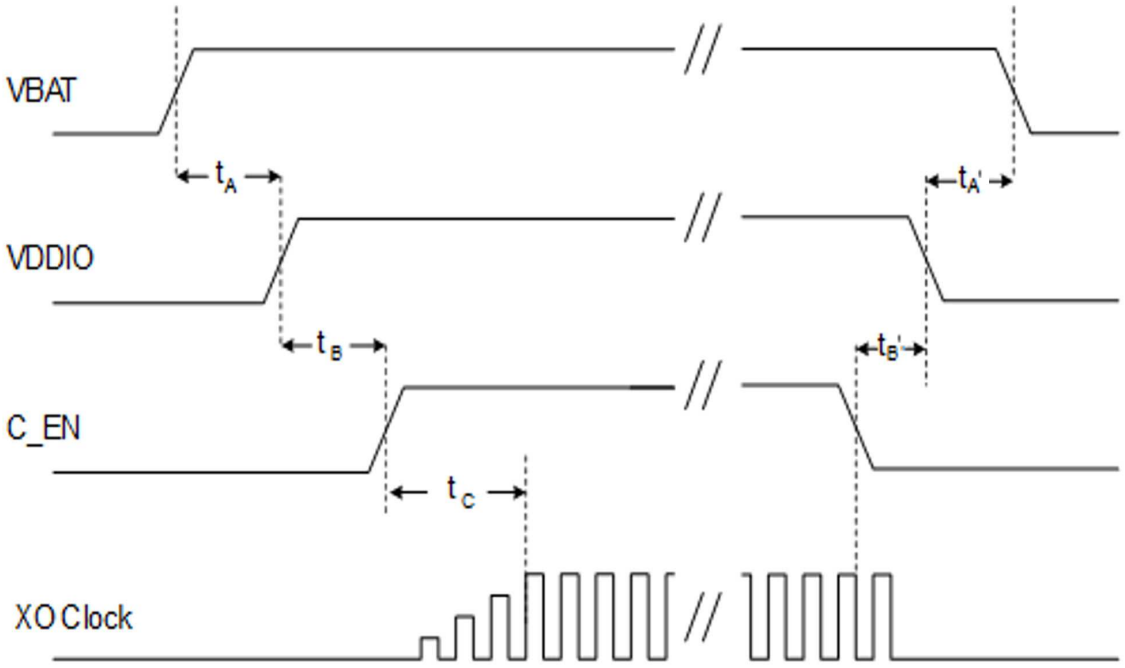
If voltage is to be applied to the signal pads, while the chip is in a low-power state, the VDDIO supply must be on, so that the Power_Down state is used. Similarly, to prevent the pin-to-ground diode from turning on, do not apply a voltage to any pin that is more than one diode-drop below ground.

The AO_GPIO_0 pin can be used to control the device from entering and exiting Ultra_Low_Power mode. When AO_GPIO_0 is maintained in logic high state, the device will not enter Ultra_Low_Power mode. When the AO_GPIO_0 is maintained in logic low, the device will enter Ultra_Low_Power mode provided there are no BLE events to be handled.

5.2 Power Sequences

The power sequences and timing parameters for the ATSAMB11-XR2100A and ATSAMB11-ZR210CA, are illustrated below.

Figure 5-1. Power-up/Power-down Sequence



The timing parameters are provided in following table.

Table 5-1. Power-up/Power-down Sequence Timing

Parameter	Min.	Max.	Units	Description	Notes
t_A	0		ms	VBAT rise to VDDIO rise	VBAT and VDDIO can rise simultaneously or can be tied together
t_B	0			VDDIO rise to C_EN rise	C_EN must not rise before VDDIO. C_EN must be driven high or low, not left floating.
t_C	10		µs	C_EN rise to 31.25 kHz (2 MHz/64) oscillator stabilizing	
$t_{B'}$	0		ms	C_EN fall to VDDIO fall	C_EN must fall before VDDIO. C_EN must be driven high or low, not left floating.
$t_{A'}$	0			VDDIO fall to VBAT fall	VBAT and VDDIO can fall simultaneously or be tied together

5.3 Digital and Mixed-Signal I/O Pin Behavior during Power-Up Sequences

The following table represents I/O pin states corresponding to device power modes.

Table 5-2. I/O Pin Behavior in the Different Device States (1)

Device State	VDDIO	CHIP_EN	Output Driver	Input Driver	Pull Up/Down Resistor (2)
Power_Down: core supply off	High	Low	Disabled (Hi-Z)	Disabled	Disabled
Power-on Reset: core supply on, POR hard reset pulse on	High	High	Disabled (Hi-Z)	Disabled	Disabled (3)
Power-on Default: core supply on, device out of reset but not programmed yet	High	High	Disabled (Hi-Z)	Enabled(4)	Enabled Pull-Up (4)
MCU_Only, BLE_On: core supply on, device programmed by firmware	High	High	Programmed by firmware for each pin: Enabled or Disabled (Hi-Z) (5) ,when Enabled driving 0 or 1	Opposite of Output Driver state: Disabled or Enabled (5)	Programmed by firmware for each pin: Enabled or Disabled, Pull-Up or Pull- Down(5)
Ultra_Low_Power: core supply on for always-on domain, core supply off for switchable domains	High	High	Retains previous state(6) for each pin: Enabled or Disabled (Hi-Z), when Enabled driving 0 or 1	Opposite of Output Driver state: Disabled or Enabled(6)	Retains previous state (6) for each pin: Enabled or Disabled, Pull-Up or Pull-Down

Note:

1. This table applies to all three types of I/O pins (digital switchable domain GPIOs, digital always-on/wake-up GPIO, and mixed-signal GPIOs) unless otherwise noted.
2. Pull-up/down resistor value is 96 kOhm ±10%.
3. In Power-on Reset state, the pull-up resistor is enabled in the always-on/wake-up GPIO only.
4. In Power-on Default state, the input drivers and pull-up/down resistors are disabled in the mixed-signal GPIOs only (mixed-signal GPIOs are defaulted to analog mode, see the note below).
5. Mixed-signal GPIOs can be programmed to be in analog or digital mode for each pin: when programmed to analog mode (default), the output driver, input driver, and pull-up/down resistors are all disabled.
6. In Ultra_Low_Power state, the always-on/wake-up GPIO does not have retention capability and behaves same as in MCU_Only or BLE_On states, also for mixed-signal GPIOs programming analog mode overrides retention functionality for each pin.

6. Processor Architecture

6.1 ARM Subsystem

The ATSAMB11-XR2100A and ATSAMB11-ZR210CA have an ARM Cortex-M0 32-bit processor. It is responsible for controlling the BLE Subsystem and handling all application features.

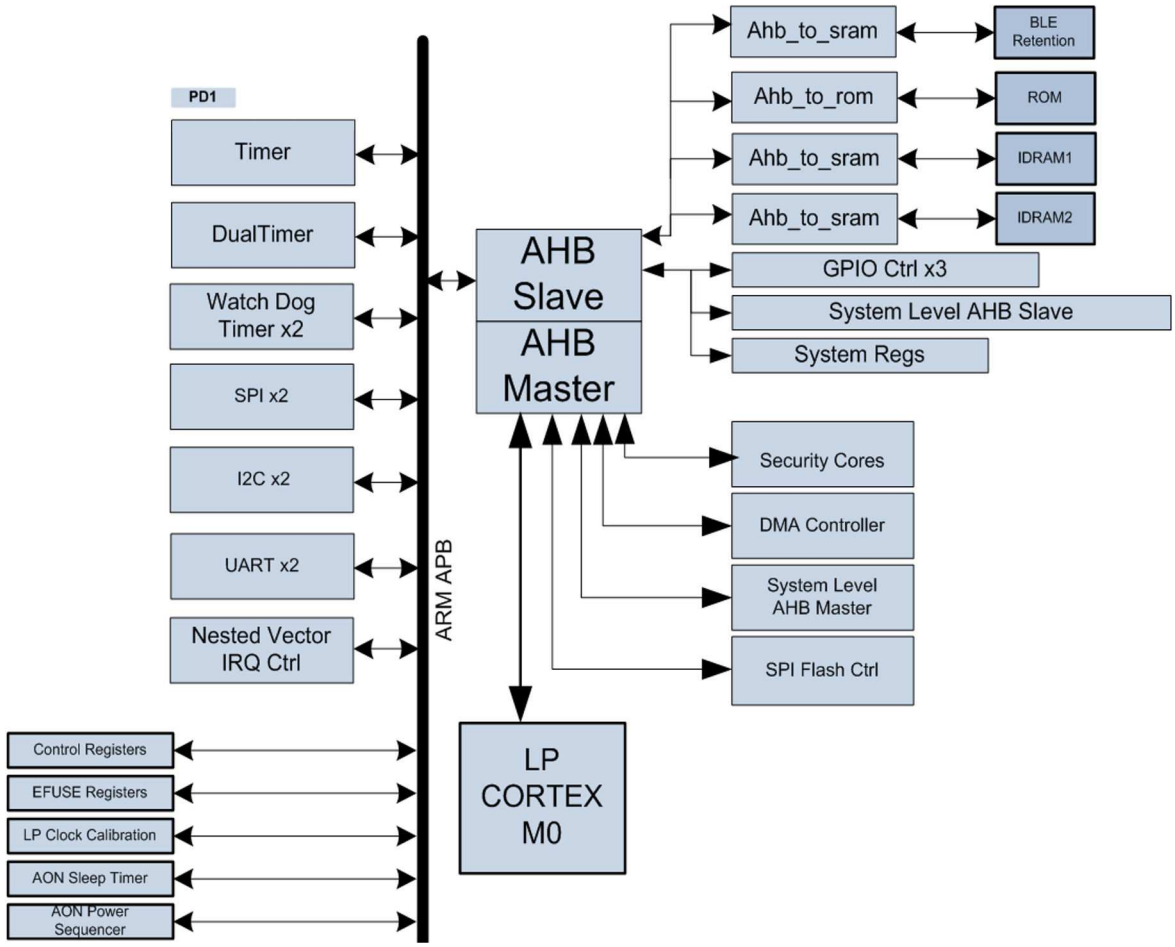
The Cortex-M0 Microcontroller consists of a full 32-bit processor capable of addressing 4GB of memory. It has a RISC like load/store instruction set and internal 3-stage Pipeline Von Neumann architecture.

The Cortex-M0 processor provides a single system-level interface using AMBA technology to provide high speed, low latency memory accesses.

The Cortex-M0 processor implements a complete hardware debug solution with four hardware breakpoint and two watchpoint options. This provides high system visibility of the processor, memory, and peripherals through a 2-pin Serial Wire Debug (SWD) port that is ideal for microcontrollers and other small package devices.

ATSAMB11 is running a proprietary RTOS tightly coupled with FW in the ROM and the user can not override it. SysTick timer is being used by the stack and will not be available for usage by the application.

Figure 6-1. ARM Cortex-M0 Subsystem



6.1.1 Features

The processor features and benefits are:

- Tight integration with the system peripherals to reduce area and development costs
- Thumb instruction set combines high code density with 32-bit performance
- Integrated sleep modes using a Wakeup Interrupt Controller for low power consumption
- Deterministic and high-performance interrupt handling via Nested Vector Interrupt Controller for time-critical applications
- Serial Wire Debug reduces the number of pins required for debugging
- DMA engine for Peripheral-to-Memory, Memory-to-Memory, and Memory-to-Peripheral operation

6.1.2 Wakeup Sources

Ultra_Low_Power is the lowest possible power state for the system. In Ultra_Low_Power state, ARM Cortex-M0, BLE core, GPIO's, and all other peripheral cores are powered-down. Only AON-GPIO_0 and AON-Sleep timer are functional in this state.

ATSAMB11 contains the following wake-up sources that wake up the system from Ultra_Low_Power mode:

- BLE events
- AON-GPIO_0
- AON-Sleep timer

6.2 Cortex M0 Peripherals

- System Control Space (SCS)
  The processor provides debug through registers in the SCS. For more details, refer to the Cortex-M0 Technical Reference Manual (http://www.arm.com).
- Nested Vectored Interrupt Controller (NVIC)
  External interrupt signals connect to the NVIC, and the NVIC prioritizes the interrupts. Software can set the priority of each interrupt. The NVIC and the Cortex-M0 processor core are closely coupled, providing low latency interrupt processing and efficient processing of late arriving interrupts. For more details, refer to the Cortex-M0 Technical Reference Manual (http://www.arm.com).
- System Timer (SysTick)
  The System Timer is a 24-bit timer clocked by CLK_CPU that extends the functionality of both the processor and the NVIC. For more details, refer to the Cortex-M0 Technical Reference Manual (http://www.arm.com).
- System Control Block (SCB)
  The System Control Block provides system implementation information, and system control. This includes configuration, control, and reporting of the system exceptions. For more details, refer to the Cortex-M0 Devices Generic User Guide (http://www.arm.com).

6.2.1 Cortex M0 Peripheral Memory Map

- 0xE000E000 System Control Space (SCS)
- 0xE000E010 System Timer (SysTick)
- 0xE000E100 Nested Vectored Interrupt Controller (NVIC)
- 0xE000ED00 System Control Block (SCB)

6.3 Nested Vector Interrupt Controller

External interrupt signals are connected to the NVIC, and the NVIC prioritizes the interrupts. Software can set the priority of each interrupt. The NVIC and the Cortex-M0 processor core are closely coupled to provide low-latency interrupt processing and efficient processing of late arriving interrupts.

All NVIC registers are accessible via word transfers and are little endian. Any attempt to read or write a half-word or byte individually is unpredictable.

The NVIC allows the CPU to be able to individually enable or disable each interrupt source, and hold each interrupt until it is serviced and cleared by the CPU.

Table 6-1. NVIC Register Summary

Name	Description
ISER	Interrupt Set-Enable Register
ICER	Interrupt Clear-Enable Register
ISPR	Interrupt Set-Pending Register
ICPR	Interrupt Clear-Pending Register
IPR0-IPR7	Interrupt Priority Registers

Note: For a description of each register, see the Cortex-M0 documentation from ARM (http://www.arm.com).

6.3.1 Functional Description

The Cortex-M0 NVIC is connected to 32 IRQ sources. The following table lists the interrupts that are available in ATSAMB11. Also, some of the interrupts are marked as RESERVED as they are used by the BLE stack and are used for firmware in general. Applications must refrain from registering an ISR for those interrupts as it affects the chip functionality.

Perform the following steps to enable an interrupt:

- Configure and enable peripheral interrupt using peripheral-specific registers. Refer to the intended peripheral chapter for configuring interrupt.
- The ISRs are mapped in RAM memory called interrupt vector table. 0x10000000 is the start address of first ISR index 0 and 4 bytes are allocated for each ISR index in incrementing order. The specific peripheral ISR handler to be registered by assigning the handler address to this interrupt vector table.
- Set the NVIC priority of the interrupt if required. IPR0-IPR7 ARM NVIC registers are used to set the priority level for individual interrupt sources. IRQ number of the specific interrupt source as per the following table is used. Only two bits are allocated for each interrupt source. Therefore, four priority levels (0, 1, 2, and 3) are possible. The priority value is zero by default, and is also the highest priority.
  Note: The BLE subsystem is handled by ROM firmware and BLE-specific interrupts are with default priority value equal to zero (highest priority). It is only possible to set the same or lesser priority than BLE-specific for other peripheral interrupts. Same or lesser priority interrupts cannot interrupt the running ISR. The latency to serve other peripheral interrupt when BLE ISR is servicing depends on the full execution time for BLE ISR.
- Enable NVIC interrupt of specific IRQ numbers using ISER register.

Table 6-2. ATSAMB11 Interrupt Vector Table

IRQ Number	ISR Index	Interrupt Source	Muxability
-15	1	Reset	Non-muxable
-14	2	NMI	Non-muxable
-13	3	Hard Fault	Non-muxable
-5	11	SVC	Non-muxable
-2	14	Pending SV	Non-muxable
-1	15	SysTick	Non-muxable
0	16	UART0 RX	Muxable
1	17	UART0 TX	Muxable
2	18	UART1 RX	Muxable
3	19	UART1 TX	Muxable
4	20	SPI0 RX	Muxable
5	21	SPI0 TX	Muxable
6	22	SPI1 RX	Muxable
7	23	SPI1 TX	Muxable
8	24	I^2C0 RX	Muxable
9	25	I^2C0 TX	Muxable
10	26	I^2C1 RX	Muxable
11	27	I^2C1 TX	Muxable
12	28	Watchdog 0	Muxable(1)
13	29	Watchdog 1	Muxable
14	30	ARM® Dual Timer	Muxable
15	31	BLE Peripheral Register	Muxable
16	32	EFuse Out of Reset	Muxable(1)
17	33	BLE Security	Muxable(1)
18	34	SPI Flash	Muxable
19	35	Calibration Done	Muxable(1)
20	36	Brown Out Detected	Muxable
21	37	BLE specific	Non-Muxable(1)
22	38	BLE specific	Non-Muxable(1)
23	39	GPIO 0 Combined	Non-Muxable
24	40	GPIO 1 Combined	Non-Muxable

IRQ Number	ISR Index	Interrupt Source	Muxability
25	41	GPIO 2 combined	Non-Muxable
26	42	ARM timer	Non-Muxable(1)
27	43	AON sleep timer	Non-Muxable
28	44	BLE specific	Non-Muxable(1)
29	45	BLE specific	Non-Muxable(1)
30	46	BLE specific	Non-Muxable(1)
31	47	BLE specific	Non-Muxable(1)

Note:

1. This ISR index is used by the BLE stack. Applications must refrain from registering an ISR as it affects the chip functionality.

For more details on configuration options for muxable interrupts, see Muxable Interrupt.

7. Memory Subsystem

The Cortex-M0 core uses a 128 KB instruction/boot ROM along with a 128 KB shared instruction and data RAM.

7.1 Shared Instruction and Data Memory

The Instruction and Data Memory (IDRAM1 and IDRAM2) contains instructions and data used by the ARM. The 128 KB size of IDRAM1 and IDRAM2 is used for the BLE subsystem and also for the user application. IDRAM1 contains three 32 KB memories and IDRAM2 contains two 16 KB memories that are accessible to the ARM and used for instruction/data storage.

RAM memory is used by the user application as well as ROM firmware for data storage. The memory split-up between application and firmware might change when there is a BluSDK SMART release. Refer to BluSDK SMART Example Profiles Application User Guide for the memory map of this memory section.

7.2 ROM

The ROM is used to store the boot code and BLE firmware, stack, and selected user profiles. The ROM contains the 128 KB memory that is accessible to the ARM. The Boot loader code stored in ROM loads the application from Flash to RAM.

7.3 BLE Retention Memory

The BLE functionality requires 8 KB state, instruction, and data to be retained in memory, when the processor either goes into Sleep mode or Power down mode. The RAM is separated into specific power domains to allow tradeoff in power consumption with retention memory size.

7.4 Non-Volatile Memory

The ATSAMB11-XR2100A and ATSAMB11-ZR210CA have 768 bits of non-volatile eFuse memory that can be read by the CPU after device reset. This memory region is one-time- programmable. It is partitioned into six 128-bit banks. Each bank is divided into four blocks with each block containing 32 bits of memory locations. This non-volatile, one-time-programmable memory is used to store customer specific parameters as listed below.

- 26 MHz XO Calibration information
- BT address

The bit map for the block containing the above parameters is detailed in the following figures.

Figure 7-1. Bank 5 Block 0

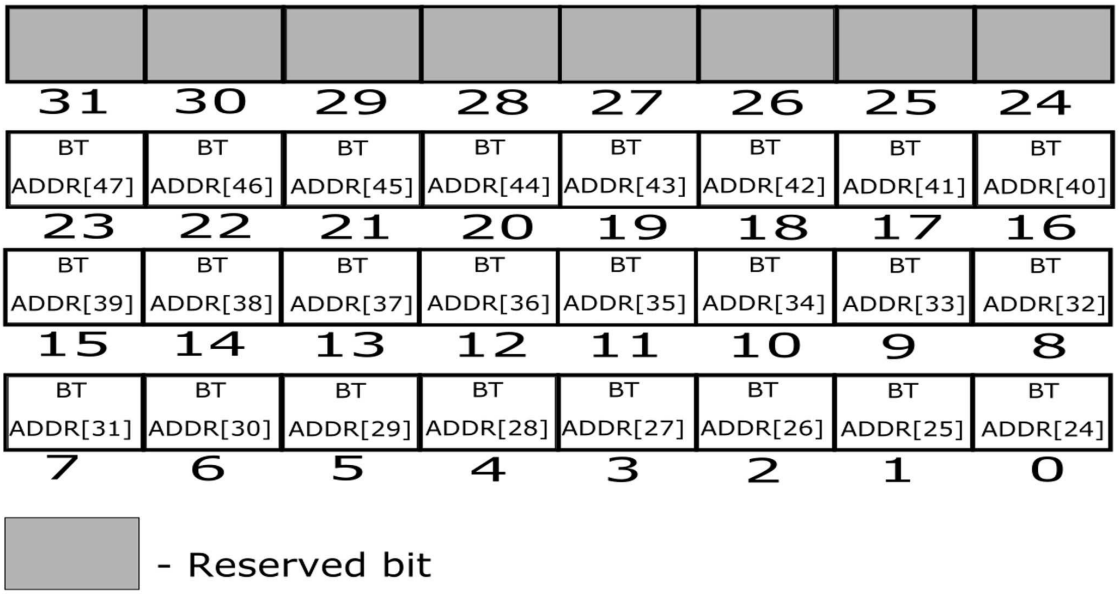


Figure 7-2. Bank 5 Block 1

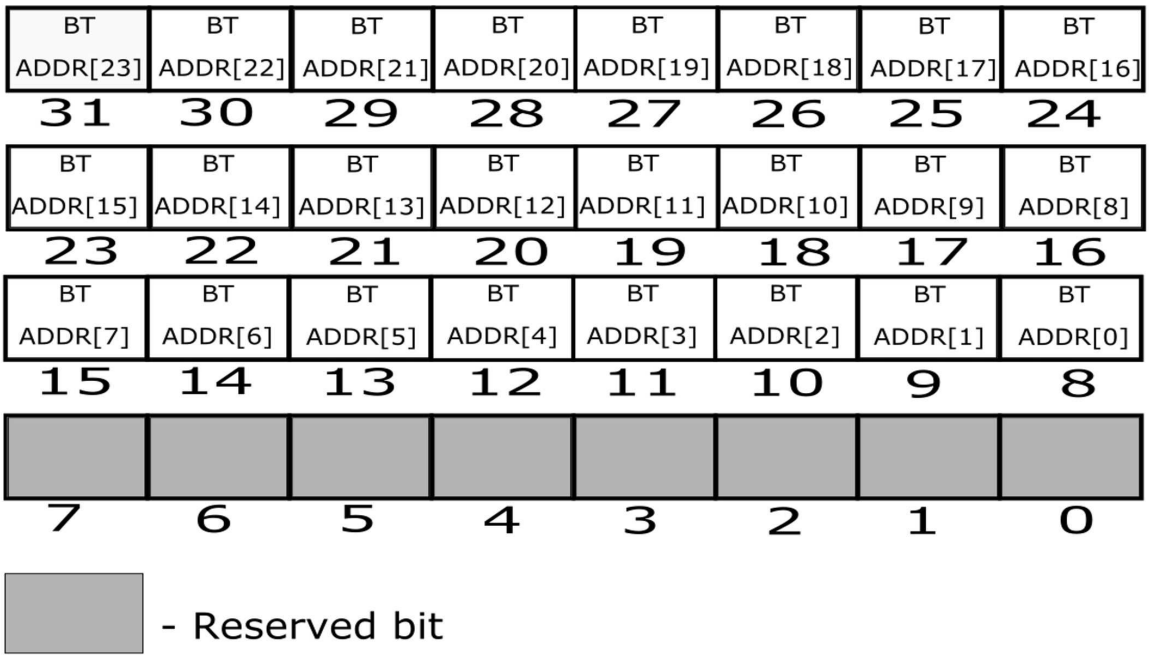
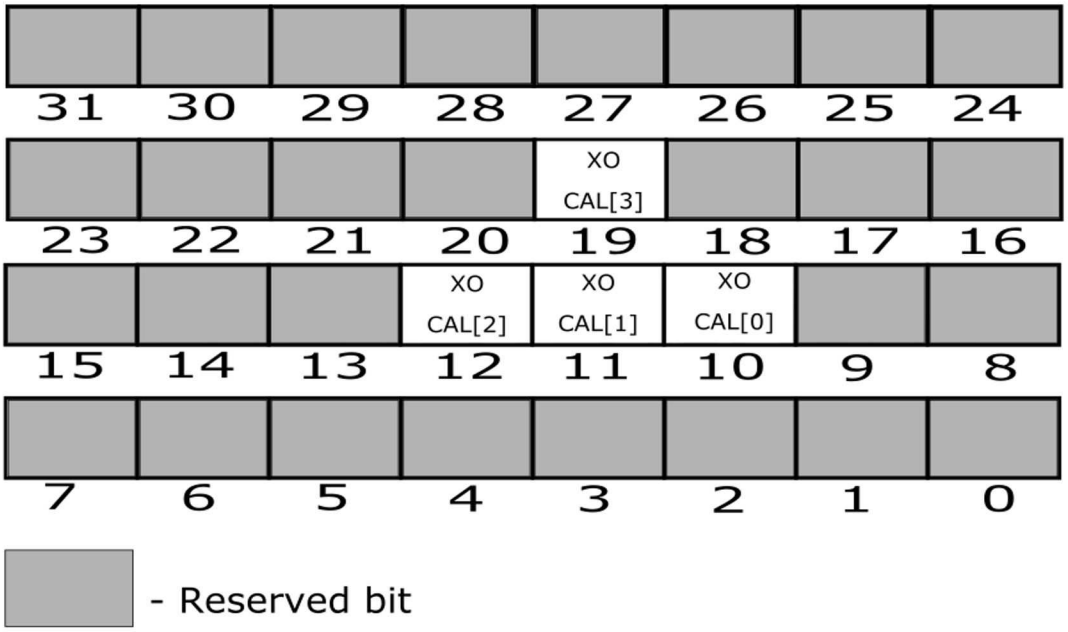


Figure 7-3. Bank 5 Block 3



The bits that are not depicted in the above register description are all reserved for future use.

7.4.1 26 MHz XO Calibration information

Information for both ATSAMB11-XR2100A and ATSAMB11-ZR210CA will be pre-programmed.

7.4.2 BT Address

These bits contain the BT address used by the user application. For ATSAMB11-ZR210CA modules, the BT address is pre-programmed. For ATSAMB11-XR2100A, the user must purchase the MAC address from IEEE and program it to the designated bit locations of the non-volatile memory.

7.4.3 Flash Memory

The ATSAMB11-XR2100A and ATSAMB11-ZR210CA have 256 kB of Flash memory, stacked on top of the MCU and BLE SoC. It is accessed through the SPI Flash controller.

Flash memory features are:

- 256 bytes per programmable page
- Uniform 4 kB Sectors, 32 kB & 64 kB Blocks
- Sector Erase (4 Kbyte)
- Block Erase (32 K or 64 Kbyte)
- Page program up to 256 bytes <1 ms
- More than 100,000 erase/write cycles and more than 20-year data retention
- 2.3 V to 3.6 V supply range