Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

SAMB11 QFN SOC

Ultra-low Power BLE 4.1 SoC

DATASHEET

Description

The SAMB11 is an ultra-low power Bluetooth® SMART (BLE 4.1) System on a Chip with Integrated MCU, Transceiver, Modem, MAC, PA, TR Switch, and Power Management Unit (PMU). It is a standalone Cortex®-M0 applications processor with embedded Flash memory and BLE connectivity.

The qualified Bluetooth Smart protocol stack is stored in dedicated ROM, the firmware includes L2CAP service layer protocols, Security Manager, Attribute protocol (ATT), Generic Attribute Profile (GATT) and the Generic Access Profile (GAP). Additionally, application profiles such as Proximity, Thermometer, Heart Rate, Blood Pressure, and many others are supported and included in the protocol stack.

Features

- 2.4GHz transceiver and Modem
  - -95dBm/-93dBm programmable receiver sensitivity
  - -20 to +3.5dBm programmable TX output power
  - Integrated T/R switch
  - Single wire antenna connection
- ARM® Cortex®-M0 32-bit processor
  - Single wire Debug (SWD) interface
  - 4-channel DMA controller
  - Brown-out detector and Power On Reset
  - Watchdog Timer
- Memory
  - 128kB embedded RAM (96kB available for application)
  - 128kB embedded ROM
  - 256kB Stacked Flash Memory
- Hardware Security Accelerators
  - AES-128
  - SHA-256
- Peripherals
  - 23 digital and 4 mixed-signal GPIOs with 96kΩ internal programmable pull-up or down resistors and retention capability, and 3 wake up GPIOs with 96kΩ internal pull-up resistor
  - 2x SPI Master/Slave
  - 2x I^2C Master/Slave and 1x I^2C Slave
  - 2x UART
  - Three-axis quadrature decoder
  - 4x Pulse Width Modulation (PWM), three General Purpose Timers, and one Wakeup Timer
  - 4-channel 11-bit ADC
- Clock
  - Integrated 26MHz RC oscillator

  - 26MHz crystal oscillator
  - Integrated 2MHz sleep RC oscillator
  - 32.768kHz RTC crystal oscillator
- Ultra Low Power
  - 1.1µA sleep current (8K RAM retention and RTC running)
  - 3.0mA peak TX current (0dBm, 3.6V)
  - 4.2mA peak RX current (3.6V, -93dBm sensitivity)
- Integrated Power Management
  - 2.3 to 4.3V battery voltage range
  - 2.3 to 3.6V input range for I/O (limited by Flash memory)
  - Fully integrated Buck DC/DC converter
- Bluetooth SIG Certification
  - The ATSAMB11 uses the ATBTLC1000 as its Bluetooth controller and is certified under the ATBTLC1000.
    - QD ID Controller (see declaration D028678)
    - QD ID Host (see declaration D028679)

Table of Contents

1 Ordering Information

Ordering Code	Package	Description
ATSAMB11G18A-MU-T	6x6mm QFN 48	SAMB11Tape & Reel
ATSAMB11G18A-MU-Y	6x6mm QFN 48	SAMB11 Tray

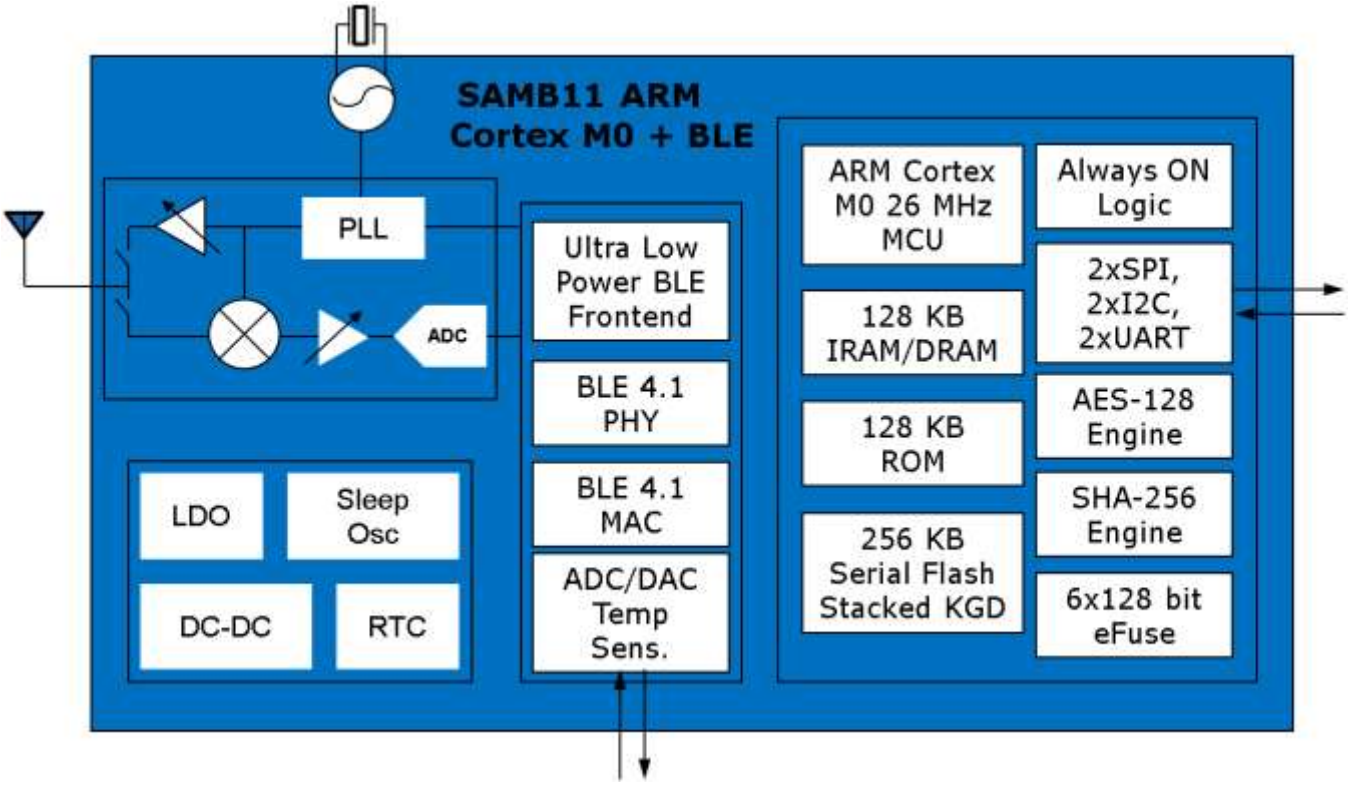
2 Package Information

Table 2-1. SAMB11 6x6 QFN 48 Package Information

Parameter	Value	Units	Tolerance
Package Size	6x6	mm	±0.1 mm
QFN Pad Count	48		
Total Thickness	0.85	mm	+0.15/-0.05mm
QFN Pad Pitch	0.4		
Pad Width	0.2		
Exposed Pad size	4.2x4.2		

3 Block Diagram

Figure 3-1. SAMB11 Block Diagram



4 Pinout Information

SAMB11 is offered in an exposed pad 48-pin QFN package. This package has an exposed paddle that must be connected to the system board ground. The QFN package pin assignment is shown in Figure 4-1. The color shading is used to indicate the pin type as follows:

- Red – analog
- Green – digital I/O (switchable power domain)
- Blue – digital I/O (always-on power domain)
- Yellow – digital I/O power
- Purple – PMU
- Shaded green/red – configurable mixed-signal GPIO (digital/analog)

The SAMB11 pins are described in Table 4-1.

Figure 4-1. SAMB11 Pin Assignment

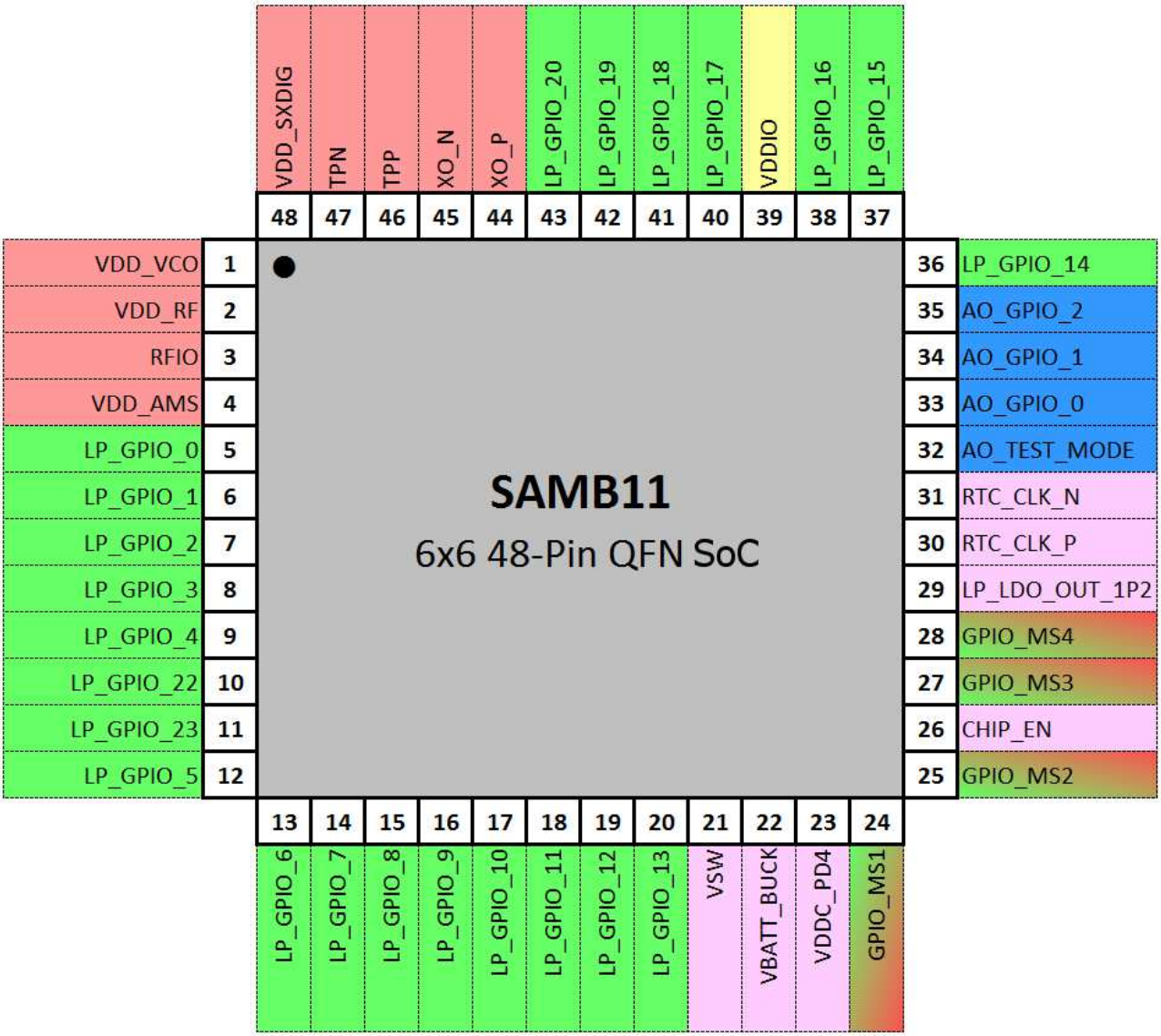


Table 4-1. SAMB11 Pin Description with Default Peripheral Mapping

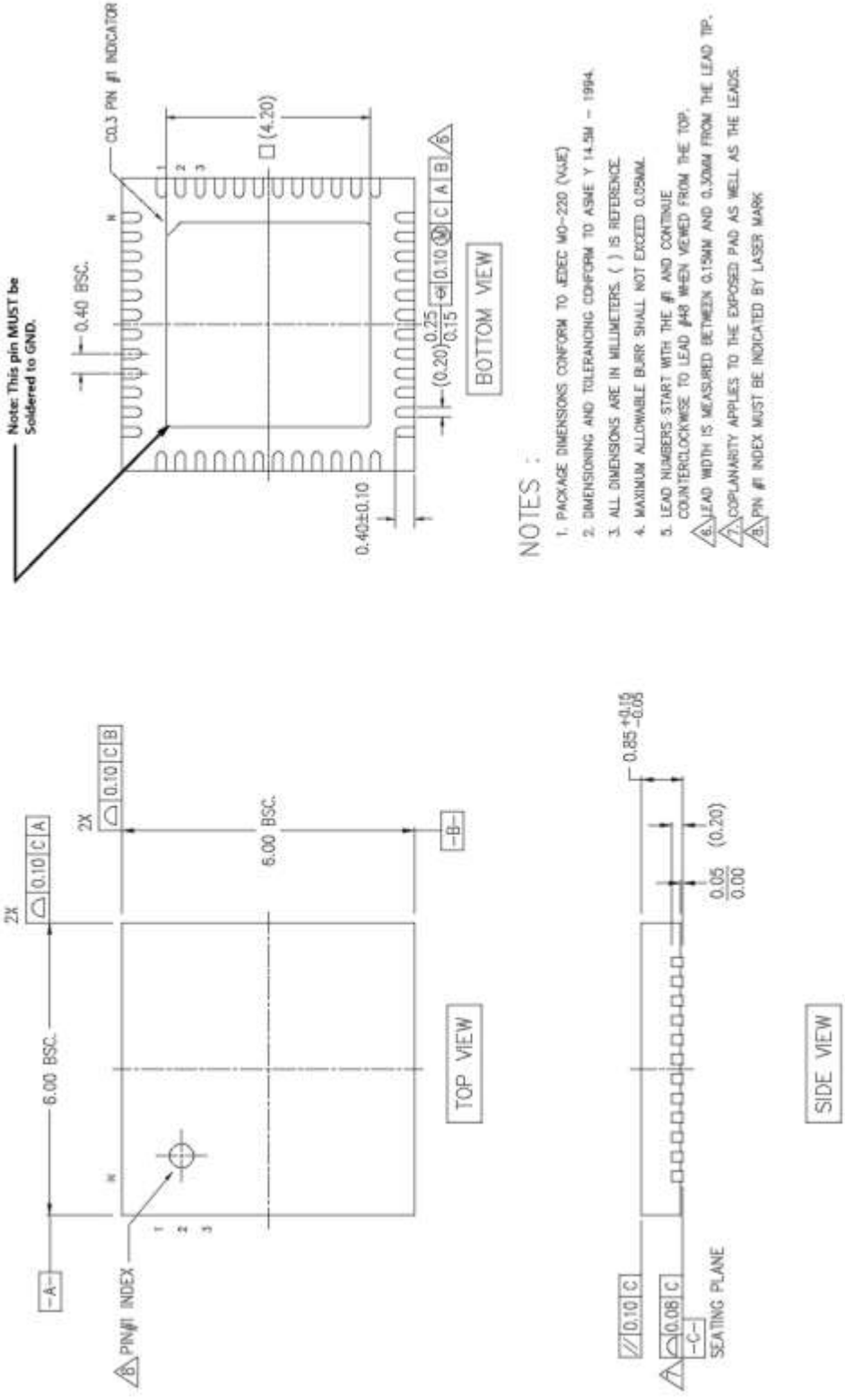
Pin #	Pin Name	Pin Type	Description / Default Function
1	VDD_VCO	Analog/RF	RF Supply 1.2V
2	VDD_RF	Analog/RF	RF Supply 1.2V
3	RFIO	Analog/RF	RX input and TX output
4	VDD_AMS	Analog/RF	AMS Supply 1.2V
5	LP_GPIO_0	Digital I/O, Programmable Pull-Up/Down	SWD Clock
6	LP_GPIO_1	Digital I/O, Programmable Pull-Up/Down	SWD I/O
7	LP_GPIO_2	Digital I/O, Programmable Pull-Up/Down	UART1 RXD
8	LP_GPIO_3	Digital I/O, Programmable Pull-Up/Down	UART1 TXD
9	LP_GPIO_4	Digital I/O, Programmable Pull-Up/Down	UART1 CTS
10	LP_GPIO_22	Digital I/O, Programmable Pull-Up/Down	GPIO
11	LP_GPIO_23	Digital I/O, Programmable Pull-Up/Down	GPIO
12	LP_GPIO_5	Digital I/O, Programmable Pull-Up/Down	UART1 RTS
13	LP_GPIO_6	Digital I/O, Programmable Pull-Up/Down	UART2 RXD
14	LP_GPIO_7	Digital I/O, Programmable Pull-Up/Down	UART2 TXD
15	LP_GPIO_8	Digital I/O, Programmable Pull-Up/Down	I2C0 SDA (high-drive pad, see Table 13-3)
16	LP_GPIO_9	Digital I/O, Programmable Pull-Up/Down	I2C0 SCL (high-drive pad, see Table 13-3)
17	LP_GPIO_10	Digital I/O, Programmable Pull-Up/Down	SPI0 SCK
18	LP_GPIO_11	Digital I/O, Programmable Pull-Up/Down	SPI0 MOSI
19	LP_GPIO_12	Digital I/O, Programmable Pull-Up/Down	SPI0 SSN
20	LP_GPIO_13	Digital I/O, Programmable Pull-Up/Down	SPI0 MISO
21	VSW	PMU	DC/DC Converter Switching Node
22	VBATT_BUCK	PMU	DC/DC Converter Supply and General Battery Connection
23	VDDC_PD4	PMU	DC/DC Converter 1.2V output and feedback node
24	GPIO_MS1	Mixed Signal I/O, Programmable Pull-Up/Down	Configurable to be a GPIO Mixed Signal only (ADC interface)

Pin #	Pin Name	Pin Type	Description / Default Function
25	GPIO_MS2	Mixed Signal I/O, Programmable Pull-Up/Down	Configurable to be a GPIO Mixed Signal only (ADC interface)
26	CHIP_EN	PMU	Master Enable for chip
27	GPIO_MS3	Mixed Signal I/O, Programmable Pull-Up/Down	Configurable to be a GPIO Mixed Signal only (ADC interface)
28	GPIO_MS4	Mixed Signal I/O, Programmable Pull-Up/Down	Configurable to be a GPIO Mixed Signal only (ADC interface)
29	LP_LDO_OUT_1P2	PMU	Low Power LDO output (connect to 1µF decoupling cap)
30	RTC_CLK_P	PMU	RTC terminal + / 32.768kHz XTAL +
31	RTC_CLK_N	PMU	RTC terminal - / 32.768kHz XTAL +
32	AO_TEST_MODE	Digital Input	Test Mode Selection (SCAN ATE) /GND for normal operation
33	AO_GPIO_0	Digital I/O, Programmable Pull-Up	Always On External Wakeup
34	AO_GPIO_1	Digital I/O, Programmable Pull-Up	Always On External Wakeup
35	AO_GPIO_2	Digital I/O, Programmable Pull-Up	Always On External Wakeup
36	LP_GPIO_14	Digital I/O, Programmable Pull-Up/Down	UART2 CTS
37	LP_GPIO_15	Digital I/O, Programmable Pull-Up/Down	UART2 RTS
38	LP_GPIO_16	Digital I/O, Programmable Pull-Up/Down	GPIO
39	VDDIO	I/O Power	I/O Supply can be less than or equal to VBATT_BUCK
40	LP_GPIO_17	Digital I/O, Programmable Pull-Up/Down	GPIO
41	LP_GPIO_18	Digital I/O, Programmable Pull-Up/Down	GPIO
42	LP_GPIO_19	Digital I/O, Programmable Pull-Up/Down	GPIO
43	LP_GPIO_20	Digital I/O, Programmable Pull-Up/Down	GPIO
44	XO_P	Analog/RF	XO Crystal +
45	XO_N	Analog/RF	XO Crystal -
46	TPP	Analog/RF	Test MUX + output
47	TPN	Analog/RF	Test MUX – output
48	VDD_SXDIG	Analog/RF	RF Supply 1.2V

5 Package drawing

The SAMB11 QFN package is RoHS/green compliant.

Figure 5-1. SAMB11 6x6 QFN 48 Package Outline Drawing



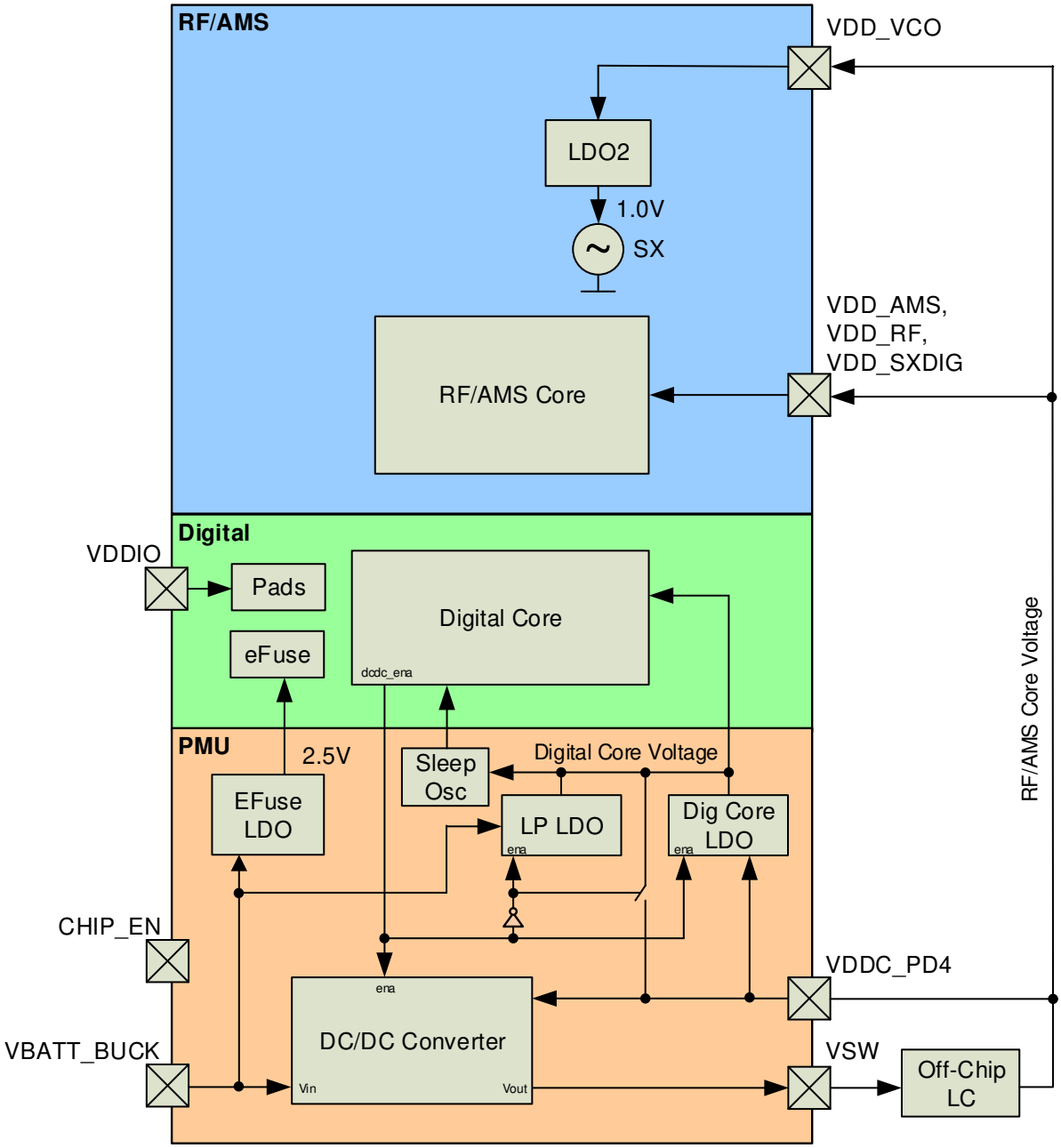
6 Power Management

6.1 Power Architecture

SAMB11 uses an innovative power architecture to eliminate the need for external regulators and reduce the number of off-chip components. The integrated power management block includes a DC/DC buck converter and separate Low Dropout (LDO) regulators for different power domains. The DCDC buck converter converts battery voltage to a lower internal voltage for the different circuit blocks and does this with high efficiency. The DCDC requires three external components for proper operation (two inductors L 4.7µH and 9.1nH, and one capacitor C 4.7µF).

The stacked Flash has a supply pin that is internally connected to the VDDIO pin.

Figure 6-1. SAMB11 Power Architecture



6.2 DC/DC Converter

The DC/DC Converter is intended to supply current to the BLE digital core and the RF transceiver core. The DC/DC consists of a power switch, 26MHz RC oscillator, controller, external inductor, and an external capacitor. The DCDC is utilizing pulse skipping discontinuous mode as its control scheme. The DC/DC specifications are shown in the following tables and charts.

Table 6-1. DC/DC Converter Specifications (performance is guaranteed for 4.7µF L and 4.7µF C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Output current capability	I_{REG}	0	10	30	mA	Dependent on external component values and DC/DC settings with acceptable efficiency
External capacitor range (1)	C_{EXT}	4.7 - 10%	4.7	20	µF	External capacitance range
External inductor range	L_{EXT}	2.2 - 10%	4.7	4.7 +10%	µH	External inductance range
Battery voltage	V_{BAT}	2.3	3.3	4.3	V	Functionality and stability given
Output voltage range	V_{REG}	1.05	1.2	1.47		25mV step size
Current consumption	I_{DD}		125		µA	DC/DC quiescent current
Startup time	$t_{startup}$	50		600	µs	Dependent on external component values and DC/DC settings
Voltage ripple	ΔV_{REG}	5	10	30	mV	Dependent on external component values and DC/DC settings
Efficiency	η		85		%	Measured at 3V VBATT, at load of 10mA
Overshoot at startup	V_{OS}		0		mV	No overshoot, no output pre-charge
Line Regulation	ΔV_{REG}		10			From 2.35 - 4.3V
Load regulation	ΔV_{REG}		5			From 0 - 10mA

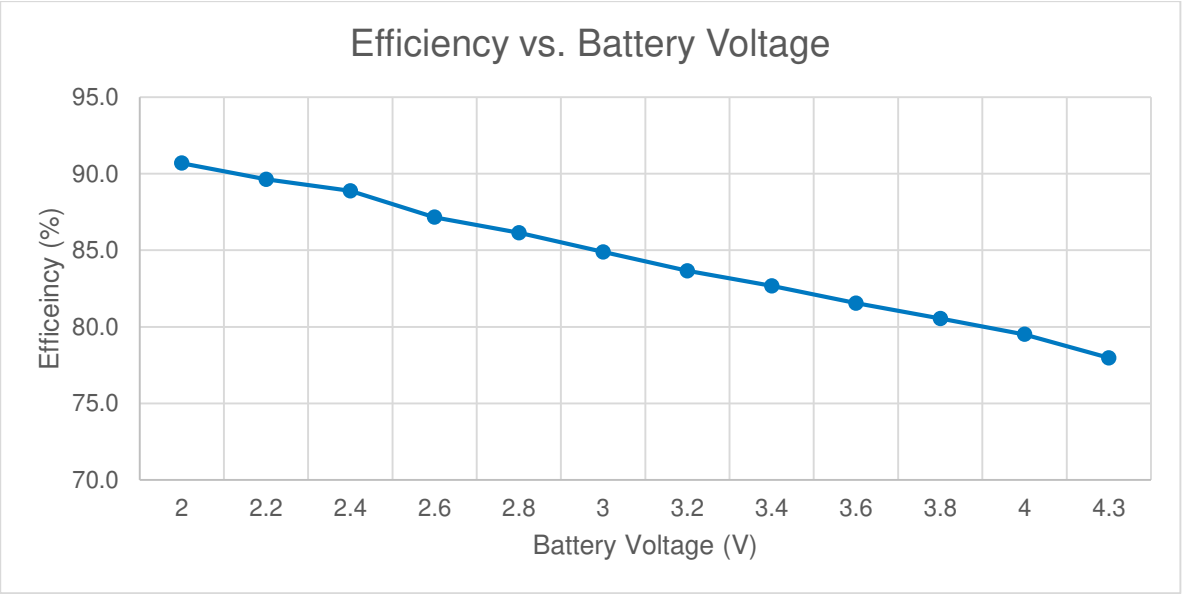
Note: 1. External Cap: Sum of all caps connected to the DC/DC output node.

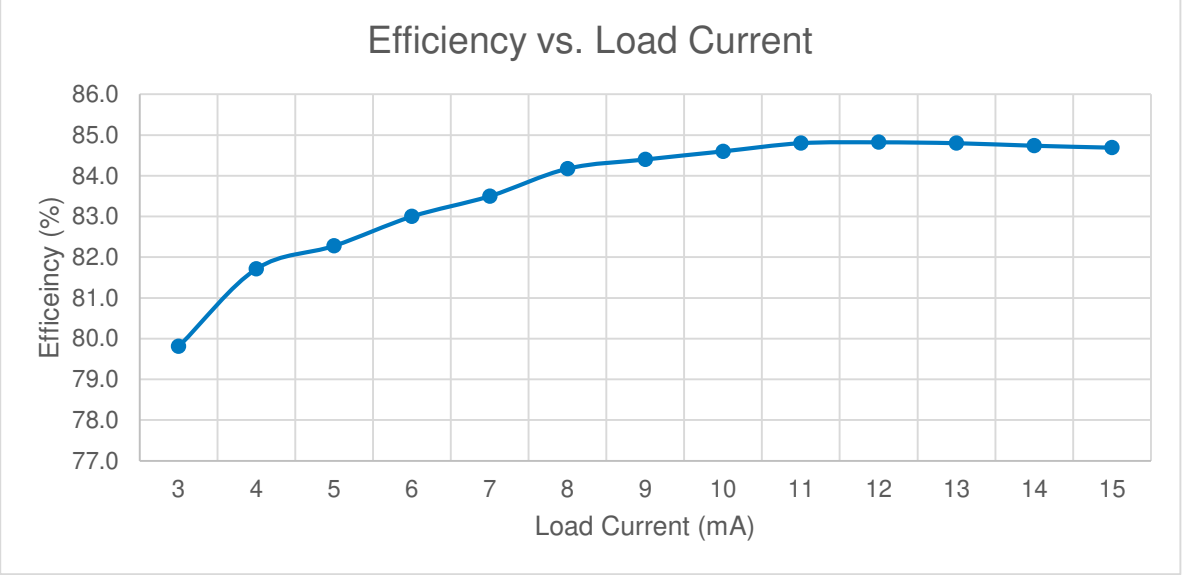
Table 6-2. DC/DC Converter Allowable Onboard Inductor and Capacitor Values (VBATT=3V)

Inductor [µH]	Efficiency [%]	Vripple [mV]			RX sensitivity (1) [dBm]
		C=2.2µF	C=4.7µF	C=10µF	
2.2	83	N/A	<5	<5	~1.5dB degrade
4.7	85	9	5	<5	~0.7dB degrade

Note: 1. Degradation relative to design powered by external LDO and DC/DC disabled.

Figure 6-2. DC/DC Converter Efficiency





6.3 Power Consumption

6.3.1 Description of Device States

SAMB11 has multiple device states, depending on the state of the ARM processor and BLE subsystem.

Note: The ARM is required to be powered ON if the BLE subsystem is active.

- BLE_On_Transmit – Device is actively transmitting a BLE signal (Application may or may not be active)
- BLE_On_Receive – Device is actively receiving a BLE signal (Application may or may not be active)
- MCU_Only – Device has ARM processor powered on and BLE subsystem powered down
- Ultra_Low_Power – BLE is powered down and Application is powered down (with or without RAM retention)
- Power_Down – Device core supply off

6.3.2 Controlling the Device States

The following pins are used to switch between the main device states:

- CHIP_EN – Used to enable PMU
- VDDIO – I/O supply voltage from external supply

In Power_Down state, VDDIO is on and CHIP_EN is low (at GND level). To switch between Power_Down state and MCU_Only state CHIP_EN has to change between low and high (VDDIO voltage level). Once the device is the MCU_Only state, all other state transitions are controlled entirely by software. When VDDIO is off and CHIP_EN is low, the chip is powered off with no leakage.

When no power is supplied to the device (the DC/DC Converter output and VDDIO are both off and at ground potential), a voltage cannot be applied to the SAMB11 pins because each pin contains an ESD diode from the pin to supply. This diode will turn on when a voltage higher than one diode-drop is supplied to the pin.

If a voltage must be applied to the signal pads while the chip is in a low power state, the VDDIO supply must be on, so the Power_Down state must be used. Similarly, to prevent the pin-to-ground diode from turning on, do not apply a voltage that is more than one diode-drop below ground to any pin.

6.3.3 Current Consumption in Various Device States

Table 6-3. SAMB11 Device Current Consumption

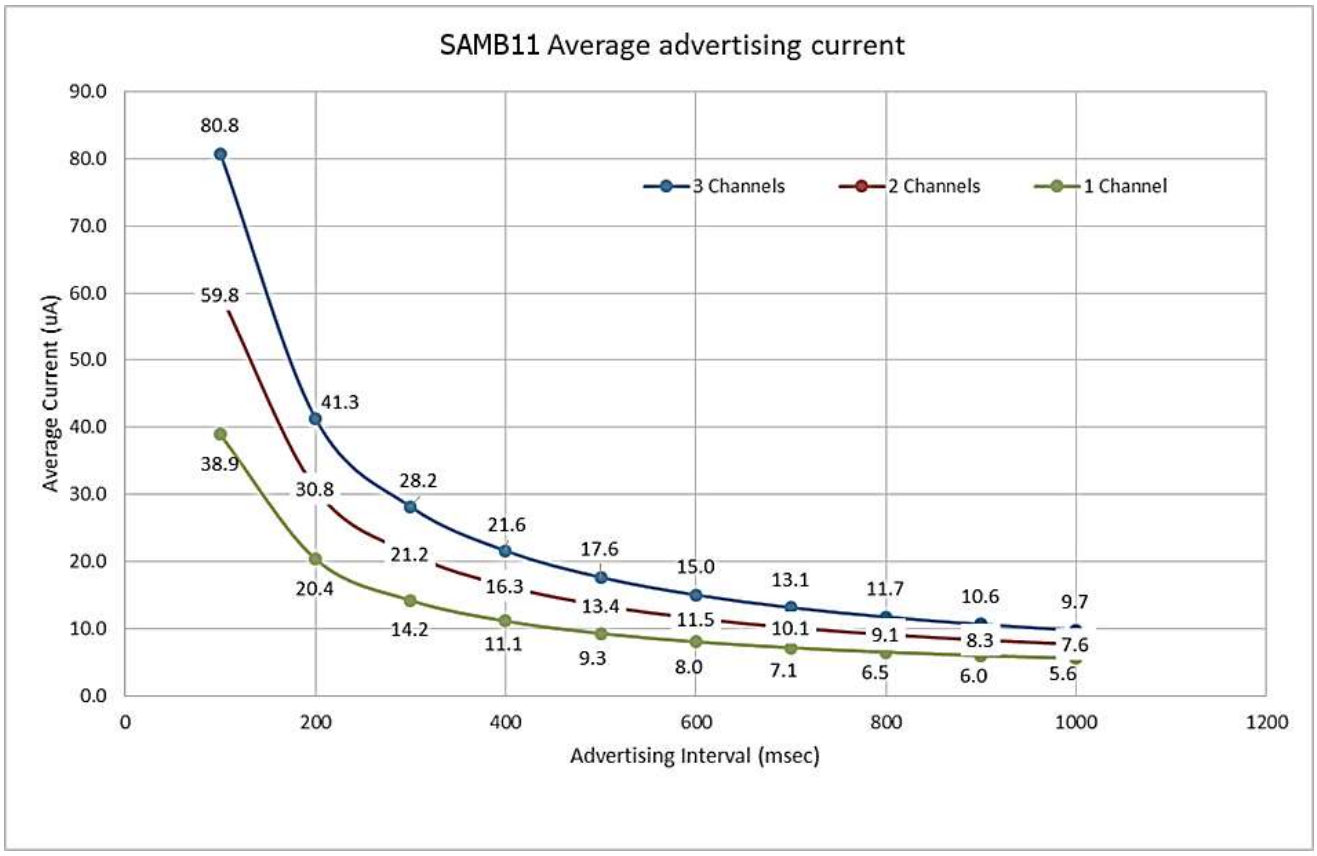
Device State	CHIP_EN	VDDIO	I_{VBATT} (typical)	I_{VDDIO} (typical)	Remark
Power_Down	Off	On	<50nA	<50nA	
Ultra_Low_Power Standby	On	On	900nA	50nA	
Ultra_Low_Power with 8KB retention, BLE timer, no RTC (1)	On	On	1.1µA	0.2µA	
Ultra_Low_Power with 8KB retention, BLE timer, with RTC (2)	On	On	1.25µA	0.1uA	
MCU_Only, idle (waiting for interrupt)	On	On	0.85mA	12µA	
BLE_On_Receive@-95dBm	On	On	4.5mA	12µA	
BLE_On_Transmit, 0dBm output power	On	On	3.0mA	12µA	
BLE_On_Transmit, 3.5dBm output power	On	On	4.0mA	12µA	

Notes: 1. Sleep clock derived from internal 32kHz RC oscillator.

2. Sleep clock derived from external 32.768kHz crystal specified for C_L=7pF, using the default on-chip capacitance only, without using external capacitance.

Note: The average advertising current for connectable beacon with a full payload (37-byte packet) is targeted to be 9.7µA. The average advertising current is based on automatic advertising from the ROM with RTC 32kHz, BLE sleep timers, and 8KB memory retention. IDRAM1 and IDRAM2 are OFF. External Peripherals and debug clocks are turned OFF. VBATT is set to 3.6V. This advertising current will be enabled in a future SDK release. For current SDK based advertising current, see errata Chapter 14.

Figure 6-3. SAMB11 Average Advertising Current



6.4 Power-up Sequence

The power-up sequence for SAMB11 is shown in Figure 6-4. The timing parameters are provided in Table 6-4.

Figure 6-4. SAMB11 Power-up Sequence

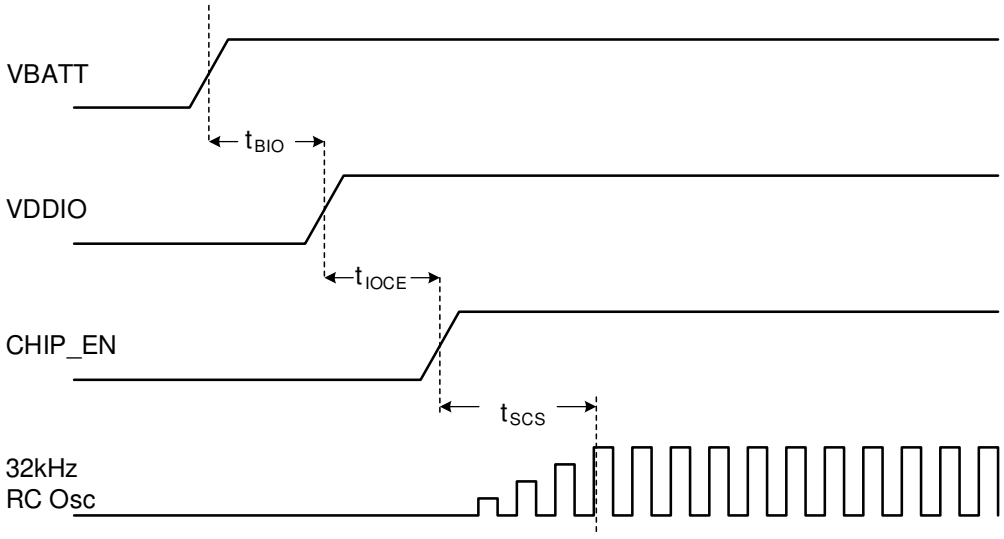


Table 6-4. SAMB11 Power-up Sequence Timing

Parameter	Min.	Max.	Units	Description	Notes
t_{BIO}	0		ms	VBATT rise to VDDIO rise	VBATT and VDDIO can rise simultaneously or can be tied together.
t_{IOCE}	0			VDDIO rise to CHIP_EN rise	CHIP_EN must not rise before VDDIO. CHIP_EN must be driven high or low, not left floating.
t_{SCS}	10		µs	CHIP_EN rise to 31.25kHz (2MHz/64) oscillator stabilizing	

6.5 Power On Reset (POR) and Brown Out Detector (BOD)

The SAMB11 has a POR circuit for proper system power bring up and a brown-out detector to reset the system's operation when a drop in battery voltage is detected.

- POR is a power on reset circuit that outputs a HI logic value when the VBATT_BUCK is below a voltage threshold. The POR output becomes a LO logic value when the VBATT_BUCK is above a voltage threshold.
- BOD is a brown out detector that outputs a HI logic value when the bandgap reference (BGR) voltage falls below a programmable voltage threshold. When the bandgap voltage reference voltage level is restored above a voltage threshold, the BOD output becomes a LO logic value.
- The counter creates a pulse that is HI for 256*(64*T_2MHz) ~8.2ms

The system block diagram and timing are illustrated in Figure 6-5 and Figure 6-6.

Table 6-5 shows the BOD thresholds.

Figure 6-5. SAMB11 POR and BOD Block Diagram

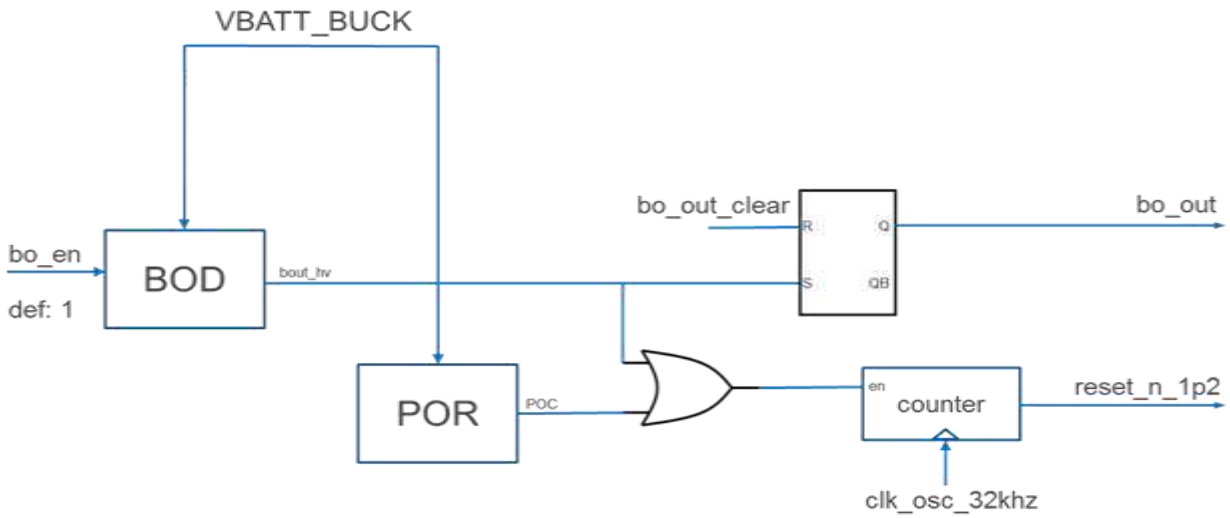


Figure 6-6. SAMB11 POR and BOD Timing Sequence

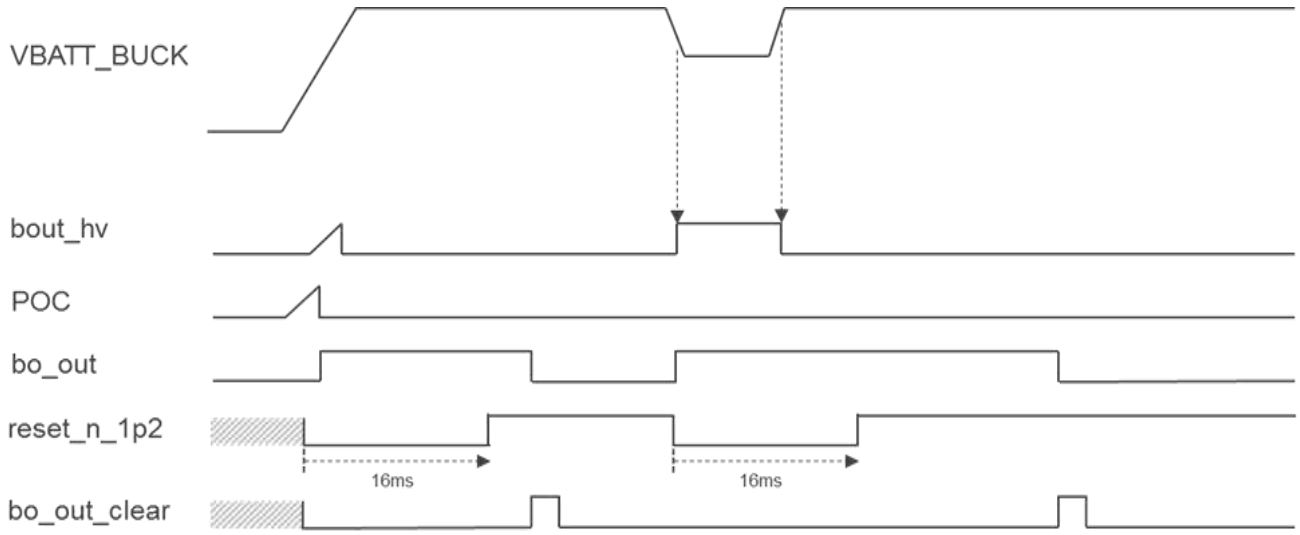


Table 6-5. ATBTLC1000 BOD Thresholds

Parameter	Min.	Typ.	Max.	Comment
BOD threshold	1.73V	1.80V	1.92V	
BOD threshold temperature coefficient		-1.09mV/C		
BOD current consumption		300nA		
t_{POR}		8.2ms		

6.6 Digital and Mixed-Signal I/O Pin Behavior during Power-Up Sequences

The following table represents I/O pin states corresponding to device power modes.

Table 6-6. I/O Pin Behavior in Different Device States[1]

Device State	VDDIO	CHIP_EN	Output Driver	Input Driver	Pull Up/Down Resistor [2]
Power_Down: core supply off	High	Low	Disabled (Hi-Z)	Disabled	Disabled
Power-On Reset: core supply on, POR hard reset pulse on	High	High	Disabled (Hi-Z)	Disabled	Disabled[3]
Power-On Default: core supply on, device out of reset but not programmed yet	High	High	Disabled (Hi-Z)	Enabled[4]	Enabled Pull-Up[4]
MCU_Only, BLE_On: core supply on, device programmed by firmware	High	High	Programmed by firmware for each pin: Enabled or Disabled (Hi-Z)[5], when Enabled driving 0 or 1	Opposite of Output Driver state: Disabled or Enabled[5]	Programmed by firmware for each pin: Enabled or Disabled, Pull-Up or Pull-Down[5]

Device State	VDDIO	CHIP_EN	Output Driver	Input Driver	Pull Up/Down Resistor [2]
Ultra_Low_Power: core supply on for always-on domain, core supply off for switchable domains	High	High	Retains previous state[6] for each pin: Enabled or Disabled (Hi-Z), when Enabled driving 0 or 1	Opposite of Output Driver state: Disabled or Enabled[5]	Retains the previous state[6] for each pin: Enabled or Disabled, Pull-Up or Pull-Down

Notes:
1. This table applies to all three types of I/O pins (digital switchable domain GPIOs, digital always-on/wakeup GPIOs, and mixed-signal GPIOs) unless otherwise noted
2. Pull-up/down resistor value is 96kΩ ±10%
3. In Power-On Reset state pull-up resistor is enabled in the always-on/wakeup GPIOs only
4. In Power-On Default state input drivers and pull-up/down resistors are disabled in the mixed-signal GPIOs only (mixed-signal GPIOs are defaulted to analog mode, see the note below)
5. Mixed-signal GPIOs can be programmed to be in analog or digital mode for each pin: when programmed to analog mode (default), the output driver, input driver, and pull-up/down resistors are all disabled
6. In Ultra_Low_Power state always-on/wakeup GPIOs do not have retention capability and behave same as in MCU_Only or BLE_On states, also for mixed-signal GPIOs programming analog mode overrides retention functionality for each pin

7 Clocking

7.1 Overview

Figure 7-1. SAMB11 Clock Architecture

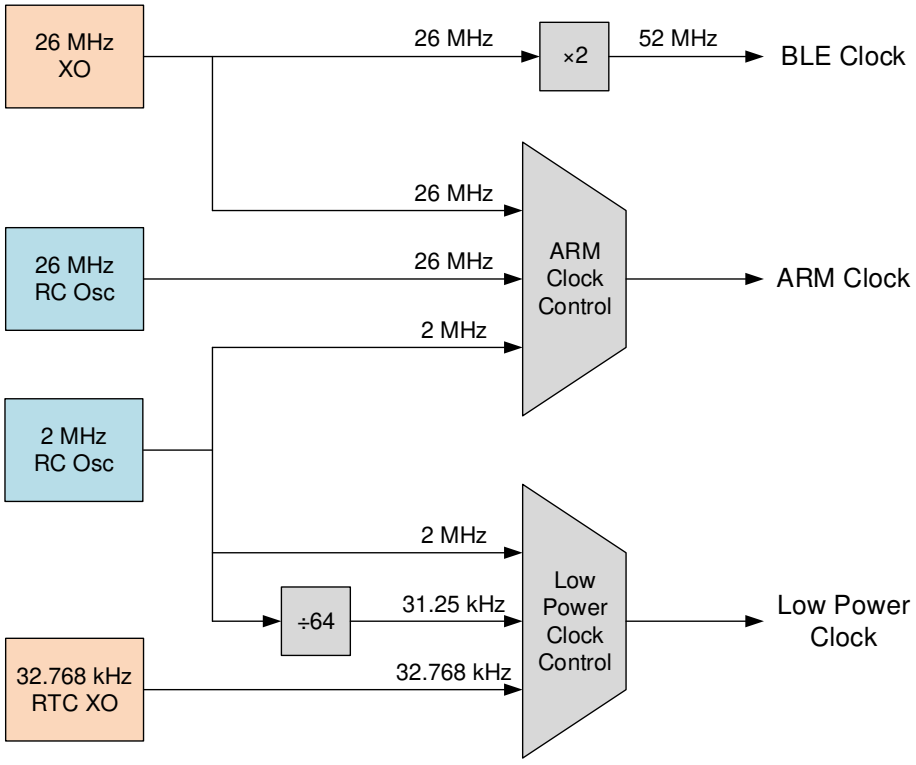


Figure 7-1 provides an overview of the clock tree and clock management blocks.

The BLE Clock is used to drive the BLE subsystem. The ARM clock is used to drive the Cortex-M0 MCU and its interfaces (UART, SPI, and I²C), the nominal MCU clock speed is 26MHz. The Low Power Clock is used to drive all the low power applications like the BLE sleep timer, always-on power sequencer, always-on timer, and others.

The 26MHz Crystal Oscillator (XO) must be used for the BLE operations or in the event a very accurate clock is required for the ARM subsystem operations.

The 26MHz integrated RC Oscillator is used for most general purpose operations on the MCU and its peripherals. In cases when the BLE subsystem is not used, the RC oscillator can be used for lower power consumption. The frequency variation of this RC oscillator is up to ±50% over process, voltage, and temperature.

The 2MHz integrated RC Oscillator can be used as the Low Power Clock for applications that require a fast wake up of the ARM or for generating a ~31.25 kHz clock for a slower wake up but lowest power in sleep mode. This 2MHz oscillator can also be used as the ARM Clock for low-power applications where the MCU needs to remain on but run at a reduced clock speed. The frequency variation of this RC oscillator is up to ±50% over process, voltage, and temperature.

The 32.768kHz RTC Crystal Oscillator (RTC XO) is recommended to be used for BLE operations (although optional) as it will reduce power consumption by providing the best timing for wake up precision, allowing circuits to be in low power sleep mode for as long as possible until they need to wake up and connect during the BLE connection event. The ~31.25kHz clock derived from the 2MHz integrated RC Oscillator can be used instead of RTC XO but it has low accuracy over process, voltage and temperature variations (up to ±50%) and thus needs to

be frequently calibrated to within ±500ppm if the RC oscillator is used for BLE timing during a connection event. Because this clock is less accurate than RTC XO, it will require waking up earlier to prepare for a connection event and this will increase the average power consumption. Calibration of the RC Oscillator is described in the application note.

7.2 26MHz Crystal Oscillator (XO)

Table 7-1. SAMB11 26MHz Crystal Oscillator Parameters

Parameter	Min.	Typ.	Max.	Units
Crystal Resonant Frequency	N/A	26	N/A	MHz
Crystal Equivalent Series Resistance		50	80	Ω
Stability - Initial Offset (1)	-50		50	ppm
Stability - Temperature and Aging	-40		40	ppm

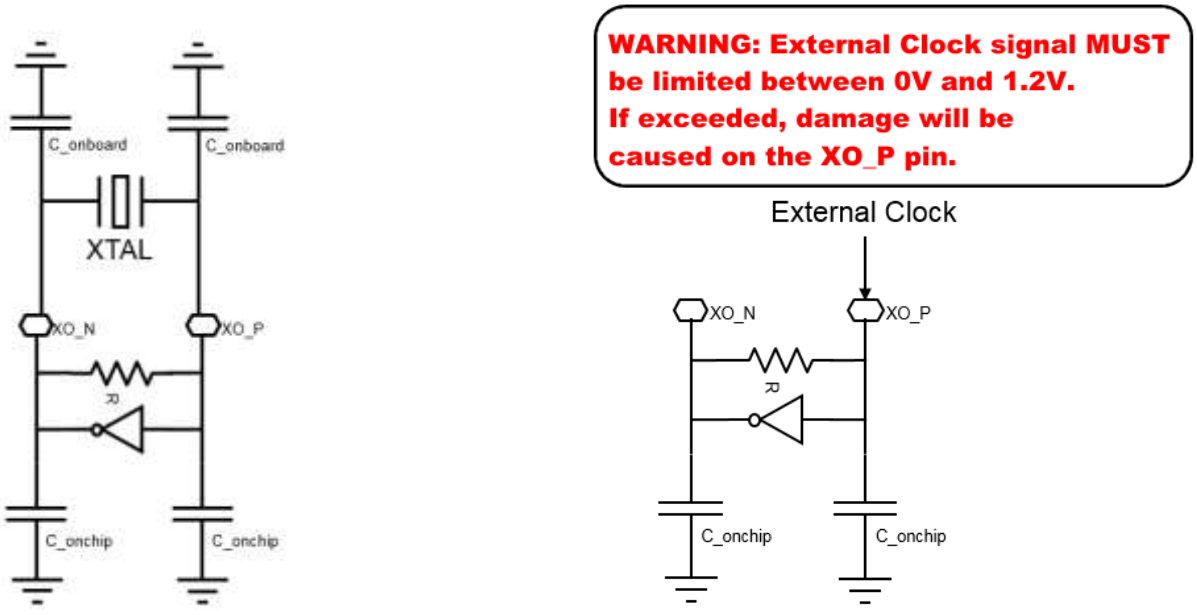
Note: 1. The initial offset must be calibrated to maintain ±25ppm in all operating conditions. This calibration is performed during final production testing and calibration offset values are stored in eFuse. More details are provided in the calibration application note.

The block diagram in Figure 7-2(a) shows how the internal Crystal Oscillator (XO) is connected to the external crystal.

The XO has up to 10pF internal capacitance on each terminal XO_P and XO_N (programmable in steps of 1.25pF). To bypass the crystal oscillator, an external Signal capable of driving 10pF can be applied to the XO_P terminal as shown in Figure 7-2(b).

The needed external bypass capacitors depend on the chosen crystal characteristics. Refer to the datasheet of the preferred crystal and take into account the on-chip capacitance.
When bypassing XO_P from an external clock, XO_N is required to be floating.

Figure 7-2. SAMB11 Connections to XO



(a) Crystal oscillator is used

(b) Crystal oscillator is bypassed

Table 7-2. SAMB11 26MHz XTAL C_onchip Programming

xo_cap[3:0]	40020808[17]	40020848[17]	40020814[7,6,15]	Cl,on-chip [pF]
0	0	0	000	1.00
1	0	0	001	2.25
2	0	0	010	3.50
3	0	0	011	4.75
4	0	0	100	**6.00**
5	0	0	101	7.25
6	0	0	110	8.50
7	0	0	111	9.75
8	1	1	000	6.00
9	1	1	001	7.25
10	1	1	010	8.50
11	1	1	011	9.75
12	1	1	100	11.00
13	1	1	101	12.25
14	1	1	110	13.50
15	1	1	111	14.75

Table 7-3 specifies the electrical and performance requirements for the external clock.

Table 7-3. SAMB11 Bypass Clock Specification

Parameter	Min.	Max.	Unit	Comments
Oscillation frequency	26	26	MHz	Must be able to drive 5pF load @ desired frequency
Voltage swing	0.75	1.2	Vpp	
Stability – Temperature and Aging	-50	+50	ppm	BLE Spec has +-50ppm Frequency accuracy requirement.
Phase Noise		-130	dBc/Hz	At 10kHz offset
Jitter (RMS)		<1psec		Based on integrated phase noise spectrum from 1kHz to 1MHz

7.3 32.768kHz RTC Crystal Oscillator (RTC XO)

7.3.1 General Information

SAMB11 has a 32.768kHz RTC oscillator that is preferably used for BLE activities involving connection events. To be compliant with the BLE specifications for connection events, the frequency accuracy of this clock has to be within ±500ppm. Because of the high accuracy of the 32.768kHz crystal oscillator clock, the power consumption can be minimized by leaving radio circuits in low-power sleep mode for as long as possible until they need to wake up for the next connection timed event.

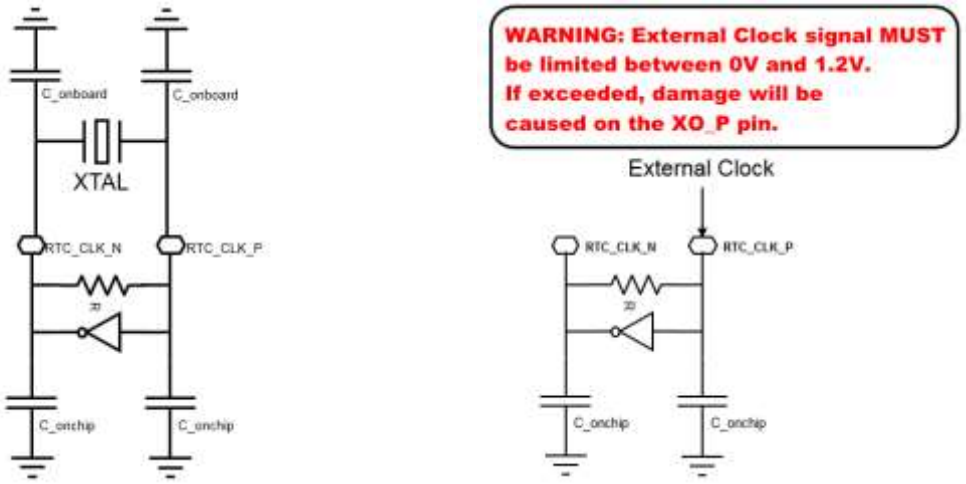
The block diagram in Figure 7-3(a) shows how the internal low-frequency Crystal Oscillator (XO) is connected to the external crystal.

The RTC XO has a programmable internal capacitance with a maximum of 15pF on each terminal, RTC_CLK_P, and RTC_CLK_N. When bypassing the crystal oscillator with an external signal, one can program down the internal capacitance to its minimum value (~1pF) for easier driving capability. The driving signal can be applied to the RTC_CLK_P terminal as shown in Figure 7-3(b).

The needed external bypass capacitors depend on the chosen crystal characteristics. Refer to the datasheet of the preferred crystal and take into account the on-chip capacitance.

When bypassing RTC_CLK_P from an external clock, RTC_CLK_N is required to be floating.

Figure 7-3. SAMB11 Connections to RTC XO



(a) Crystal oscillator is used

(b) Crystal oscillator is bypassed

Table 7-4. 32.768kHz XTAL C_onchip Programming

Register: pierce_cap_ctrl[3:0]	Cl_onchip [pF]
0000	0.0
0001	1.0
0010	2.0
0011	3.0
0100	4.0
0101	5.0
0110	6.0
0111	7.0
1000	8.0
1001	9.0
1010	10.0
1011	11.0
1100	12.0
1101	13.0
1110	14.0
1111	15.0

7.3.2 RTC XO Design and Interface Specification

The RTC consists of two main blocks: The Programmable Gm stage and tuning capacitors. The programmable Gm stage is used to guarantee oscillation startup and to sustain oscillation. Tuning capacitors are used to adjust the XO center frequency and control the XO precision for different crystal models. The output of the XO is driven to the digital domain via a digital buffer stage with a supply voltage of 1.2V.

Table 7-5. RTC XO Interface

Pin Name	Function	Register Default
Digital Control Pins		
Pierce_res_ctrl	Control feedback resistance value: 0 = 20MΩ Feedback resistance 1 = 30MΩ Feedback resistance	0X4000F404<15>='1'
Pierce_cap_ctrl<3:0>	Control the internal tuning capacitors with step of 700fF: 0000=700fF 1111=11.2pF Refer to crystal datasheet to check for optimum tuning cap value	0X4000F404<23:20>="1000"
Pierce_gm_ctrl<3:0>	Controls the Gm stage gain for different crystal mode: 0011= for crystal with shunt cap of 1.2pF 1000= for crystal with shunt cap >3pF	0X4000F404<19:16>="1000"
Supply Pins		
VDD_XO	1.2V	

7.3.3 RTC Characterization with Gm Code Variation at Supply 1.2V and Temp. = 25°C

This section shows the RTC total drawn current and the XO accuracy versus different tuning capacitors and different GM codes, at supply voltage of 1.2V and temp. = 25°C.

Figure 7-4. RTC Drawn Current vs. Tuning Caps at 25°C

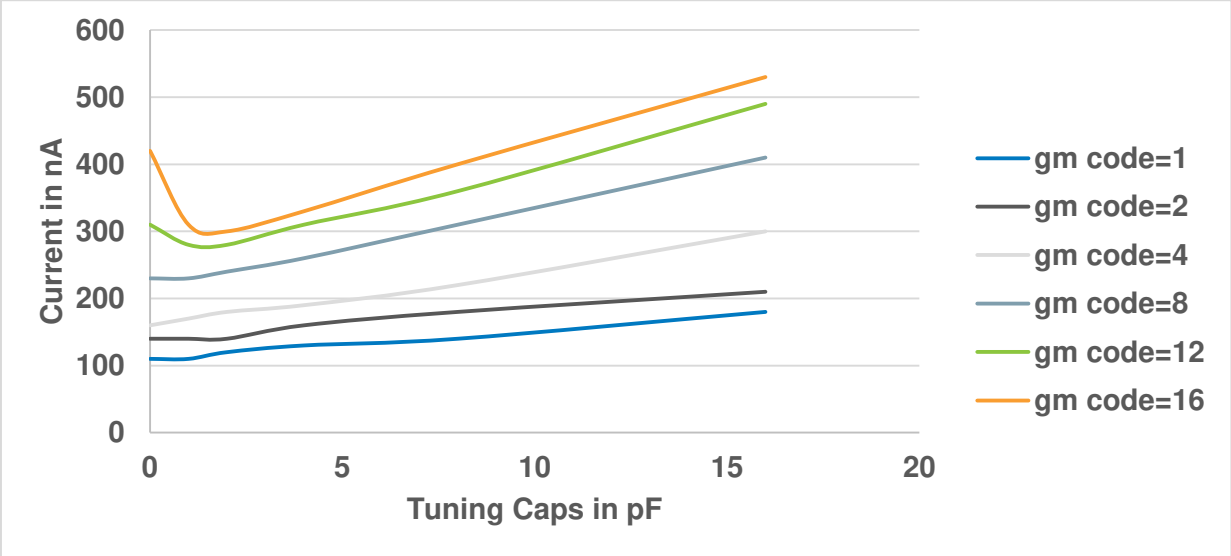
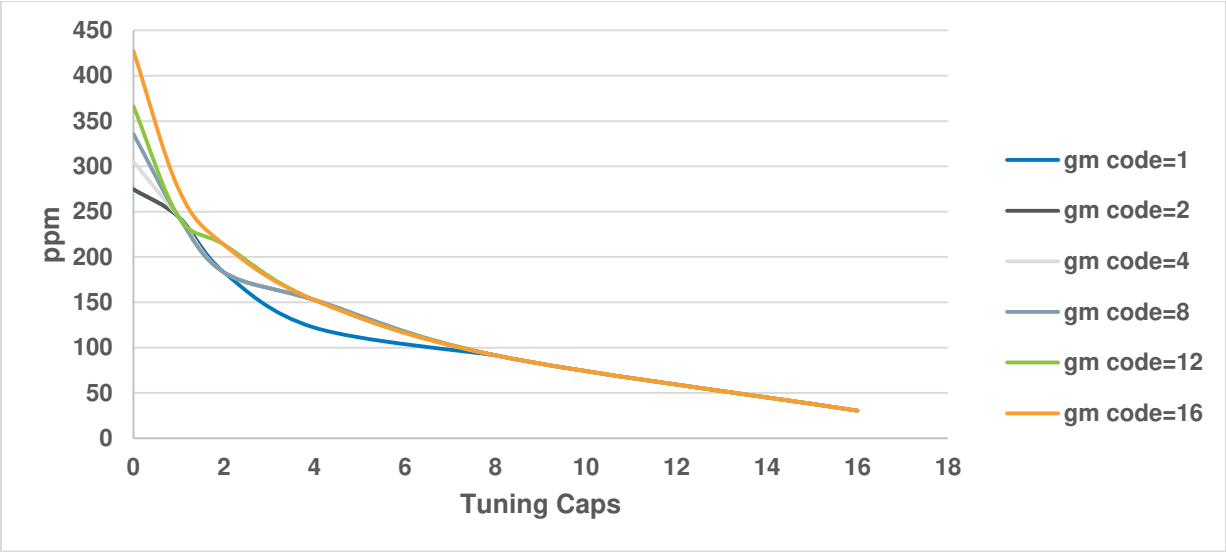


Figure 7-5. RTC Oscillation Frequency Deviation vs. Tuning Caps at 25°C



7.3.4 RTC Characterization with Supply Variation and Temp. = 25°C

Figure 7-6. RTC Drawn Current vs. Supply Variation

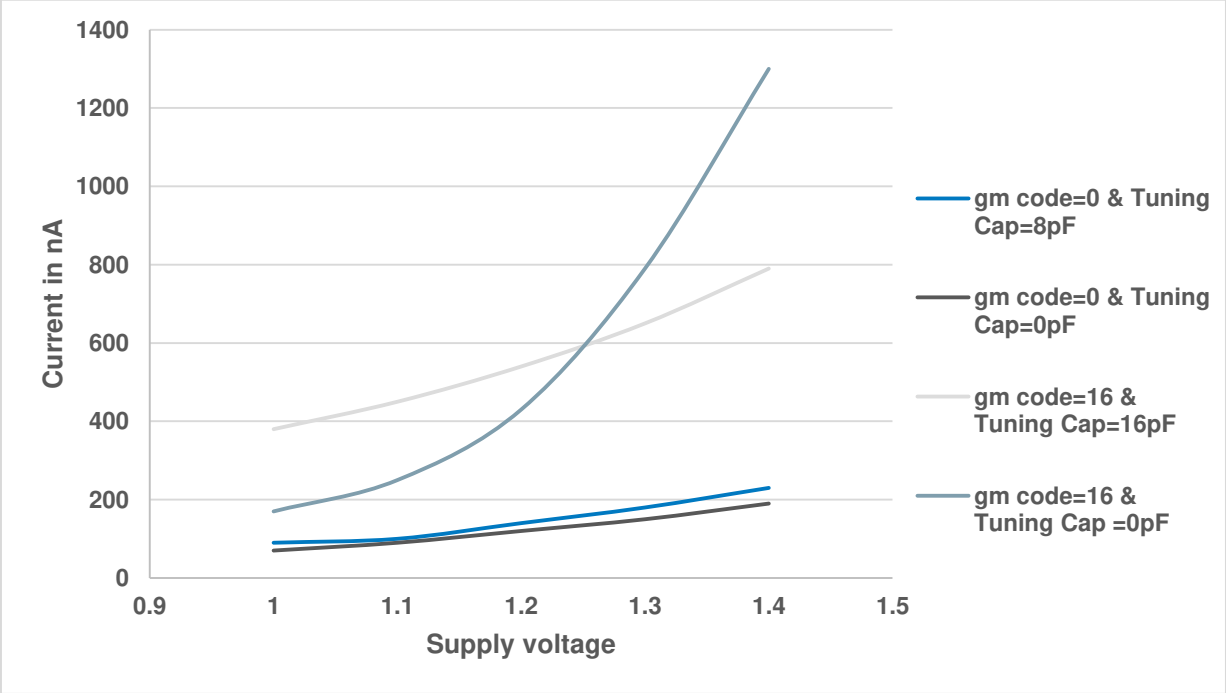
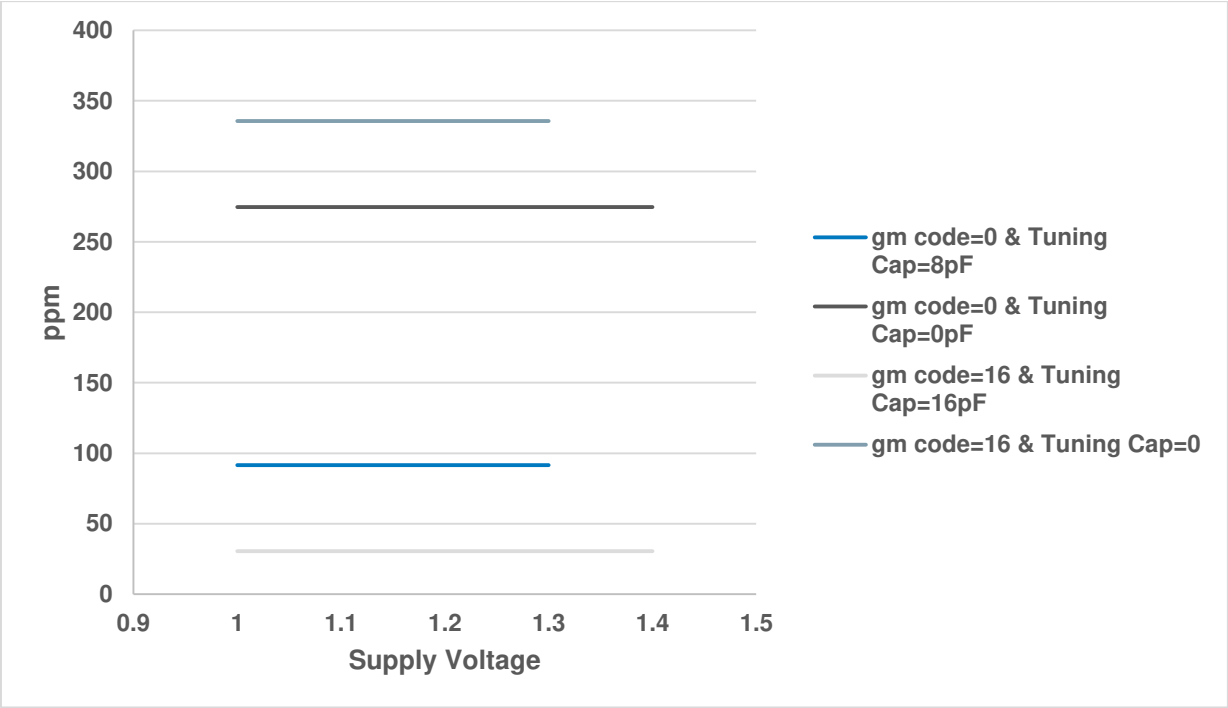


Figure 7-7. RTC Frequency Deviation vs. Supply Voltage



7.4 2MHz and 26MHz Integrated RC Oscillator

The 2MHz integrated RC Oscillator circuit without calibration has a frequency variation of 50% over process, temperature, and voltage variation. The ~31.25kHz clock is derived from the 2MHz clock by dividing by 64 and provides for lowest sleep power mode with a real-time clock running. As described above, calibration over process, temperature, and voltage is required to maintain the accuracy of this clock.

Figure 7-8. 32kHz RC Oscillator PPM Variation vs. Calibration Time at Room Temperature