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Introduction

The Atmel® | SMART™ SAM C20 is a series of microcontrollers optimized for industrial automation, appliances and other 5V applications using the 32-bit ARM® Cortex®-M0+ processor, ranging from 32- to 64-pins with up to 256KB Flash and 32KB of SRAM and operate at a maximum frequency of 48MHz and reach 2.46 CoreMark®/MHz. The SAM C20 devices are designed for simple and intuitive migration with identical peripheral modules, hex compatible code, identical linear address map and pin compatible migration paths between all devices in the product series. All devices include intelligent and flexible peripherals, Atmel Event System for inter-peripheral signaling, and support for capacitive touch button, slider and wheel user interfaces.

SAM C20 devices are pin compatible to the SAM D and SAM C family of general purpose microcontrollers.

Features

- Processor
 - ARM Cortex-M0+ CPU running at up to 48MHz
 - Single-cycle hardware multiplier
 - Micro Trace Buffer
 - Memory Protection Unit (MPU)
- Memories
 - 32/64/128/256KB in-system self-programmable Flash
 - 1/2/4/8KB independent self-programmable Flash for EEPROM emulation
 - 4/8/16/32KB SRAM Main Memory
- System
 - Power-on reset (POR) and brown-out detection (BOD)
 - Internal and external clock options with 48MHz to 96MHz Fractional Digital Phase Locked Loop (FDPLL96M)
 - External Interrupt Controller (EIC)
 - 16 external interrupts
 - One non-maskable interrupt

- Two-pin Serial Wire Debug (SWD) programming, test and debugging interface
- Low Power
 - Idle, standby, and off sleep modes
 - SleepWalking peripherals
- Peripherals
 - Hardware Divide and Square Root Accelerator (DIVAS)
 - 6-channel Direct Memory Access Controller (DMAC)
 - 6-channel Event System
 - Up to five 16-bit Timer/Counters (TC), configurable as either:
 - One 16-bit TC with compare/capture channels
 - One 8-bit TC with compare/capture channels
 - One 32-bit TC with compare/capture channels, by using two TCs
 - One 24-bit Timer/Counter for Control (TCC), with extended functions:
 - Up to four compare channels with optional complementary output
 - Generation of synchronized pulse width modulation (PWM) pattern across port pins
 - Deterministic fault protection, fast decay and configurable dead-time between complementary output
 - Dithering that increase resolution with up to 5 bit and reduce quantization error
 - Frequency Meter
 - 32-bit Real Time Counter (RTC) with clock/calendar function
 - Watchdog Timer (WDT)
 - CRC-32 generator
 - Up to four Serial Communication Interfaces (SERCOM), each configurable to operate as either:
 - USART with full-duplex and single-wire half-duplex configuration
 - I²C up to 3.4MHz
 - SPI
 - LIN master/slave
 - RS-485
 - One Configurable Custom Logic (CCL)
 - One 12-bit, 1Msps Analog-to-Digital Converter (ADC) with up to 12 channels
 - Differential and single-ended input
 - Automatic offset and gain error compensation
 - Oversampling and decimation in hardware to support 13-, 14-, 15- or 16-bit resolution
 - Two Analog Comparators (AC) with window compare function
 - Peripheral Touch Controller (PTC)
 - 256-Channel capacitive touch and proximity sensing
- I/O
 - Up to 52 programmable I/O pins
- Drop in compatible with SAM D20 and SAM D21
- Packages
 - 64-pin TQFP, QFN
 - 56-pin WLCSP
 - 48-pin TQFP, QFN

- 32-pin TQFP, QFN
- Operating Voltage
 - 2.7V – 5.5V

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1. Description

The Atmel SAM C20 devices provide the following features: In-system programmable Flash, six-channel direct memory access (DMA) controller, six-channel Event System, programmable interrupt controller, up to 52 programmable I/O pins, 32-bit real-time clock and calendar, up to five 16-bit Timer/Counters (TC) and three Timer/Counters for Control (TCC), where each TC can be configured to perform frequency and waveform generation, accurate program execution timing or input capture with time and frequency measurement of digital signals. The TCs can operate in 8- or 16-bit mode, selected TCs can be cascaded to form a 32-bit TC, and three timer/counters have extended functions optimized for motor, lighting and other control applications. Two TCC can operate in 24-bit mode, and the third TCC can operate in 16-bit mode. The series provide up to four Serial Communication Modules (SERCOM) that each can be configured to act as an USART, UART, SPI, I²C up to 3.4MHz, SMBus, RS-485 and LIN master/slave; one 12-bit, 1Msps ADC with up to 12-channels, two analog comparators with window mode, Peripheral Touch Controller supporting up to 256 buttons, sliders, wheels and proximity sensing; programmable Watchdog Timer, brown-out detector and power-on reset and two-pin Serial Wire Debug (SWD) program and debug interface.

All devices have accurate and low-power external and internal oscillators. All oscillators can be used as a source for the system clock. Different clock domains can be independently configured to run at different frequencies, enabling power saving by running each peripheral at its optimal clock frequency, and thus maintaining a high CPU frequency while reducing power consumption.

The SAM C20 devices have three software-selectable sleep modes, idle, standby and off. In idle mode the CPU is stopped while all other functions can be kept running. In standby all clocks and functions are stopped except those selected to continue running. In this mode all RAMs and logic contents are retained. The device supports SleepWalking. This feature allows the peripheral to wake up from sleep based on predefined conditions, and thus allows some internal operation like DMA transfer and/or the CPU to wake up only when needed, e.g. when a threshold is crossed or a result is ready. The Event System supports synchronous and asynchronous events, allowing peripherals to receive, react to and send events even in standby mode.

The Flash program memory can be reprogrammed in-system through the SWD interface. The same interface can be used for non-intrusive on-chip debug of application code. A boot loader running in the device can use any communication interface to download and upgrade the application program in the Flash memory.

The Atmel SAM C20 devices are supported with a full suite of program and system development tools, including C compilers, macro assemblers, program debugger/simulators, programmers and evaluation kits.

2. Configuration Summary

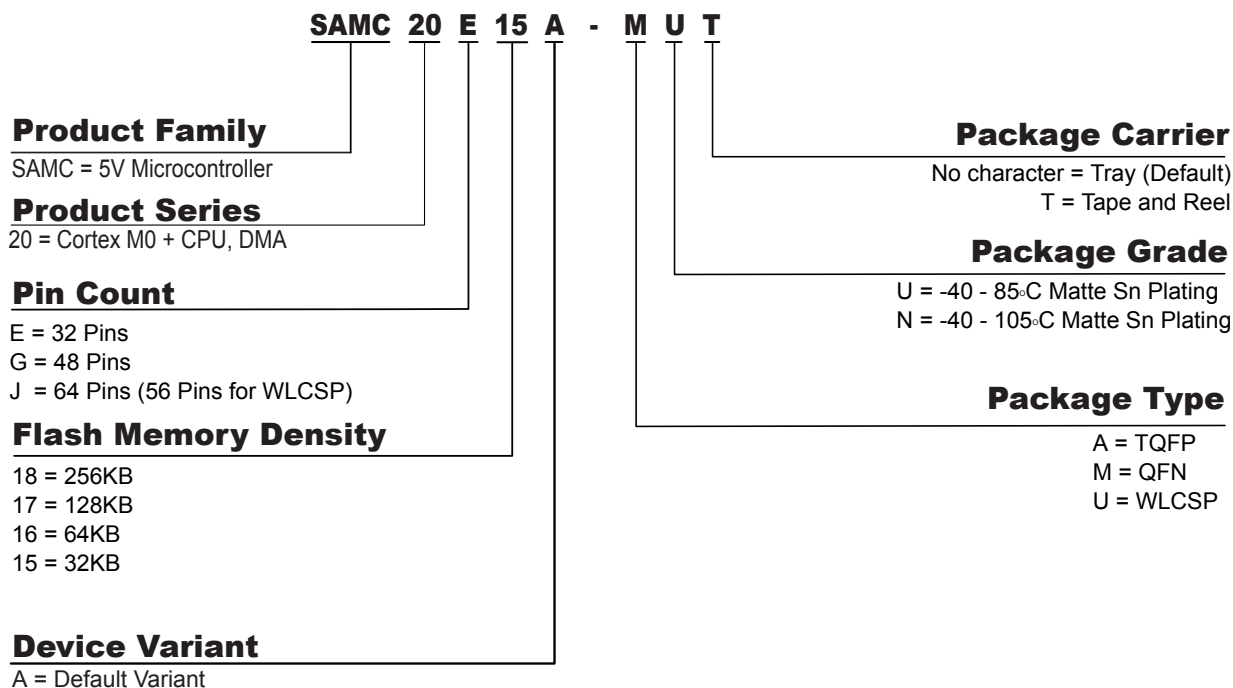
	SAM C20J	SAM C20G	SAM C20E
Pins	64 (56 for WLCSP)	48	32
General Purpose I/O-pins (GPIOs)	52	38	26
Flash	256/128/64/32KB	256/128/64/32KB	256/128/64/32KB
Flash RWW section	8/4/2/1KB	8/4/2/1KB	8/4/2/1KB
System SRAM	32/16/8/4KB	32/16/8/4KB	32/16/8/4KB
Timer Counter (TC) instances	5	5	5
Waveform output channels per TC instance	2	2	2
Timer Counter for Control (TCC) instances	1	1	1
Waveform output channels per TCC	8	8	6
DMA channels	6	6	6
Configurable Custom Logic (CCL) (LUTs)	4	4	4
Serial Communication Interface (SERCOM) instances	4	4	4
Analog-to-Digital Converter (ADC) channels	12	12	10
Analog Comparators (AC)	2	2	2
Real-Time Counter (RTC)	Yes	Yes	Yes
RTC alarms	1	1	1
RTC compare values	One 32-bit value or two 16-bit values	One 32-bit value or two 16-bit values	One 32-bit value or two 16-bit values
External Interrupt lines	16	16	16
Peripheral Touch Controller (PTC)	32	22	16
Number of self-capacitance channels (Y-lines)			
Peripheral Touch Controller (PTC)	256 (16x16)	121 (11x11)	64 (8x8)
Number of mutual-capacitance channels (X x Y lines)			
Maximum CPU frequency	48MHz		
Packages	QFN TQFP WLCSP	QFN TQFP	QFN TQFP

	SAM C20J	SAM C20G	SAM C20E
Oscillators	32.768kHz crystal oscillator (XOSC32K) 0.4-32MHz crystal oscillator (XOSC) 32.768kHz internal oscillator (OSC32K) 32KHz ultra-low-power internal oscillator (OSCULP32K) 48MHz high-accuracy internal oscillator (OSC48M) 96MHz Fractional Digital Phased Locked Loop (FDPLL96M)		
Event System channels	6	6	6
SW Debug Interface	Yes	Yes	Yes
Watchdog Timer (WDT)	Yes	Yes	Yes

Related Links

[I/O Multiplexing and Considerations](#) on page 21

3. Ordering Information



3.1. SAM C20E

Table 3-1. SAM C20E15A Ordering Codes

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type	Temp
ATSAM C20E15A-AUT	32K	4K	TQFP32	Tape & Reel	85°C
ATSAM C20E15A-ANT	32K	4K	TQFP32	Tape & Reel	105°C
ATSAM C20E15A-MUT	32K	4K	QFN32	Tape & Reel	85°C
ATSAM C20E15A-MNT	32K	4K	QFN32	Tape & Reel	105°C

Table 3-2. SAM C20E16A Ordering Codes

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type	Temp
ATSAM C20E16A-AUT	64K	8K	TQFP32	Tape & Reel	85°C
ATSAM C20E16A-ANT	64K	8K	TQFP32	Tape & Reel	105°C
ATSAM C20E16A-MUT	64K	8K	QFN32	Tape & Reel	85°C
ATSAM C20E16A-MNT	64K	8K	QFN32	Tape & Reel	105°C

Table 3-3. SAM C20E17A Ordering Codes

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type	Temp
ATSAM C20E17A-AUT	128K	16K	TQFP32	Tape & Reel	85°C
ATSAM C20E17A-ANT	128K	16K	TQFP32	Tape & Reel	105°C
ATSAM C20E17A-MUT	128K	16K	QFN32	Tape & Reel	85°C
ATSAM C20E17A-MNT	128K	16K	QFN32	Tape & Reel	105°C

Table 3-4. SAM C20E18A Ordering Codes

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type	Temp
ATSAM C20E18A-AUT	256K	32K	TQFP32	Tape & Reel	85°C
ATSAM C20E18A-ANT	256K	32K	TQFP32	Tape & Reel	105°C
ATSAM C20E18A-MUT	256K	32K	QFN32	Tape & Reel	85°C
ATSAM C20E18A-MNT	256K	32K	QFN32	Tape & Reel	105°C

3.2. SAM C20G

Table 3-5. SAM C20G15A Ordering Codes

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type	Temp
ATSAM C20G15A-AUT	32K	4K	TQFP48	Tape & Reel	85°C
ATSAM C20G15A-ANT	32K	4K	TQFP48	Tape & Reel	105°C
ATSAM C20G15A-MUT	32K	4K	QFN48	Tape & Reel	85°C
ATSAM C20G15A-MNT	32K	4K	QFN48	Tape & Reel	105°C

Table 3-6. SAM C20G16A Ordering Codes

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type	Temp
ATSAM C20G16A-AUT	64K	8K	TQFP48	Tape & Reel	85°C
ATSAM C20G16A-ANT	64K	8K	TQFP48	Tape & Reel	105°C
ATSAM C20G16A-MUT	64K	8K	QFN48	Tape & Reel	85°C
ATSAM C20G16A-MNT	64K	8K	QFN48	Tape & Reel	105°C

Table 3-7. SAM C20G17A Ordering Codes

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type	Temp
ATSAM C20G17A-AUT	128K	16K	TQFP48	Tape & Reel	85°C
ATSAM C20G17A-ANT	128K	16K	TQFP48	Tape & Reel	105°C
ATSAM C20G17A-MUT	128K	16K	QFN48	Tape & Reel	85°C
ATSAM C20G17A-MNT	128K	16K	QFN48	Tape & Reel	105°C

Table 3-8. SAM C20G18A Ordering Codes

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type	Temp
ATSAM C20G18A-AUT	256K	32K	TQFP48	Tape & Reel	85°C
ATSAM C20G18A-ANT	256K	32K	TQFP48	Tape & Reel	105°C
ATSAM C20G18A-MUT	256K	32K	QFN48	Tape & Reel	85°C
ATSAM C20G18A-MNT	256K	32K	QFN48	Tape & Reel	105°C

3.3. SAM C20J

Table 3-9. SAM C20J15A Ordering Codes

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type	Temp
ATSAM C20J15A-AUT	32K	4K	TQFP64	Tape & Reel	85°C
ATSAM C20J15A-ANT	32K	4K	TQFP64	Tape & Reel	105°C
ATSAM C20J15A-MUT	32K	4K	QFN64	Tape & Reel	85°C
ATSAM C20J15A-MNT	32K	4K	QFN64	Tape & Reel	105°C

Table 3-10. SAM C20J16A Ordering Codes

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type	Temp
ATSAM C20J16A-AUT	64K	8K	TQFP64	Tape & Reel	85°C
ATSAM C20J16A-ANT	64K	8K	TQFP64	Tape & Reel	105°C
ATSAM C20J16A-MUT	64K	8K	QFN64	Tape & Reel	85°C
ATSAM C20J16A-MNT	64K	8K	QFN64	Tape & Reel	105°C

Table 3-11. SAM C20J17A Ordering Codes

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type	Temp
ATSAM C20J17A-AUT	128K	16K	TQFP64	Tape & Reel	85°C
ATSAM C20J17A-ANT	128K	16K	TQFP64	Tape & Reel	105°C
ATSAM C20J17A-MUT	128K	16K	QFN64	Tape & Reel	85°C
ATSAM C20J17A-MNT	128K	16K	QFN64	Tape & Reel	105°C
ATSAM C20J17A-UUT ⁽¹⁾	128K	16K	WLCSP56	Tape & Reel	85°C

1. Contact your local Microchip sales representative for availability.

Table 3-12. SAM C20J18A Ordering Codes

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type	Temp
ATSAM C20J18A-AUT	256K	32K	TQFP64	Tape & Reel	85°C
ATSAM C20J18A-ANT	256K	32K	TQFP64	Tape & Reel	105°C
ATSAM C20J18A-MUT	256K	32K	QFN64	Tape & Reel	85°C
ATSAM C20J18A-MNT	256K	32K	QFN64	Tape & Reel	105°C
ATSAM C20J18A-UUT ⁽¹⁾	256K	32K	WLCSP56	Tape & Reel	85°C

1. Contact your local Microchip sales representative for availability.

3.4. Device Identification

The DSU - Device Service Unit peripheral provides the Device Selection bits in the Device Identification register (DID.DEVSEL) in order to identify the device by software. The SAM C20 variants have a reset value of DID=0x1101drxx, with the LSB identifying the die number ('d'), the die revision ('r') and the device selection ('xx').

Table 3-13. SAM C20 Device Identification Values

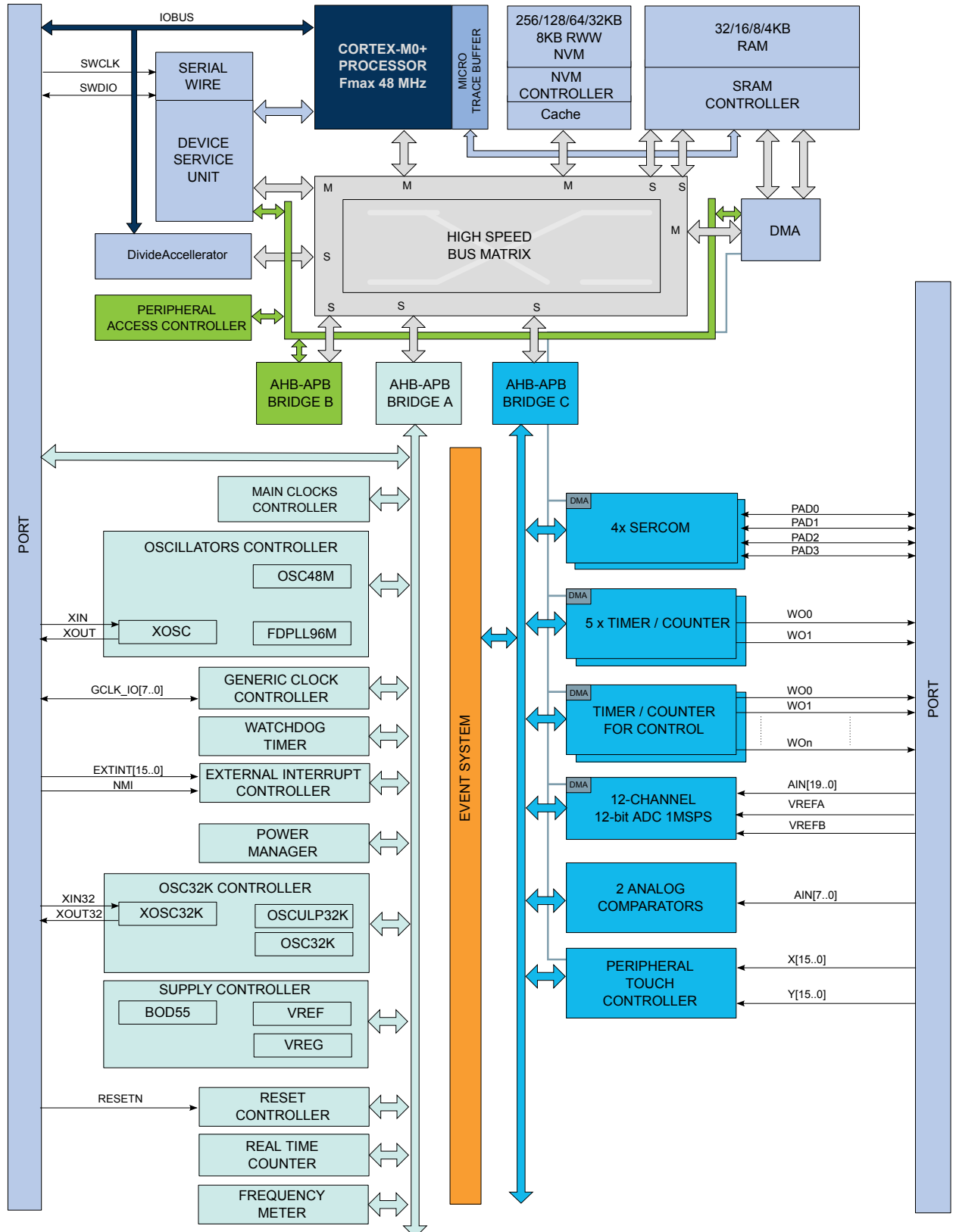
DEVSEL (DID[7:0])	Device
0x00	SAM C20J18A
0x01	SAM C20J17A
0x02	SAM C20J16A
0x03	SAM C20J15A
0x04	Reserved
0x05	SAM C20G18A
0x06	SAM C20G17A
0x07	SAM C20G16A
0x08	SAM C20G15A

DEVSEL (DID[7:0])	Device
0x09	Reserved
0x0A	SAM C20E18A
0x0B	SAM C20E17A
0x0C	SAM C20E16A
0x0D	SAM C20E15A
0x0E-0xFF	Reserved

Note: The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die.

4. Block Diagram

Figure 4-1. System Block Diagram for SAM C20E/G/J



Note:

1. Some products have different number of SERCOM instances, Timer/Counter instances, PTC signals and ADC signals.
2. The three TCC instances have different configurations, including the number of Waveform Output (WO) lines.

Related Links

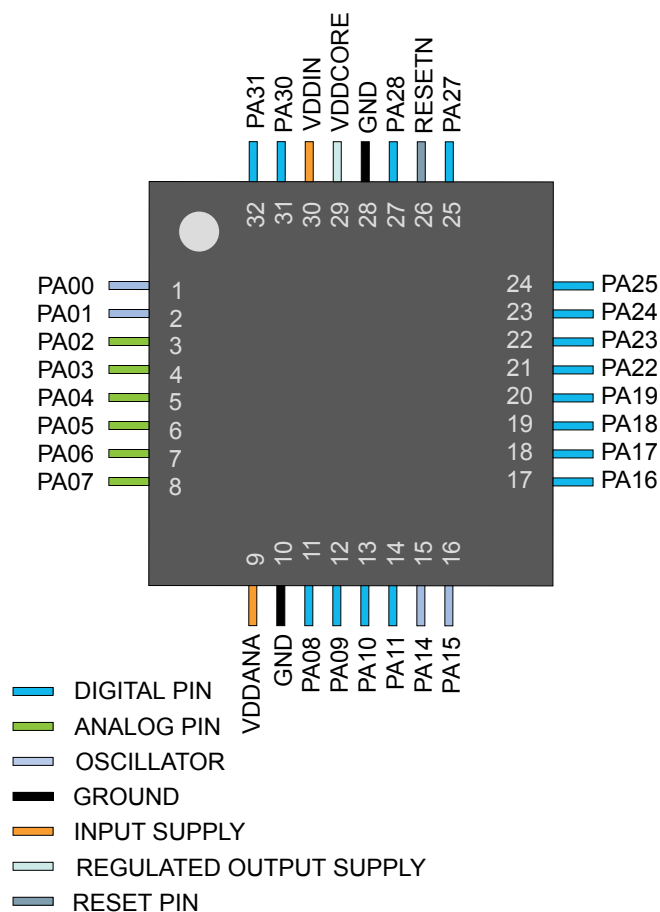
[TCC Configurations](#) on page 24

[Multiplexed Signals](#) on page 21

5. Pinout

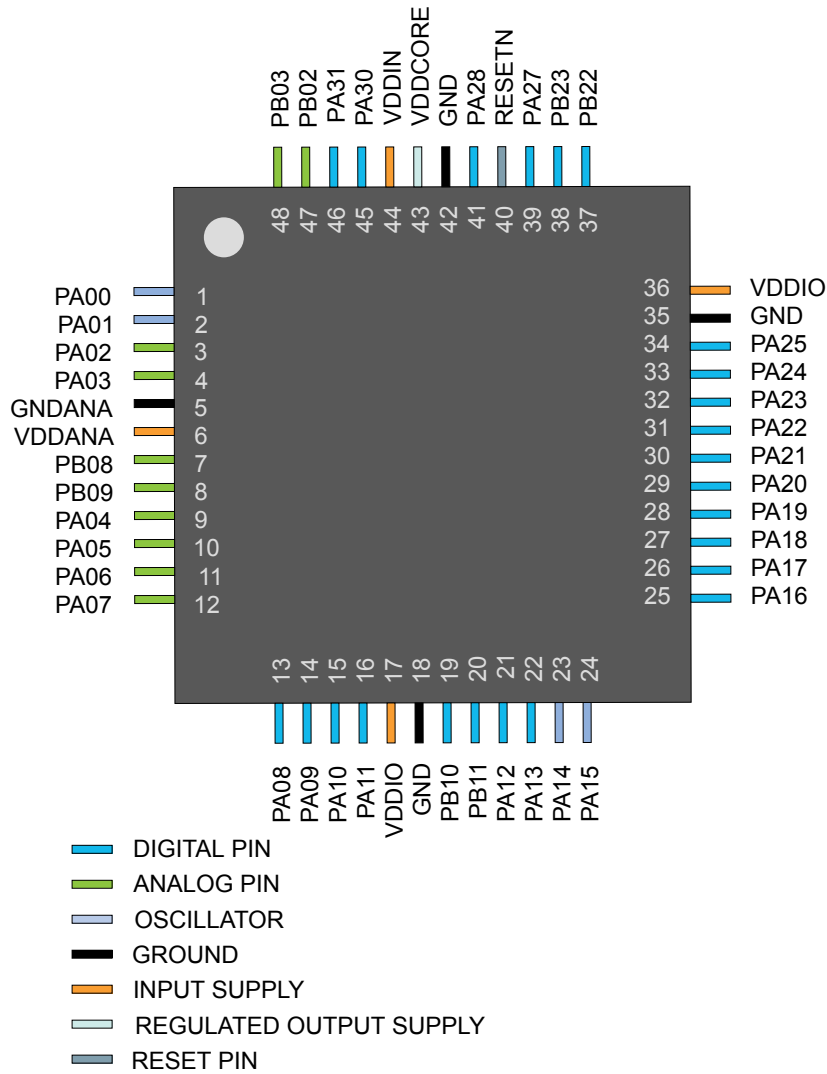
5.1. SAM C20E

5.1.1. QFN32 / TQFP32



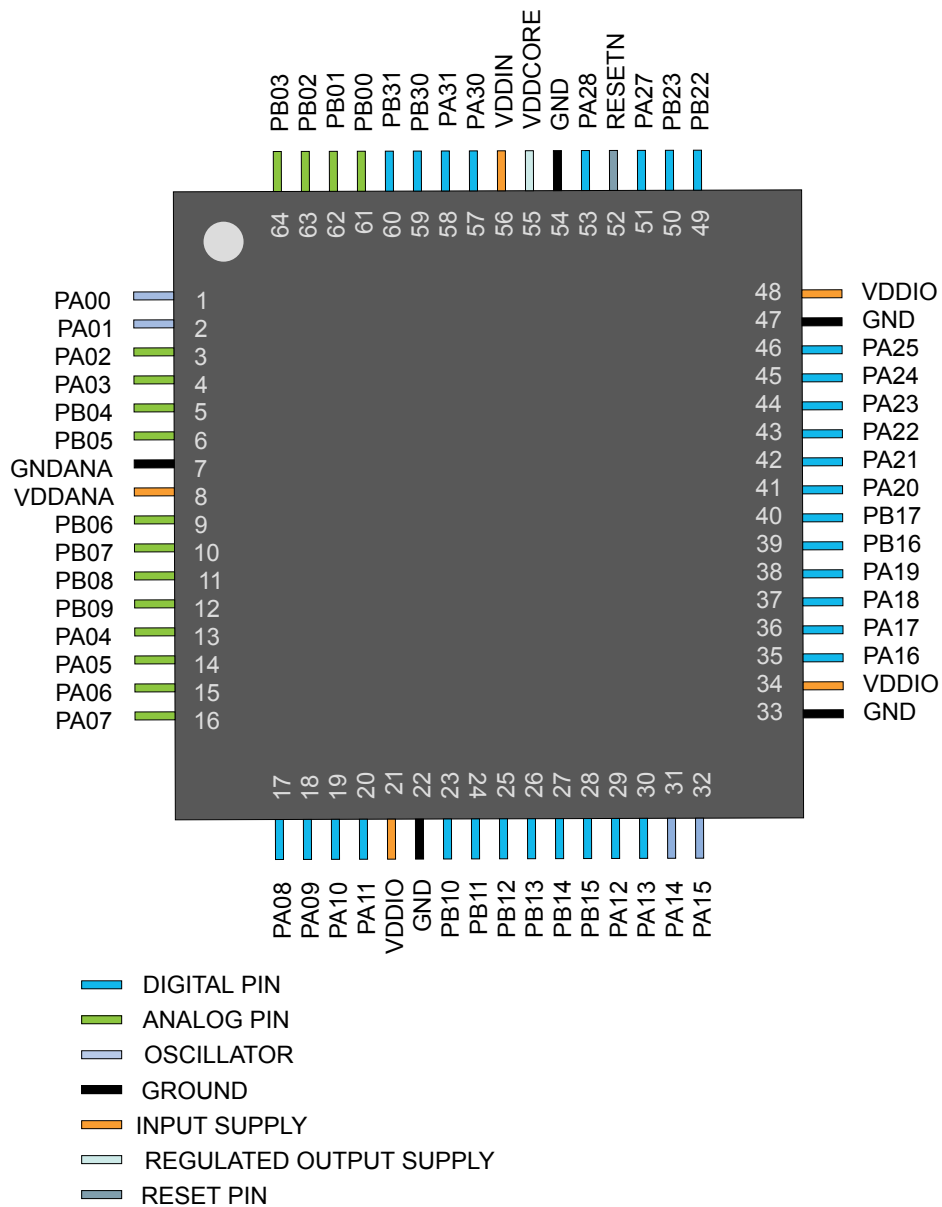
5.2. SAM C20G

5.2.1. QFN48 / TQFP48

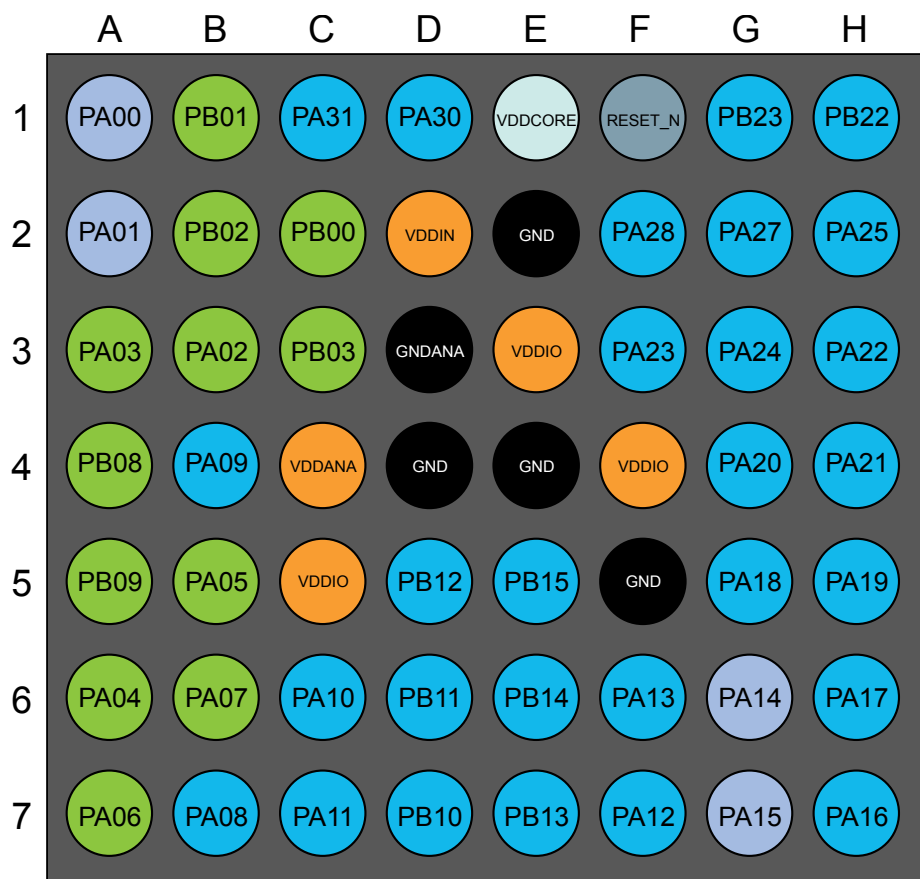


5.3. SAM C20J

5.3.1. QFN64 / TQFP64



5.3.2. WLCSP56



- DIGITAL PIN
- ANALOG PIN
- OSCILLATOR
- GROUND
- INPUT SUPPLY
- REGULATED OUTPUT SUPPLY
- RESET PIN

6. Signal Descriptions List

The following table gives details on signal names classified by peripheral.

Table 6-1. Signal Descriptions List

Signal Name	Function	Type	Active Level
Analog Comparators - AC			
AIN[7:0]	AC Analog Inputs	Analog	
CMP[2:0]	AC Comparator Outputs	Digital	
Analog Digital Converter - ADCx			
AIN[11:0]	ADC Analog Inputs	Analog	
VREFA	ADC Voltage External Reference A	Analog	
External Interrupt Controller - EIC			
EXTINT[15:0]	External Interrupts inputs	Digital	
NMI	External Non-Maskable Interrupt input	Digital	
Generic Clock Generator - GCLK			
GCLK_IO[7:0]	Generic Clock (source clock inputs or generic clock generator output)	Digital	
Custom Control Logic - CCL			
IN[11:0]	Logic Inputs	Digital	
OUT[3:0]	Logic Outputs	Digital	
Power Manager - PM			
RESETN	Reset input	Digital	Low
Serial Communication Interface - SERCOMx			
PAD[3:0]	SERCOM Inputs/Outputs Pads	Digital	
Oscillators Control - OSCCTRL			
XIN	Crystal or external clock Input	Analog/Digital	
XOUT	Crystal Output	Analog	
32KHz Oscillators Control - OSC32CTRL			
XIN32	32KHz Crystal or external clock Input	Analog/Digital	
XOUT32	32KHz Crystal Output	Analog	
Timer Counter - TCx			
WO[1:0]	Waveform Outputs	Digital	
Timer Counter - TCCx			
WO[1:0]	Waveform Outputs	Digital	
Peripheral Touch Controller - PTC			
X[15:0]	PTC Input	Analog	
Y[15:0]	PTC Input	Analog	
General Purpose I/O - PORT			
PA25 - PA00	Parallel I/O Controller I/O Port A	Digital	

Signal Name	Function	Type	Active Level
PA28 - PA27	Parallel I/O Controller I/O Port A	Digital	
PA31 - PA30	Parallel I/O Controller I/O Port A	Digital	
PB17 - PB00	Parallel I/O Controller I/O Port B	Digital	
PB23 - PB22	Parallel I/O Controller I/O Port B	Digital	
PB31 - PB30	Parallel I/O Controller I/O Port B	Digital	

7. I/O Multiplexing and Considerations

7.1. Multiplexed Signals

Each pin is by default controlled by the PORT as a general purpose I/O and alternatively it can be assigned to one of the peripheral functions A, B, C, D, E, F, G, H or I. To enable a peripheral function on a pin, the Peripheral Multiplexer Enable bit in the Pin Configuration register corresponding to that pin (PINCFGn.PMUXEN, n = 0-31) in the PORT must be written to one. The selection of peripheral function A to H is done by writing to the Peripheral Multiplexing Odd and Even bits in the Peripheral Multiplexing register (PMUXn.PMUXE/O) in the PORT.

Table 7-1. PORT Function Multiplexing

	Pin ⁽¹⁾		I/O Pin	Supply	A			B ⁽²⁾⁽³⁾		C	D	E	F	G	H	I
SAM C20E	SAM C20G	SAM C20J			EIC	REF	ADC0	AC	PTC	SERCOM ⁽²⁾⁽³⁾	SERCOM-ALT	TC TCC	TCC	COM	AC/GCLK	CCL
1	1	1	PA00	VDDANA	EXTINT[0]						SERCOM1/ PAD[0]				CMP[2]	
2	2	2	PA01	VDDANA	EXTINT[1]						SERCOM1/ PAD[1]				CMP[3]	
3	3	3	PA02	VDDANA	EXTINT[2]		AIN[0]	AIN[4]	Y[0]							
4	4	4	PA03	VDDANA	EXTINT[3]	ADC/VREFA	AIN[1]	AIN[5]	Y[1]							
		5	PB04	VDDANA	EXTINT[4]				Y[10]							
		6	PB05	VDDANA	EXTINT[5]			AIN[6]	Y[11]							
		9	PB06	VDDANA	EXTINT[6]			AIN[7]	Y[12]							CCL2/ IN[6]
		10	PB07	VDDANA	EXTINT[7]				Y[13]							CCL2/ IN[7]
	7	11	PB08	VDDANA	EXTINT[8]		AIN[2]		Y[14]			TC0/WO[0]				CCL2/ IN[8]
	8	12	PB09	VDDANA	EXTINT[9]		AIN[3]		Y[15]			TC0WO[1]				CCL2/ OUT[2]
5	9	13	PA04	VDDANA	EXTINT[4]		AIN[4]	AIN[0]	Y[2]		SERCOM0/ PAD[0]	TCC0/WO[0]				CCL0/ IN[0]
6	10	14	PA05	VDDANA	EXTINT[5]		AIN[5]	AIN[1]	Y[3]		SERCOM0/ PAD[1]	TCC0/WO[1]				CCL0/ IN[1]
7	11	15	PA06	VDDANA	EXTINT[6]		AIN[6]	AIN[2]	Y[4]		SERCOM0/ PAD[2]					CCL0/ IN[2]
8	12	16	PA07	VDDANA	EXTINT[7]		AIN[7]	AIN[3]	Y[5]		SERCOM0/ PAD[3]					CCL0/ OUT[0]
11	13	17	PA08	VDDIO	NMI		AIN[8]		X[0]/Y[16]	SERCOM0/ PAD[0]	SERCOM2/ PAD[0]	TCC0/WO[0]				CCL1/ IN[3]
12	14	18	PA09	VDDIO	EXTINT[9]		AIN[9]		X[1]/Y[17]	SERCOM0/ PAD[1]	SERCOM2/ PAD[1]	TCC0/WO[1]				CCL1/ IN[4]
13	15	19	PA10	VDDIO	EXTINT[10]		AIN[10]		X[2]/Y[18]	SERCOM0/ PAD[2]	SERCOM2/ PAD[2]		TCC0/ WO[2]		GCLK_IO[4]	CCL1/ IN[5]
14	16	20	PA11	VDDIO	EXTINT[11]		AIN[11]		X[3]/Y[19]	SERCOM0/ PAD[3]	SERCOM2/ PAD[3]		TCC0/ WO[3]		GCLK_IO[5]	CCL1/ OUT[1]
	19	23	PB10	VDDIO	EXTINT[10]							TC1/WO[0]	TCC0/ WO[4]		GCLK_IO[4]	CCL1/ IN[5]
	20	24	PB11	VDDIO	EXTINT[11]							TC1/WO[1]	TCC0/ WO[5]		GCLK_IO[5]	CCL1/ OUT[1]
		25	PB12	VDDIO	EXTINT[12]				X[12]/Y[28]			TC0/WO[0]	TCC0/ WO[6]		GCLK_IO[6]	
		26	PB13	VDDIO	EXTINT[13]				X[13]/Y[29]			TC0/WO[1]	TCC0/ WO[7]		GCLK_IO[7]	
		27	PB14	VDDIO	EXTINT[14]				X[14]/Y[30]			TC1/WO[0]			GCLK_IO[0]	CCL3/ IN[9]
		28	PB15	VDDIO	EXTINT[15]				X[15]/Y[31]			TC1/WO[1]			GCLK_IO[1]	CCL3/ IN[10]
	21	29	PA12	VDDIO	EXTINT[12]					SERCOM2/ PAD[0]			TCC0/ WO[6]		AC/CMP[0]	
	22	30	PA13	VDDIO	EXTINT[13]					SERCOM2/ PAD[1]			TCC0/ WO[7]		AC/CMP[1]	
15	23	31	PA14	VDDIO	EXTINT[14]					SERCOM2/ PAD[2]		TC4/WO[0]	TCC0/ WO[4]		GCLK_IO[0]	
16	24	32	PA15	VDDIO	EXTINT[15]					SERCOM2/ PAD[3]		TC4/WO[1]	TCC0/ WO[5]		GCLK_IO[1]	
17	25	35	PA16	VDDIO	EXTINT[0]				X[4]/Y[20]	SERCOM1/ PAD[0]	SERCOM3/ PAD[0]		TCC0/ WO[6]		GCLK_IO[2]	CCL0/ IN[0]

SAM C20E	Pin ⁽¹⁾ SAM C20G	SAM C20J	I/O Pin	Supply	A EIC	REF	ADC0	B ⁽²⁾⁽³⁾ AC	PTC	C SERCOM ⁽²⁾⁽³⁾	D SERCOM-ALT	E TC TCC	F TCC	G COM	H AC/GCLK	I CCL
18	26	36	PA17	VDDIO	EXTINT[1]				X[5]/Y[21]	SERCOM1/ PAD[1]	SERCOM3/ PAD[1]		TCC0/ WO[7]		GCLK_IO[3]	CCL0/ IN[1]
19	27	37	PA18	VDDIO	EXTINT[2]				X[6]/Y[22]	SERCOM1/ PAD[2]	SERCOM3/ PAD[2]	TC4/WO[0]	TCC0/ WO[2]		AC/CMP[0]	CCL0/ IN[2]
20	28	38	PA19	VDDIO	EXTINT[3]				X[7]/Y[23]	SERCOM1/ PAD[3]	SERCOM3/ PAD[3]	TC4/WO[1]	TCC0/ WO[3]		AC/CMP[1]	CCL0/ OUT[0]
		39	PB16	VDDIO	EXTINT[0]							TC2/WO[0]	TCC0/ WO[4]		GCLK_IO[2]	CCL3/ IN[11]
		40	PB17	VDDIO	EXTINT[1]							TC2/WO[1]	TCC0/ WO[5]		GCLK_IO[3]	CCL3/ OUT[3]
	29	41	PA20	VDDIO	EXTINT[4]				X[8]/Y[24]		SERCOM3/ PAD[2]	TC3/WO[0]	TCC0/ WO[6]		GCLK_IO[4]	
	30	42	PA21	VDDIO	EXTINT[5]				X[9]/Y[25]		SERCOM3/ PAD[3]	TC3/WO[1]	TCC0/ WO[7]		GCLK_IO[5]	
21	31	43	PA22	VDDIO	EXTINT[6]				X[10]/Y[26]	SERCOM3/ PAD[0]		TC0/WO[0]	TCC0/ WO[4]		GCLK_IO[6]	CCL2/ IN[6]
22	32	44	PA23	VDDIO	EXTINT[7]				X[11]/Y[27]	SERCOM3/ PAD[1]		TC0/WO[1]	TCC0/ WO[5]		GCLK_IO[7]	CCL2/ IN[7]
23	33	45	PA24	VDDIO	EXTINT[12]					SERCOM3/ PAD[2]		TC1/WO[0]			AC/CMP[2]	CCL2/ IN[8]
24	34	46	PA25	VDDIO	EXTINT[13]					SERCOM3/ PAD[3]		TC1/WO[1]			AC/CMP[3]	CCL2/ OUT[2]
	37	49	PB22	VDDIN	EXTINT[6]							TC3/WO[0]			GCLK_IO[0]	CCL0/ IN[0]
	38	50	PB23	VDDIN	EXTINT[7]							TC3/WO[1]			GCLK_IO[1]	CCL0/ OUT[0]
25	39	51	PA27	VDDIN	EXTINT[15]									BRK	GCLK_IO[0]	
27	41	53	PA28	VDDIN	EXTINT[8]										GCLK_IO[0]	
31	45	57	PA30	VDDIN	EXTINT[10]						SERCOM1/ PAD[2]			CORTEX_M0P/ SWCLK	GCLK_IO[0]	CCL1/ IN[3]
32	46	58	PA31	VDDIN	EXTINT[11]						SERCOM1/ PAD[3]			CORTEX_M0P/ SWDIO		CCL1/ OUT[1]
		59	PB30	VDDIN	EXTINT[14]							TC0/WO[0]			AC/CMP[2]	
		60	PB31	VDDIN	EXTINT[15]							TC0/WO[1]			AC/CMP[3]	
		61	PB00	VDDANA	EXTINT[0]				Y[6]			TC3/WO[0]				CCL0/ IN[1]
		62	PB01	VDDANA	EXTINT[1]				Y[7]			TC3/WO[1]				CCL0/ IN[2]
	47	63	PB02	VDDANA	EXTINT[2]				Y[8]			TC2/WO[0]				CCL0/ OUT[0]
	48	64	PB03	VDDANA	EXTINT[3]				Y[9]			TC2/WO[1]				

1. Use the SAM C21J pinout muxing for the WLCSP56 package.
2. All analog pin functions are on peripheral function B. Peripheral function B must be selected to disable the digital control of the pin.
3. Only some pins can be used in SERCOM I2C mode. Refer to [SERCOM I2C Pins](#).

Related Links

[SERCOM I2C Pins](#) on page 23

7.2. Other Functions

7.2.1. Oscillator Pinout

The oscillators are not mapped to the normal PORT functions and their multiplexing are controlled by registers in the Oscillators Controller (OSCCTRL) and in the 32K Oscillators Controller (OSC32KCTRL).

Table 7-2. Oscillator Pinout

Oscillator	Supply	Signal	I/O pin
XOSC	VDDIO	XIN	PA14
		XOUT	PA15

Oscillator	Supply	Signal	I/O pin
XOSC32K	VDDANA	XIN32	PA00
		XOUT32	PA01

7.2.2. Serial Wire Debug Interface Pinout

Only the SWCLK pin is mapped to the normal PORT functions. A debugger cold-plugging or hot-plugging detection will automatically switch the SWDIO port to the SWDIO function.

Table 7-3. Serial Wire Debug Interface Pinout

Signal	Supply	I/O pin
SWCLK	VDDIN	PA30
SWDIO	VDDIN	PA31

7.2.3. SERCOM I²C Pins

Table 7-4. SERCOM Pins Supporting I²C

Device	Pins Supporting I ² C Hs mode
SAM C20E	PA08, PA09, PA10, PA11, PA16, PA17, PA22, PA23
SAM C20G	PA08, PA09, PA10, PA11, PA12, PA13, PA16, PA17, PA22, PA23, PB10, PB11
SAM C20J	PA08, PA09, PA10, PA11, PA12, PA13, PA16, PA17, PA22, PA23, PB10, PB11, PB12, PB13, PB16, PB17, PB30, PB31

7.2.4. GPIO Clusters

Table 7-5. GPIO Clusters

Package	Cluster	GPIO	Supplies Pin connected to the cluster	
64 pins	1	PB31 PB30 PA31 PA30 PA28 PA27	VDDIN (56)	GND (54)
	2	PB23 PB22	VDDIO (48)	GND (54+47)
	3	PA25 PA24 PA23 PA22 PA21 PA20 PB17 PB16 PA19 PA18 PA17 PA16	VDDIO (48+34)	GND (47+33)
	4	PA15 PA14 PA13 PA12 PB15 PB14 PB13 PB12 PB11 PB10	VDDIO (34+21)	GND (33+22)
	5	PA11 PA10 PA08 PA09	VDDIO (21)	GND (22)
	6	PA07 PA06 PA05 PA04 PB09 PB08 PB07 PB06 PB05 PB04 PA03 PA02 PA01 PA00 PB03 PB02 PB01 PB00	VDDANA (8)	GNDANA (7)

Package	Cluster	GPIO	Supplies Pin connected to the cluster	
48 pins	1	PA31 PA30 PA28 PA27	VDDIN (44)	GND (42)
	2	PB23 PB22	VDDIO (36)	GND (42+35)
	3	PA25 PA24 PA23 PA22 PA21 PA20 PA19 PA18 PA17 PA16 PA15 PA14 PA13 PA12 PB11 PB10	VDDIO (36+17)	GND (35+18)
	4	PA11 PA10 PA08 PA09	VDDIO (17)	GND (18)
	5	PA07 PA06 PA05 PA04 PB09 PB08 PA03 PA02 PA01 PA00 PB03 PB02	VDDANA (6)	GNDANA (5)
32 pins	1	PA31 PA30 PA28 PA27	VDDIN (30)	GND (28)
	2	PA25 PA24 PA23 PA22 PA19 PA18 PA17 PA16 PA15 PA14 PA11 PA10 PA08 PA09	VDDIO (9)	GND (28+10)
	3	PA07 PA06 PA05 PA04 PA03 PA02 PA01 PA00	VDDANA (9)	GND (28+10)

7.2.5. TCC Configurations

The SAM C20 has one instance of the Timer/Counter for Control applications (TCC) peripheral, . The following table lists the features for each TCC instance.

Table 7-6. TCC Configuration Summary

TCC#	Channels (CC_NUM)	Waveform Output (WO_NUM)	Counter size	Fault	Dithering	Output matrix	Dead Time Insertion (DTI)	SWAP	Pattern generation
0	4	8	24-bit	Yes	Yes	Yes	Yes	Yes	Yes

Note: The number of CC registers (CC_NUM) for each TCC corresponds to the number of compare/capture channels, so that a TCC can have more Waveform Outputs (WO_NUM) than CC registers.

8. Product Mapping

Figure 8-1. SAM C20 Product Mapping

