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**32-bit ARM Cortex-M0+ with 5V Support, CAN-FD, PTC,
and Advanced Analog**

Features

Operating Conditions

- 2.7V – 5.5V, -40°C to +105°C, DC to 48 MHz

Core

- ARM® Cortex®-M0+ CPU running at up to 48 MHz
 - Single-cycle hardware multiplier
 - Micro Trace Buffer
 - Memory Protection Unit (MPU)

Memories

- 32/64/128/256 KB in-system self-programmable Flash
- 1/2/4/8 KB independent self-programmable Flash for EEPROM emulation
- 4/8/16/32 KB SRAM Main Memory

System

- Power-on Reset (POR) and Brown-out Detection (BOD)
- Internal and external clock options with 48 MHz to 96 MHz Fractional Digital Phase Locked Loop (FDPLL96M)
- External Interrupt Controller (EIC) (Interrupt pin debouncing is only available in SAM C21N)
- 16 external interrupts
 - Hardware debouncing (only on the 100Pin TQFP)
- One non-maskable interrupt
- Two-pin Serial Wire Debug (SWD) programming, test, and debugging interface

Low-Power

- Idle and Standby Sleep modes
- SleepWalking peripherals

Peripherals

- Hardware Divide and Square Root Accelerator (DIVAS)
- 12-channel Direct Memory Access Controller (DMAC)
- 12-channel Event System
- Up to eight 16-bit Timer/Counters (TC), configurable as either (see **Note**):
Note: Maximum and minimum capture is only available in SAM C21N devices.
 - One 16-bit TC with compare/capture channels
 - One 8-bit TC with compare/capture channels
 - One 32-bit TC with compare/capture channels, by using two TCs

- Two 24-bit Timer/Counters and one 16-bit Timer/Counter for Control (TCC), with extended functions:
 - Up to four compare channels with optional complementary output
 - Generation of synchronized pulse width modulation (PWM) pattern across port pins
 - Deterministic fault protection, fast decay and configurable dead-time between complementary output
 - Dithering that increase resolution with up to 5 bit and reduce quantization error
- Frequency Meter (The division reference clock is only available in the SAM C21N)
- 32-bit Real Time Counter (RTC) with clock/calendar function
- Watchdog Timer (WDT)
- CRC-32 generator
- Up to two Controller Area Network (CAN) interfaces:
 - CAN 2.0A/B
 - CAN-FD 1.0
 - Each CAN interface have two selectable pin locations to switch between two external CAN transceivers (without the need for an external switch)
- Up to eight Serial Communication Interfaces (SERCOM), each configurable to operate as either:
 - USART with full-duplex and single-wire half-duplex configuration
 - I²C up to 3.4 MHz (Except SERCOM6 and SERCOM7)
 - SPI
 - LIN master/slave
 - RS-485
 - PMBus
- One Configurable Custom Logic (CCL)
- Up to Two 12-bit, 1 Msps Analog-to-Digital Converter (ADC) with up to 12 channels each (20 unique channels)
 - Differential and single-ended input
 - Automatic offset and gain error compensation
 - Oversampling and decimation in hardware to support 13-, 14-, 15- or 16-bit resolution
- One 16-bit Sigma-Delta Analog-to-Digital Converter (SDADC) with up to 3 differential channels
- 10-bit, 350 ksps Digital-to-Analog Converter (DAC)
- Up to four Analog Comparators (AC) with Window Compare function
- Integrated Temperature Sensor
- Peripheral Touch Controller (PTC)
 - 256-Channel capacitive touch and proximity sensing

I/O

- Up to 84 programmable I/O pins

Packages

- 100-pin TQFP
- 64-pin TQFP, QFN
- 56-pin WLCSP
- 48-pin TQFP, QFN
- 32-pin TQFP, QFN

General

- Drop in compatible with SAM D20 and SAM D21 (see **Note**)

Note: Only applicable for 32-, 48-, and 64-pin TQFP and QFN packages.

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1. Configuration Summary

Table 1-1. SAM C20 Device-specific Features

Device	Flash (KB)	SRAM (KB)
ATSAMC20E15	32	4
ATSAMC20E16	64	8
ATSAMC20E17	128	16
ATSAMC20E18	256	32
ATSAMC20G15	32	4
ATSAMC20G16	64	8
ATSAMC20G17	128	16
ATSAMC20G18	256	32
ATSAMC20J15	32	4
ATSAMC20J16	64	8
ATSAMC20J17	128	16
ATSAMC20J18	256	32
ATSAMC20N17	128	16
ATSAMC20N18	256	32

Table 1-2. SAM C21 Device-specific Features

Device	Flash (KB)	SRAM (KB)
ATSAMC21E15	32	4
ATSAMC21E16	64	8
ATSAMC21E17	128	16
ATSAMC21E18	256	32
ATSAMC21G15	32	4
ATSAMC21G16	64	8
ATSAMC21G17	128	16
ATSAMC21G18	256	32
ATSAMC21J15	32	4
ATSAMC21J16	64	8
ATSAMC21J17	128	16
ATSAMC21J18	256	32

Device	Flash (KB)	SRAM (KB)
ATSAMC21N17	128	16
ATSAMC21N18	256	32

Table 1-3. SAM C21 Family Features

	SAM C21N	SAM C21J	SAM C21G	SAM C21E
Pins	100	64 (56 for WLCSP)	48	32
General Purpose I/O-pins (GPIOs)	84	52 (44 for WLCSP)	38	26
Flash	256/128 KB	256/128/64/32 KB	256/128/64/32 KB	256/128/64/32 KB
Flash RWW section	8/4 KB	8/4/2/1 KB	8/4/2/1 KB	8/4/2/1 KB
System SRAM	32/16 KB	32/16/8/4 KB	32/16/8/4 KB	32/16/8/4 KB
Timer Counter (TC) instances	8	5	5	5
Waveform output channels per TC instance	2	2	2	2
TC Maximum and Minimum Capture	Yes	No	No	No
Timer Counter for Control (TCC) instances	3	3	3	3
Waveform output channels per TCC	8/4/2	8/4/2	8/4/2	6/4/2
DMA channels	12	12	12	12
CAN interface	2	2	2	1
Configurable Custom Logic (CCL) (LUTs)	4	4	4	4
Serial Communication Interface (SERCOM) instances	8	6	6	4
Divide and Square Root Accelerator (DIVAS)	Yes	Yes	Yes	Yes
Analog-to-Digital Converter (ADC) channels	20	20	14	10
Analog-to-Digital Converter (ADC) instances	2	2	2	2
Sigma-Delta Analog-to-Digital Converter (SDADC) channels	3	3	2	1
Analog Comparators (AC)	4	4	4	3

	SAM C21N	SAM C21J	SAM C21G	SAM C21E
Digital-to-Analog Converter (DAC) channels	1	1	1	1
Temperature Sensor (TSENS)	1	1	1	1
Real-Time Counter (RTC)	Yes	Yes	Yes	Yes
RTC alarms	1	1	1	1
RTC compare values	One 32-bit value or two 16-bit values	One 32-bit value or two 16-bit values	One 32-bit value or two 16-bit values	One 32-bit value or two 16-bit values
External Interrupt lines	16 with HW debouncing	16	16	16
Peripheral Touch Controller (PTC) Number of self-capacitance channels (Y-lines)	32	32	22	16
Peripheral Touch Controller (PTC) Number of mutual-capacitance channels (X x Y lines)	256 (16x16)	256 (16x16)	121 (11x11)	64 (8x8)
Frequency Meter (FREQM) reference clock divider	Yes	Yes	Yes	Yes
Maximum CPU frequency	48 MHz			
Packages	TQFP	QFN TQFP WLCSP	QFN TQFP	QFN TQFP
Oscillators	32.768 kHz crystal oscillator (XOSC32K) 0.4-32 MHz crystal oscillator (XOSC) 32.768 kHz internal oscillator (OSC32K) 32 kHz ultra low-power internal oscillator (OSCULP32K) 48 MHz high-accuracy internal oscillator (OSC48M) 96 MHz Fractional Digital Phased Locked Loop (FDPLL96M)			
Event System channels	12	12	12	12
SW Debug Interface	Yes	Yes	Yes	Yes
Watchdog Timer (WDT)	Yes	Yes	Yes	Yes

Table 1-4. SAM C20 Family Features

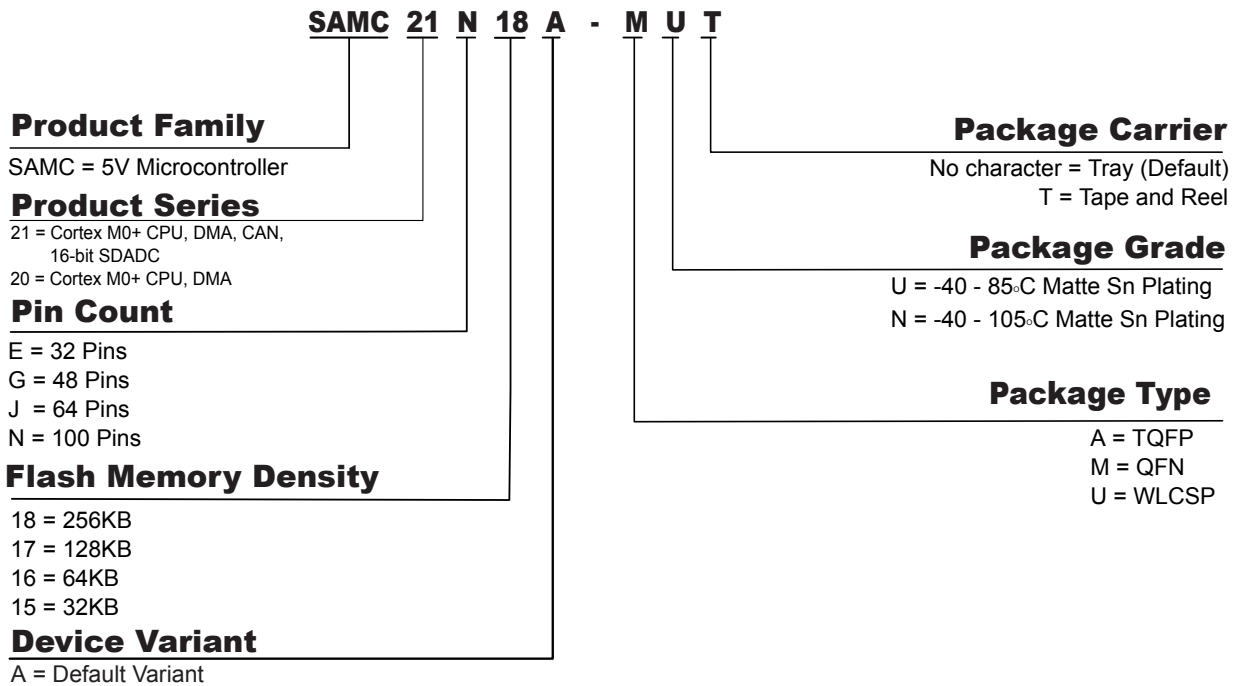
	SAM C20N	SAM C20J	SAM C20G	SAM C20E
Pins	100	64 (56 for WLCSP)	48 (44 for WLCSP)	32
General Purpose I/O-pins (GPIOs)	84	52	38	26
Flash	256/128 KB	256/128/64/32 KB	256/128/64/32 KB	256/128/64/32 KB
Flash RWW section	8/4 KB	8/4/2/1 KB	8/4/2/1 KB	8/4/2/1 KB
System SRAM	32/16 KB	32/16/8/4 KB	32/16/8/4 KB	32/16/8/4 KB
Timer Counter (TC) instances	8	5	5	5
Waveform output channels per TC instance	2	2	2	2
TC Maximum and Minimum Capture	Yes	No	No	No
Timer Counter for Control (TCC) instances	3	3	3	3
Waveform output channels per TCC	8/4/2	8/4/2	8/4/2	6/4/2
DMA channels	12	12	12	12
Configurable Custom Logic (CCL) (LUTs)	4	4	4	4
Serial Communication Interface (SERCOM) instances	8	4	4	4
Divide and Square Root Accelerator (DIVAS)	Yes	Yes	Yes	Yes
Analog-to-Digital Converter (ADC) channels	12	12	12	10
Analog-to-Digital Converter (ADC) instances	1	1	1	1
Analog Comparators (AC)	2	2	2	2
Real-Time Counter (RTC)	Yes	Yes	Yes	Yes
RTC alarms	1	1	1	1
RTC compare values	One 32-bit value or two 16-bit values	One 32-bit value or two 16-bit values	One 32-bit value or two 16-bit values	One 32-bit value or two 16-bit values
External Interrupt lines	16 with HW debouncing	16	16	16

	SAM C20N	SAM C20J	SAM C20G	SAM C20E
Peripheral Touch Controller (PTC) Number of self-capacitance channels (Y-lines)	32	32	22	16
Peripheral Touch Controller (PTC) Number of mutual-capacitance channels (X x Y lines)	256 (16x16)	256 (16x16)	121 (11x11)	64 (8x8)
Frequency Meter (FREQM) reference clock divider	Yes	Yes	Yes	Yes
Maximum CPU frequency	48 MHz			
Packages	TQFP	QFN TQFP WLCSP	QFN TQFP	QFN TQFP
Oscillators	32.768 kHz crystal oscillator (XOSC32K) 0.4-32 MHz crystal oscillator (XOSC) 32.768 kHz internal oscillator (OSC32K) 32 kHz ultra low-power internal oscillator (OSCULP32K) 48 MHz high-accuracy internal oscillator (OSC48M) 96 MHz Fractional Digital Phased Locked Loop (FDPLL96M)			
Event System channels	6	6	6	6
SW Debug Interface	Yes	Yes	Yes	Yes
Watchdog Timer (WDT)	Yes	Yes	Yes	Yes

Related Links

[I/O Multiplexing and Considerations](#)

2. Ordering Information

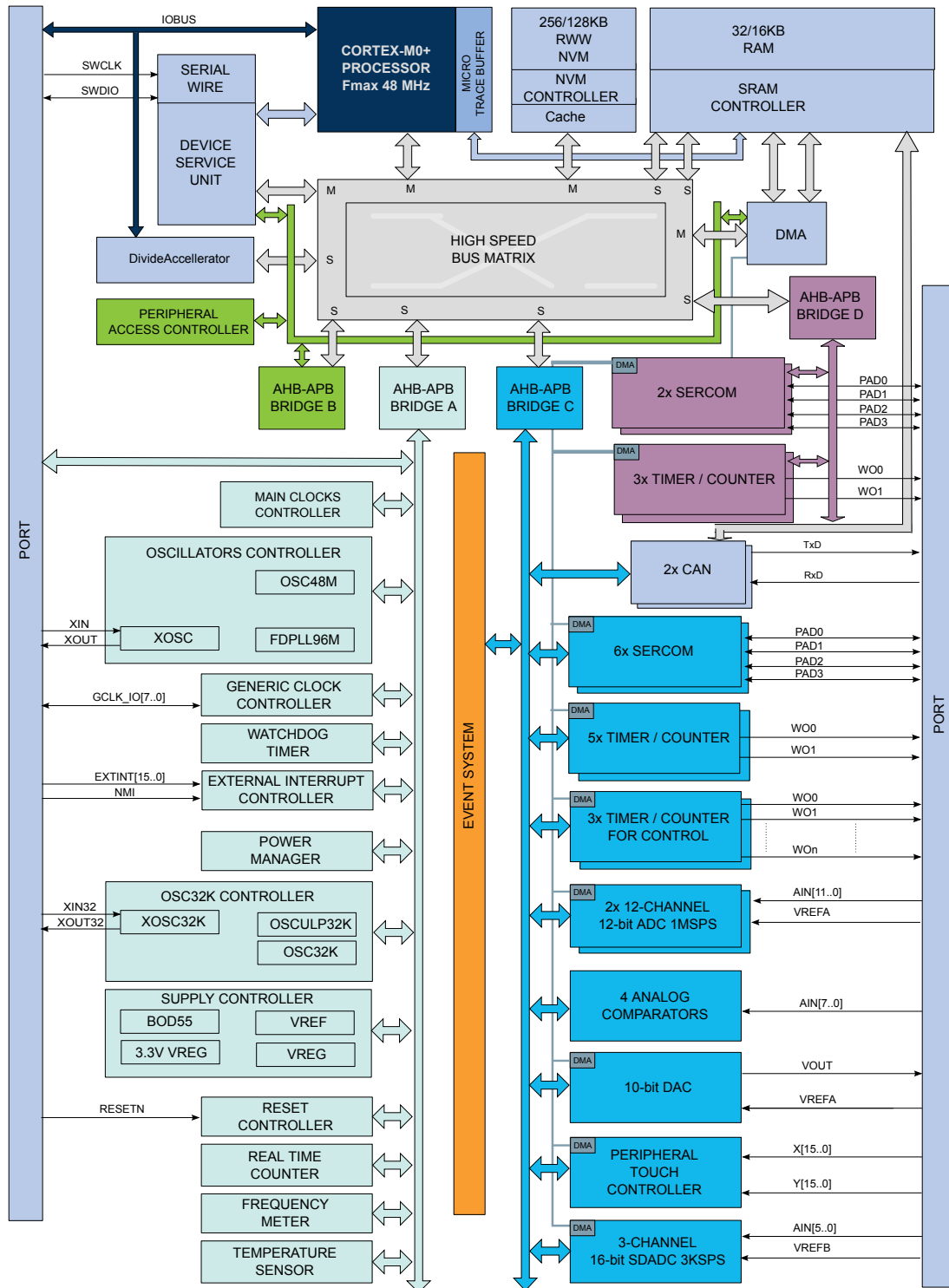


Note: Not all combinations are valid. The available ordering numbers are listed in the [Configuration Summary](#).

3. Block Diagram

Note: Not all features are available for all devices. Please refer to [Table 1-3](#) and [Table 1-4](#) to determine feature availability for the particular device.

Figure 3-1. System Block Diagram for SAM C20/C21



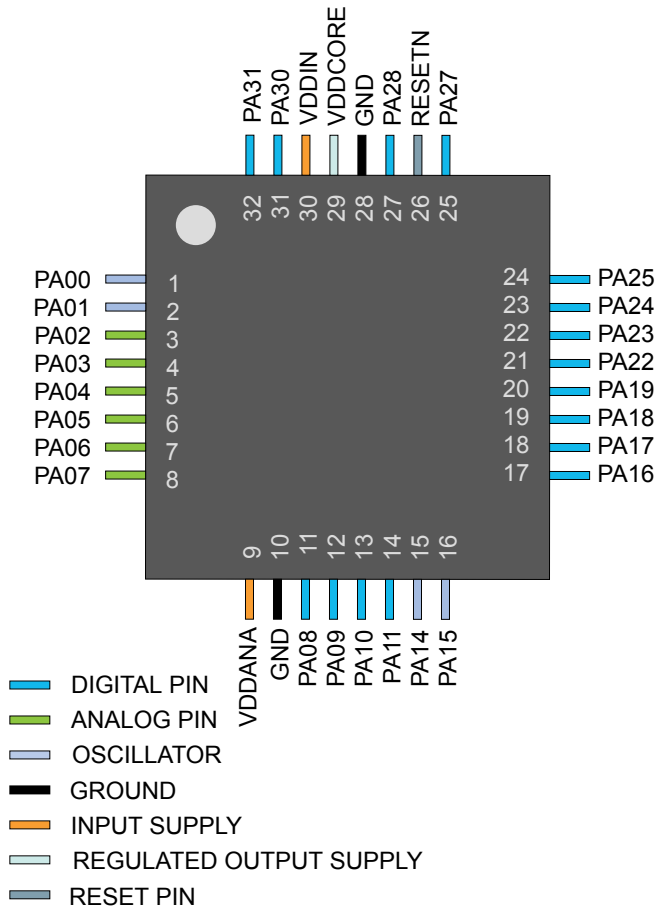
Related Links

- [TCC Configurations](#)
- [Multiplexed Signals](#)

4. Pinout

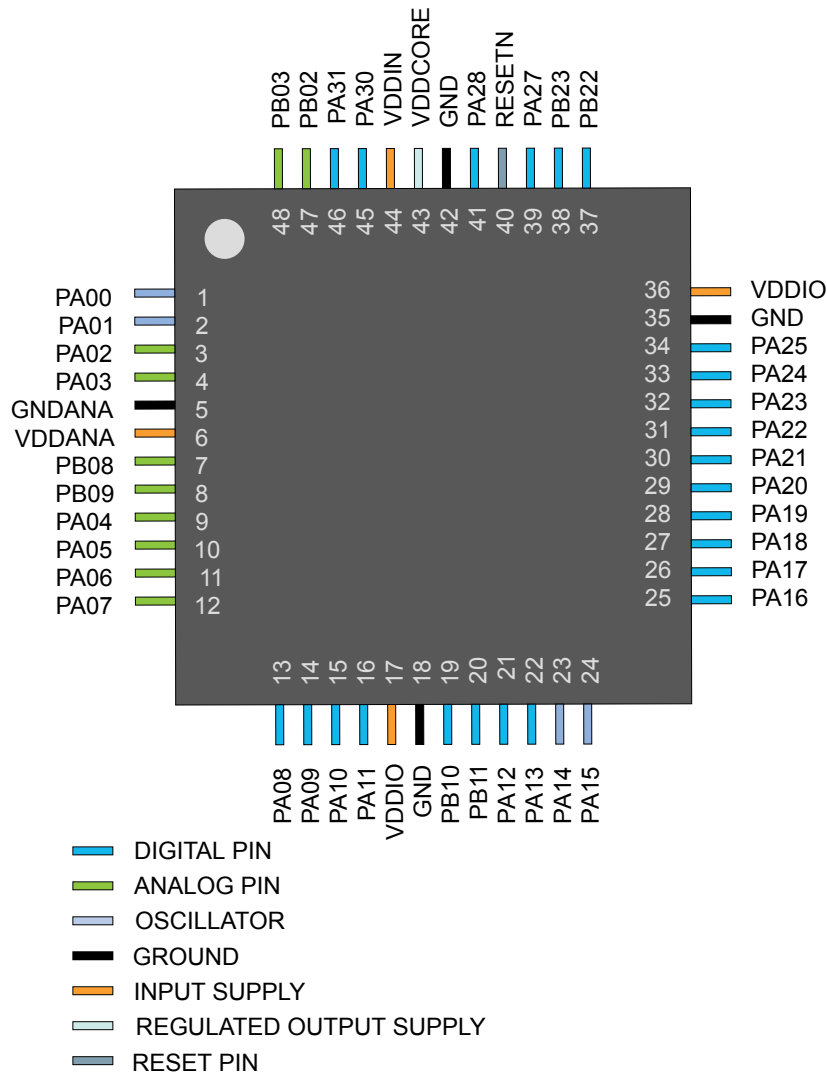
4.1 SAM C21E / SAM C20E

4.1.1 QFN32/TQFP32



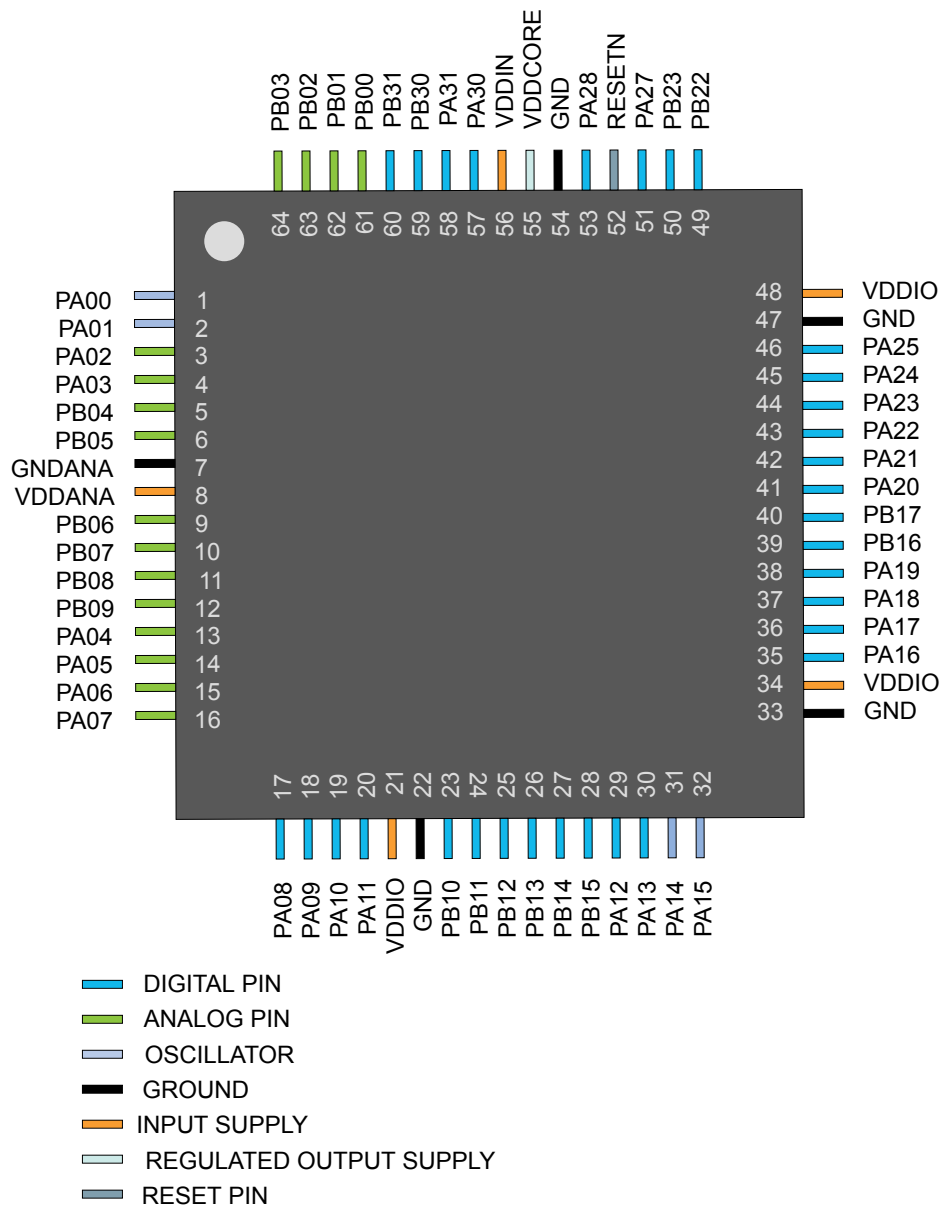
4.2 SAM C21G / SAM C20G

4.2.1 QFN48 / TQFP48

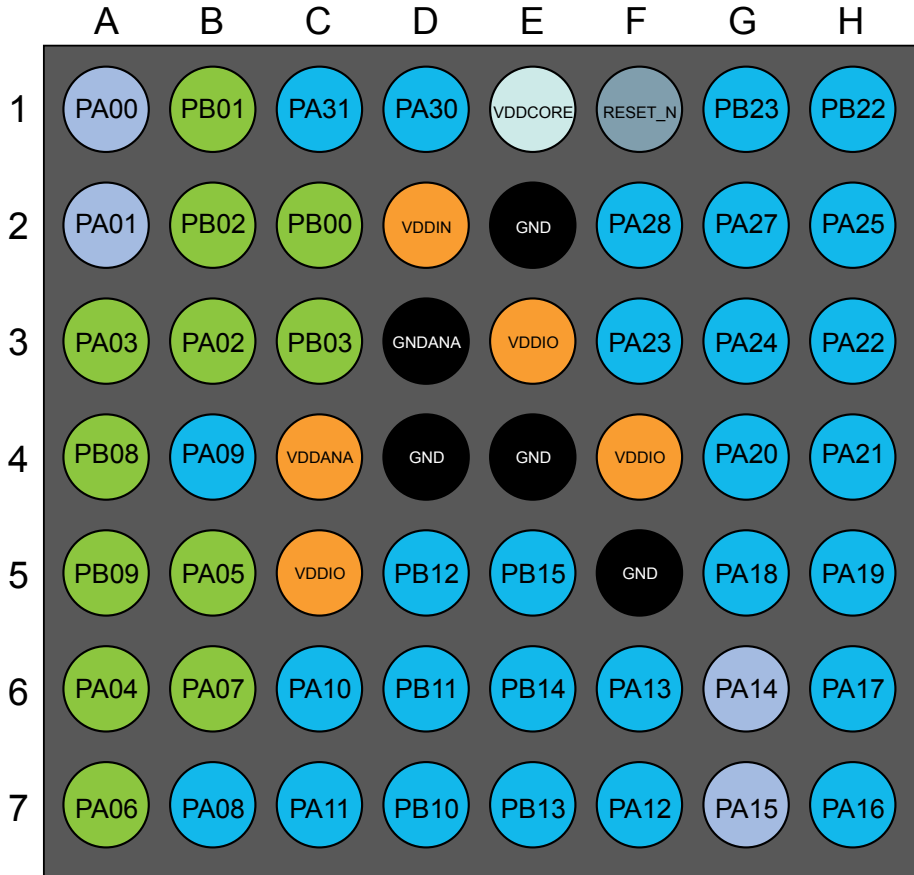


4.3 SAM C21J / SAM C20J

4.3.1 QFN64/TQFP64



4.3.2 WLCSP56



- █ DIGITAL PIN
- █ ANALOG PIN
- █ OSCILLATOR
- █ GROUND
- █ INPUT SUPPLY
- █ REGULATED OUTPUT SUPPLY
- █ RESET PIN