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SAMD5x/E5x Family Data Sheet

32-bit ARM® Cortex®-M4F MCUs with 1 Msps 12-bit ADC, QSPI, USB, Ethernet, and PTC

Features

Operating Conditions:

- -40°C to +85°C, DC to 120 MHz

Core: 120 MHz ARM® Cortex®-M4

- 403 CoreMark® at 120 MHz
- 4 KB combined instruction cache and data cache
- 8-zones Memory Protection Unit (MPU)
- Thumb®-2 instruction set
- Embedded Trace Module (ETM) with instruction trace stream
- Core Sight Embedded Trace Buffer (ETB)
- Trace Port Interface Unit (TPIU)
- Floating Point Unit (FPU)

Memories

- 1 MB/512 KB/256 KB in-system self-programmable Flash with:
  - Error Correction Code (ECC)
  - Dual bank with Read-While-Write (RWW) support
  - EEPROM hardware emulation
- 256/192/128 KB SRAM Main Memory
  - 128/96/64 KB of Error Correction Code (ECC) RAM option
- Up to 4 KB of Tightly Coupled Memory (TCM)
- Up to 8 KB additional SRAM
  - Can be retained in backup mode
- Eight 32-bit backup registers

System

- Power-on Reset (POR) and Brown-out detection (BOD)
- Internal and external clock options
- External Interrupt Controller (EIC)
- 16 external interrupts
- One non-maskable interrupt
- Two-pin Serial Wire Debug (SWD) programming, test, and debugging interface

Power Supply

- Idle, Standby, Hibernate, Backup, and Off sleep modes

- SleepWalking peripherals
- Battery backup support
- Embedded Buck/LDO regulator supporting on-the-fly selection

High-Performance Peripherals

- 32-channel Direct Memory Access Controller (DMAC)
  - Built-in CRC, with memory CRC generation/monitor hardware support
- Up to two SD(HC) Memory Card Interfaces (SDHC)
  - Up to 50 MHz operation
  - 4-bit or 1-bit interface
  - Compatibility with SD and SDHC memory card specification version 3.01
  - Compatibility with SDIO specification version 3.0
  - Compliant with JDEC specification, MMC memory cards V4.51
- One Quad I/O Serial Peripheral Interface (QSPI)
  - eXecute-In-Place (XIP) support
  - Dedicated AHB memory zone
- One Ethernet MAC (SAM E53 and SAM E54)
  - 10/100 Mbps in MII and RMII with dedicated DMA
  - IEEE 1588 Precision Time Protocol (PTP) support
  - IEEE 1588 Time Stamping Unit (TSU) support
  - IEEE802.3AZ energy efficiency support
  - Support for 802.1AS and 1588 precision clock synchronization protocol
  - Wake on LAN support
- Up to two Controller Area Network CAN (SAM E51 and SAM E54)
  - Support for CAN2.0 A/B and CAN-FD (ISO 11898-1:2015)
- One Full-Speed (12 Mbps) Universal Serial Bus (USB) 2.0 interface
  - Embedded host and device function
  - Eight endpoints
  - On-chip transceiver with integrated serial resistor

System Peripherals

- 32-channel Event System
- Up to eight Serial Communication Interfaces (SERCOM), each configurable to operate as either:
  - USART with full-duplex and single-wire half-duplex configuration
  - ISO7816
  - I^2C up to 3.4MHz
  - SPI
  - LIN master/slave
  - RS485
  - SPI inter-byte space
- Up to eight 16-bit Timers/Counters (TC) each configurable as:
  - 16-bit TC with two compare/capture channels
  - 8-bit TC with two compare/capture channels
  - 32-bit TC with two compare/capture channels, by using two TCs
- Two 24-bit Timer/Counters for Control (TCC), with extended functions:

  - Up to six compare channels with optional complementary output
  - Generation of synchronized pulse width modulation (PWM) pattern across port pins
  - Deterministic fault protection, fast decay and configurable dead-time between complementary output
  - Dithering that increase resolution with up to 5 bit and reduce quantization error
- Up to Three 16-bit Timer/Counters for Control (TCC), with extended functions:
  - Up to three compare channels with optional complementary output
- 32-bit Real Time Counter (RTC) with clock/calendar function
- Up to 4 wake-up pins with tamper detection and debouncing filter
- Watchdog Timer (WDT) with Window mode
- CRC-32 generator
- One two-channel Inter-IC Sound Interface (I2S)
- Position Decoder (PDEC)
- Frequency meter (FREQM)
- One Configurable Custom Logic (CCL)
- Dual 12-bit, 1 MSPS Analog-to-Digital Converter (ADC) with up to 16 channels each
  - Differential and single-ended input
  - Automatic offset and gain error compensation
  - Oversampling and decimation in hardware to support 13-, 14-, 15-, or 16-bit resolution
- Dual 12-bit, 1 MSPS Output Digital-to-Analog Converter (DAC)
- Two Analog Comparators (AC) with Window Compare function
- One temperature sensor
- Parallel Capture Controller (PCC)
  - Up to 14-bit parallel capture mode
- Peripheral Touch Controller (PTC)
  - Capacitive Touch buttons, sliders, and wheels
  - Wake-up on touch
  - Up to 32 self-capacitance, and up to 256 mutual-capacitance channels

Cryptography

- One Advanced Encryption System (AES) with 256-bit key length and up to 2 MB/s data rate
  - Five confidential modes of operation (ECB, CBC, CFB, OFB, CTR)
  - Supports counter with CBC-MAC mode
  - Galois Counter Mode (GCM)
- True Random Number Generator (TRNG)
- Public Key Cryptography Controller (PUKCC) and associated Classical Public Key Cryptography Library (PUKCL)
  - RSA, DSA
  - Elliptic Curves Cryptography (ECC) ECC GF(2n), ECC GF(p)
- Integrity Check Module (ICM) based on Secure Hash Algorithm (SHA1, SHA224, SHA256), DMA assisted

Oscillators

- 32.768 kHz crystal oscillator (XOSC32K)
  - Clock failure detection
- Up to two 8 MHz to 48 MHz crystal oscillator (XOSC)

  - Clock failure detection
- 32.768 kHz ultra low-power internal oscillator (OSCULP32K)
- 48 MHz Digital Frequency Locked Loop (DFLL48M)
- Two 48-200 MHz Fractional Digital Phased Locked Loop (FDPLL200M)

I/O

- Up to 99 programmable I/O pins

Packages

- 48-pin QFN
- 64-pin QFN, TQFP, WLCSP
- 100-pin TQFP
- 120-ball TFBGA
- 128-pin TQFP

Table of Contents

1. Configuration Summary

Table 1-1. SAM E53/E54 Family Features with Ethernet

Device	Program Memory (KB)	Data Memory (KB)	Pins	Packages	Peripherals																			Analog					Security				
					Ethernet Controller	CAN-FD	SERCOM	TC/Compare	TCC (24-bit/16-bit)	I2S	USB	QSPI	SDHC	DMA Channels	PCC (data size)	CCL	Position Decoder	RTC	WDT	Frequency Measurement	Event System (Channels)	External Interrupt Lines	I/O Pins	ADC (Channels ADC0/ADC1)	Analog Comparators (Channels)	DAC (Channels)	PTC (Mutual/Self-capacitance Channels)	Temperature Sensor	AES	TRNG	Public Key Cryptography (PUKCC)	Integrity Check Monitor	Tamper Pins
SAME53N20	1024	256	100	TQFP	Y	N	8	8/2	2/3	Y	Y	Y	2	32	14	4	Y	Y	Y	Y	32	16	81	16/12	4	2	256/32	Y	Y	Y	Y	Y	5
SAME53N19	512	192																															
SAME53J20	1024	256	64	TQFP, QFN			6	6/2					1		10								51	16/8									3
SAME53J19	512	192																															
SAME53J18	256	128																															
SAME54P20	1024	256	128 120	TQFP TFBGA		Y	8	8/2					2		14								99	16/16									5
SAME54P19	512	192	128 120	TQFP TFBGA																													
SAME54N20	1024	256	100	TQFP																			81	16/12									
SAME54N19	512	192																															

Table 1-2. SAM D51/E51 Family Features without Ethernet

Device	Program Memory (KB)	Data Memory (KB)	Pins	Packages	Peripherals																	Analog					Security				
					CAN-FD	SERCOM	TC/Compare	TCC (24-bit/16-bit)	I2S	USB	QSPI	SDHC	DMA Channels	PCC (data size)	CCL	Position Decoder	RTC	Frequency Measurement	Event System (Channels)	External Interrupt Lines	I/O Pins	ADC (Channels ADC0/ADC1)	Analog Comparators (Channels)	DAC (Channels)	PTC (Mutual/Self-capacitance Channels)	Temperature Sensor	AES	TRNG	Public Key Cryptography (PUKCC)	Integrity Check Monitor	Tamper Pins
SAMD51P20	1024	256	128 120	TQFP TFBGA	N	8	8/2	2/3	Y	Y	Y	2	32	14	4	Y	Y	Y	32	16	99	16/16	4	2	256/32	Y	Y	Y	Y	Y	5
SAMD51P19	512	192																															
SAMD51N20	1024	256	100	TQFP																	81	16/12									
SAMD51N19	512	192																															
SAMD51J20	1024	256	64	TQFP, QFN, WLCSP		6	6/2					1		10							51	16/8									3
SAMD51J19	512	192																															
SAMD51J18	256	128	64	TQFP, QFN																													
SAMD51G19	512	192	48	QFN			4/2	2/1	N			1		10							37	16/4			121/22						2
SAMD51G18	256	128																															
SAME51N20	1024	256	100	TQFP	Y	8	8/2	2/3	Y			2		14							81	16/12			256/32						5
SAME51N19	512	192																															
SAME51J20	1024	256	64	TQFP, QFN		6	6/2					1		10							51	16/8									3

Device	Program Memory (KB)	Data Memory (KB)	Pins	Packages	Peripherals																	Analog					Security				
					CAN-FD	SERCOM	TC/Compare	TCC (24-bit/16-bit)	I2S	USB	QSPI	SDHC	DMA Channels	PCC (data size)	CCL	Position Decoder	RTC	Frequency Measurement	Event System (Channels)	External Interrupt Lines	I/O Pins	ADC (Channels ADC0/ADC1)	Analog Comparators (Channels)	DAC (Channels)	PTC (Mutual/Self-capacitance Channels)	Temperature Sensor	AES	TRNG	Public Key Cryptography (PUKCC)	Integrity Check Monitor	Tamper Pins
SAME51J19	512	192																													
SAME51J18	256	128																													

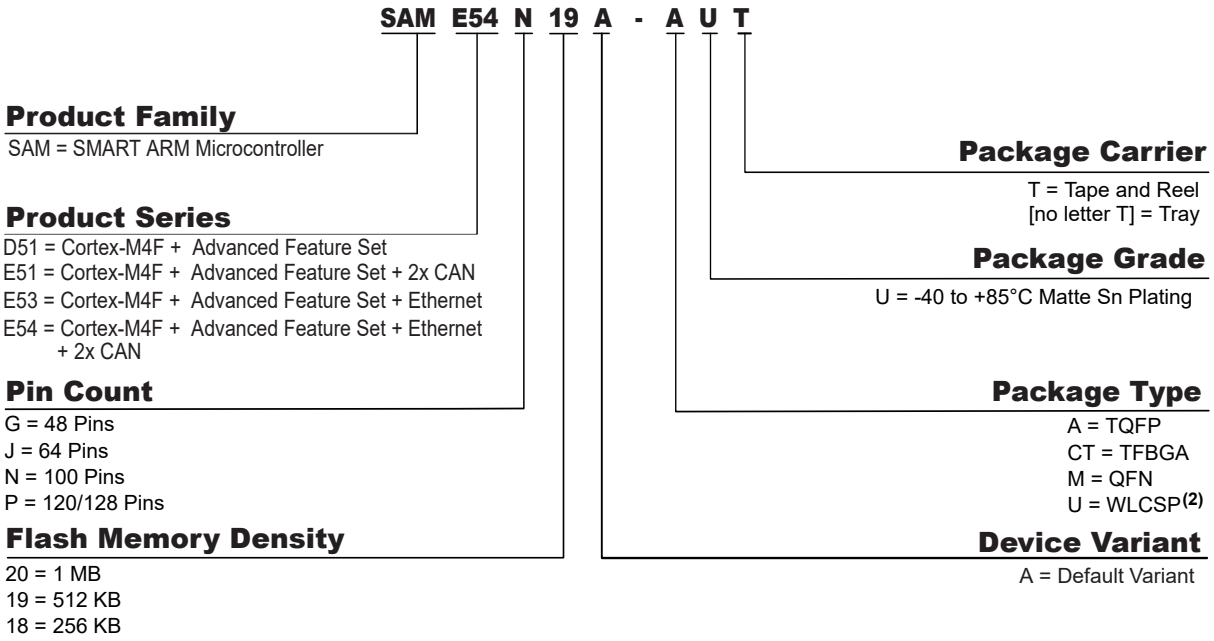
Related Links

6.2.6 SERCOM I2C Configurations

6.2.9 GPIO Clusters

2. Ordering Information

Figure 2-1. Composition of the Ordering Numbers(1)



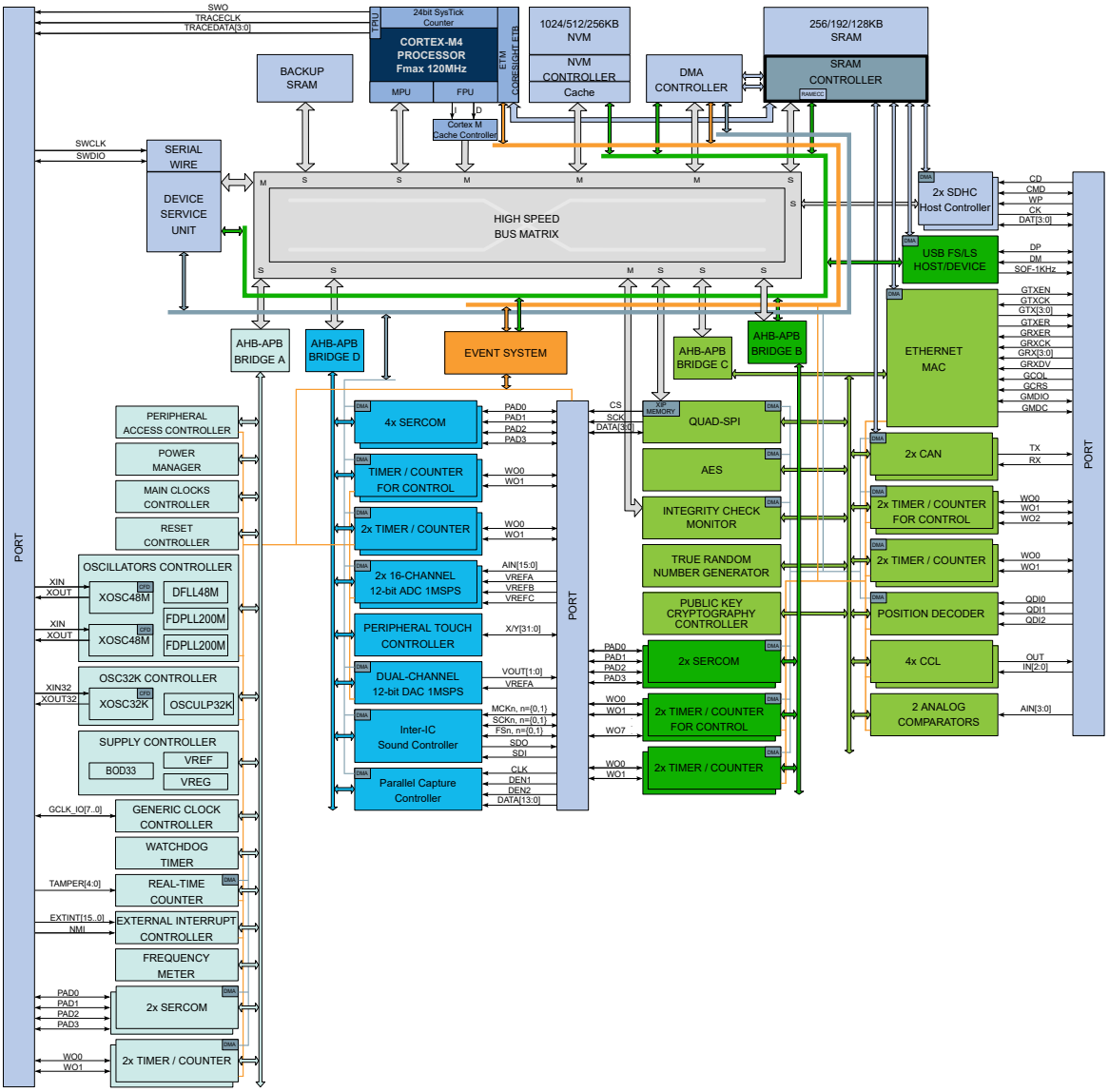
Note:

1. Not all combinations are valid. The available device part numbers are listed in Configuration Summary.
2. Devices in the WLCSP package include a factory programmed Bootloader. Please contact your local Microchip sales office for more information.

3. Block Diagram

The actual configuration may vary with device memory and number of pins. Refer to the Configuration Summary for details.

3.1 SAM D5x/E5x Block Diagram



Note:

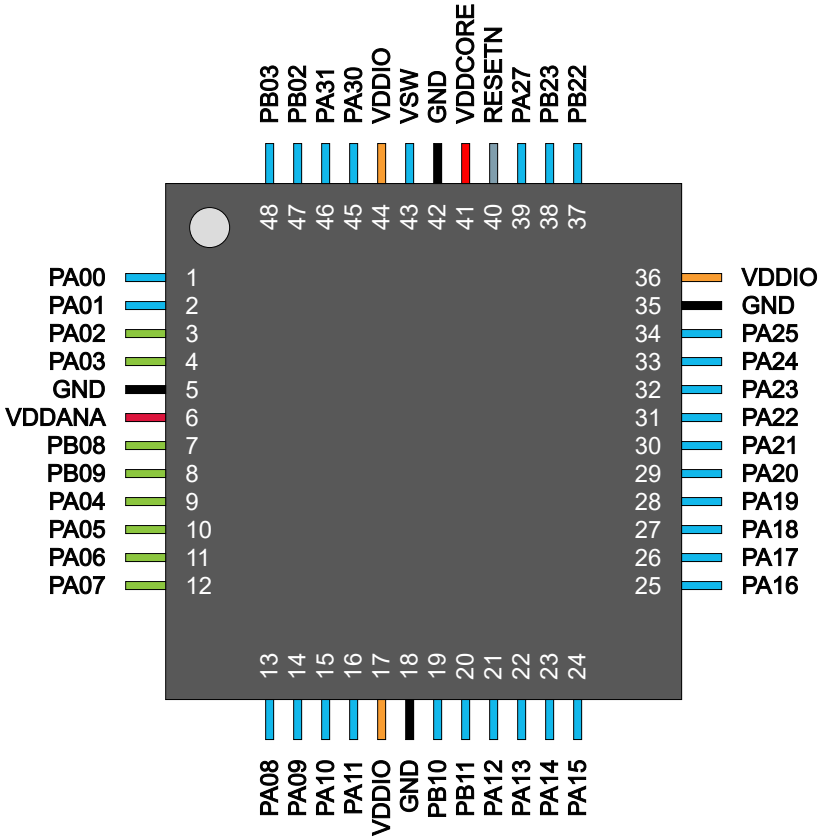
1. Some products have different number of SERCOM instances, Timer/Counter instances, PTC signals and ADC signals.
2. The block diagram is representing SAM E54P. Refer to the Configuration Summary for the configuration of a given device.

Related Links

1. Configuration Summary

4. Pinout

4.1 Pin Count 48 (G)



4.2 Pin Count 64 (J)

Figure 4-1. 64-Pin TQFP and QFN Package

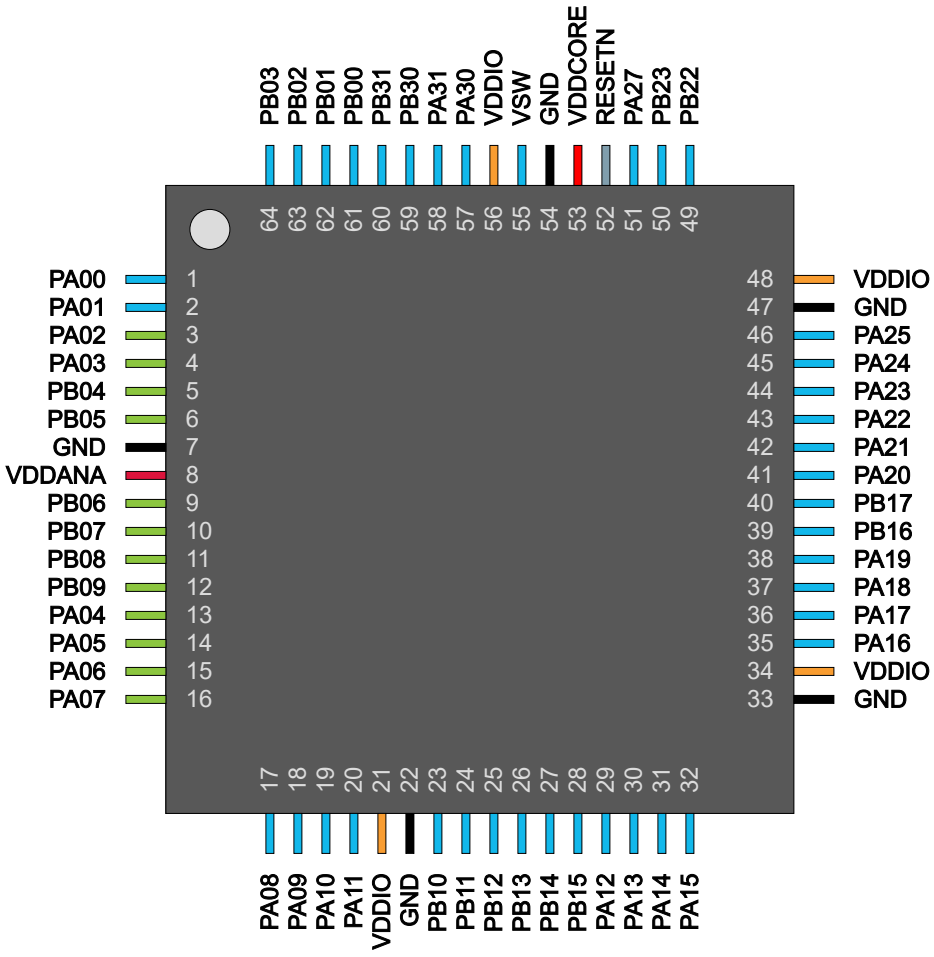
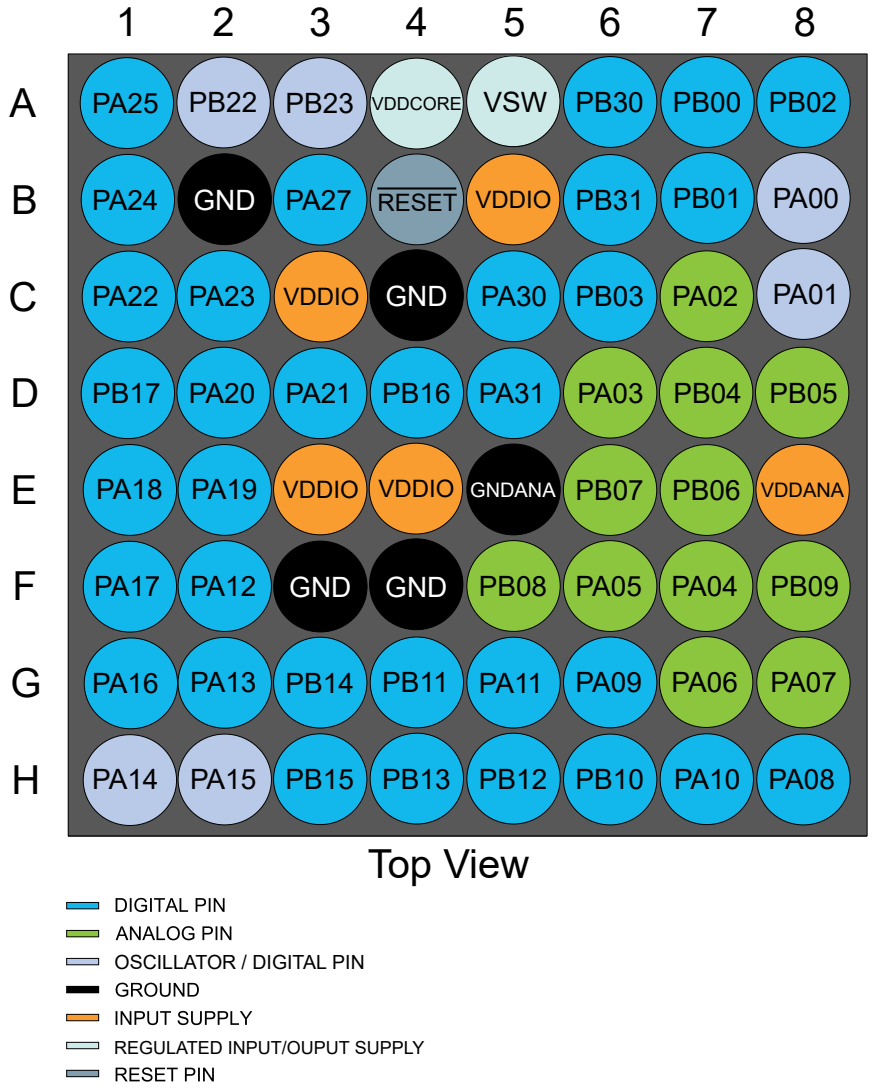


Figure 4-2. 64-Pin WLCSP Package



4.3 Pin Count 100 (N)