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SAM G53G / SAM G53N

Atmel | SMART ARM-based Flash MCU

DATASHEET

Description

The Atmel® | SMART SAM G53 is a series of Flash microcontrollers based on the high-performance 32-bit ARM® Cortex®-M4 RISC processor. It operates at a maximum speed of 48 MHz and features up to 512 Kbytes of Flash and 96 Kbytes of SRAM. The peripheral set includes one USART, two UARTs, three I^2C-bus interfaces (TWI), up to two SPIs, two three-channel general-purpose 16-bit timers, two I^2S controllers with two-way, one-channel pulse density modulation, one real-time timer (RTT) and one 8-channel 12-bit ADC.

The Atmel | SMART SAM G53 devices have two software-selectable low-power modes: Sleep and Wait. In Sleep mode, the processor is stopped while all other functions can be kept running. In Wait mode, all clocks and functions are stopped but some peripherals can be configured to wake up the system based on events, including partial asynchronous wake-up (SleepWalking™).

The Event System allows peripherals to receive, react to and send events in Active and Sleep modes without processor intervention.

A general-purpose microcontroller with the best ratio in terms of reduced power consumption, processing power and peripheral set, the SAM G53 series sustains a wide range of applications including consumer, industrial control, and PC peripherals.

The device operates from 1.62V to 3.6V and is available in a 49-ball WLCSP package and a 100-pin LQFP package.

Features

- Core
  - ARM Cortex-M4 up to 48 MHz
  - Memory Protection Unit (MPU)
  - DSP Instructions
  - Floating Point Unit (FPU)
  - Thumb®-2 instruction set
- Memories
  - 512 Kbytes embedded Flash
  - 96 Kbytes embedded SRAM
- System
  - Embedded voltage regulator for single-supply operation

  - Power-on reset (POR) and Watchdog for safe operation
  - Quartz or ceramic resonator oscillators: 3 to 20 MHz with clock failure detection and 32.768 kHz for RTT or device clock
  - High-precision 8/16/24 MHz factory-trimmed internal RC oscillator. In-application trimming access for frequency adjustment
  - Slow clock internal RC oscillator as permanent Low-power mode device clock
  - PLL range from 24 MHz to 48 MHz for device clock
  - 28 peripheral DMA (PDC) channels
  - 256-bit General-Purpose Registers (GPBR)
  - 16 external interrupt lines
- Power consumption in Active mode
  - 102 µA/MHz running Fibonacci in SRAM
- Low power modes (typical value)
  - Wait mode down to 8 µA
  - Wake-up time less than 5 µs
  - Asynchronous partial wake-up (SleepWalking™) on UART and TWI
- Peripherals
  - One USART with SPI mode
  - Two Inter-IC Sound Controllers (I^2S)
  - Two-way one-channel Pulse Density Modulation (PDM) (interfaces up to two microphones in PDM mode)
  - Two UARTs
  - Three Two-Wire Interface (TWI) modules featuring two TWI masters and one high-speed TWI slave
  - One fast SPI at up to 24Mbit/s
  - Two three-channel 16-bit Timer/Counters (TC) with Capture, Waveform, Compare and PWM modes
  - One 32-bit Real-Time Timer (RTT)
- I/O
  - Up to 38 controllable I/O lines with external interrupt capability (edge or level sensitivity), debouncing, glitch filtering and on-die series resistor termination. Individually programmable open-drain, pull-up and pull-down resistor and synchronous output
- Analog
  - One 8-channel ADC, resolution up to 12 bits, sampling rate up to 800 kSps
- Package
  - 49-ball WLCSP
  - 100-pin LQFP, 14 x 14 mm, pitch 0.5 mm
- Temperature operating range
  - Industrial (-40 °C to +85 °C)

1. Configuration Summary

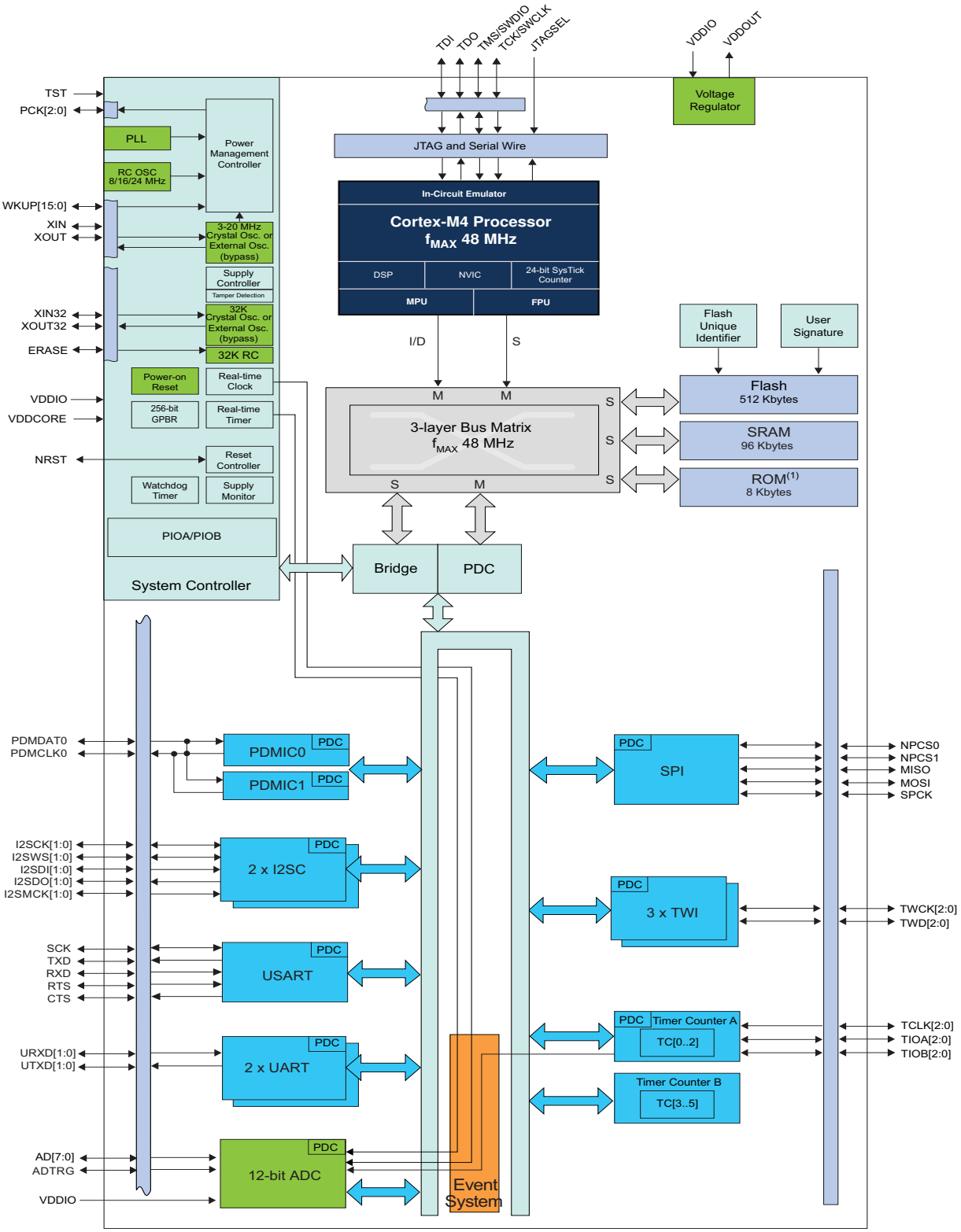
Table 1-1 summarizes the SAM G53 device configurations.

Table 1-1. Configuration Summary

Feature	SAM G53G19	SAM G53N19
Flash	512 Kbytes	512 Kbytes
SRAM	96 Kbytes	96 Kbytes
Package	WLCSP49	LQFP100
Number of PIOs	38	38
Event System	Yes	Yes
12-bit ADC	8 channels Performance: 800 KSps at 10-bit resolution 200 KSps at 11-bit resolution 50 KSps at 12-bit resolution	8 channels Performance 800 KSps at 10-bit resolution 200 KSps at 11-bit resolution 50 KSps at 12-bit resolution
16-bit Timer	6 channels (3 external channels)	6 channels (3 external channels)
I2SC/PDM	2 / 1-channel 2-way	2 / 1-channel 2-way
PDC Channels	28	28
USART/UART	1/2	1/2
SPI	1	1
TWI	2 masters at 400Kbits/s and 1 slave at 3.4Mbit/s	2 masters 400Kbits/s and 1 slave 3.4Mbit/s

2. Block Diagram

Figure 2-1. SAM G53 Block Diagram



Note: 1. The ROM is reserved for future use.

3. Signal Description

Table 3-1 provides details on the signal names classified by peripheral.

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Power Supplies					
VDDIO	Peripheral I/O Lines, Voltage Regulator, ADC Power Supply	Power	–	–	1.62V to 3.6V
VDDOUT	Voltage Regulator Output	Power	–	–	–
VDDCORE	Core Chip Power Supply	Power	–	–	Connected externally to VDDOUT
GND	Ground	Ground	–	–	–
Clocks, Oscillators and PLLs					
XIN	Main Oscillator Input (Bypass mode)	Input	–	VDDIO	Reset state: - PIO input - Internal pull-up disabled - Schmitt Trigger enabled
XOUT	Main Oscillator Output	Output	–	–	
XIN32	Slow Clock Oscillator Input (Bypass mode)	Input	–	VDDIO	
XOUT32	Slow Clock Oscillator Output	Output	–	–	
PCK0 - PCK2	Programmable Clock Output	Output	–	–	Reset state: - PIO input - Internal pull-up enabled - Schmitt Trigger enabled
ICE and JTAG					
TCK	Test Clock	Input	–	VDDIO	No pull-up resistor
TDI	Test Data In	Input	–	VDDIO	No pull-up resistor
TDO	Test Data Out	Output	–	VDDIO	–
TRACESWO	Trace Asynchronous Data Out	Output	–	VDDIO	–
SWDIO	Serial Wire Input/Output	I/O	–	VDDIO	–
SWCLK	Serial Wire Clock	Input	–	VDDIO	–
TMS	Test Mode Select	Input	–	VDDIO	No pull-up resistor
JTAGSEL	JTAG Selection	Input	High	VDDIO	Pull-down resistor
Flash Memory					
ERASE	Flash and NVM Configuration Bits Erase Command	Input	High	VDDIO	Pull-down (15 kΩ) resistor

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Reset/Test					
NRST	Microcontroller Reset	I/O	Low	VDDIO	Pull-up resistor
TST	Test Mode Select	Input	–	VDDIO	Pull-down resistor
Universal Ansynchronous Receiver Transceiver - UARTx					
URXDx	UART Receive Data	Input	–	–	–
UTXDx	UART Transmit Data	Output	–	–	–
PIO Controller - PIOA - PIOB					
PA0 - PA24	Parallel I/O Controller A	I/O	–	VDDIO	Pulled-up input at reset. No pull-down for PA3/PA4/PA14.
PB0 - PB12	Parallel I/O Controller B	I/O	–	VDDIO	Pulled-up input at reset
Wake-up Pins					
WKUP 0-15	Wake-up Pin / External Interrupt	I/O	–	VDDIO	Wake-up pins are used also as External Interrupt
Universal Synchronous Asynchronous Receiver Transmitter USART					
SCK	USART Serial Clock	I/O	–	–	–
TXD	USART Transmit Data	I/O	–	–	–
RXD	USART Receive Data	Input	–	–	–
RTS	USART Request To Send	Output	–	–	–
CTS	USART Clear To Send	Input	–	–	–
Timer/Counter - TCx					
TCLKx	TC Channel x External Clock Input	Input	–	–	–
TIOAx	TC Channel x I/O Line A	I/O	–	–	–
TIOBx	TC Channel x I/O Line B	I/O	–	–	–
Serial Peripheral Interface - SPI					
MISO	Master In Slave Out	I/O	–	–	–
MOSI	Master Out Slave In	I/O	–	–	–
SPCK	SPI Serial Clock	I/O	–	–	High-speed pad
NPCS0	SPI Peripheral Chip Select 0	I/O	Low	–	–
NPCS1	SPI Peripheral Chip Select 1	Output	Low	–	–

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Two-Wire Interface- TWIx					
TWDx	TWIx Two-wire Serial Data	I/O	–	–	High-speed pad for TWD0
TWCKx	TWIx Two-wire Serial Clock	I/O	–	–	High-speed pad for TWDCK0
10-bit Analog-to-Digital Converter - ADCC					
AD0 - AD7	Analog Inputs	Analog	–	–	–
ADTRG	ADC Trigger	Input	–	–	–
Inter-IC Sound Controller - I2SCx					
I2SMCKx	Master Clock	Output	–	–	–
I2SCKx	Serial Clock	I/O	–	–	–
I2SWSx	I2S Word Select	I/O	–	–	–
I2SDIx	Serial Data Input	Input	–	–	–
I2SDOx	Serial Data Output	Output	–	–	–
PDMCLK0	Pulse Density Modulation Clock	Output	–	–	–
PDMDAT0	Pulse Density Modulation Data	Input	–	–	–

4. Package and Pinout

Table 4-1. SAM G53 Packages

Device	Package
SAM G53G19	WLCSP49
SAM G53N19	LQFP100

4.1 49-ball WLCSP Pinout

Table 4-2. SAM G53G19 49-ball WLCSP Pinout

A1	PA9	C1	VDDCORE	E1	PB2/AD6	G1	VDDIO
A2	GND	C2	PA11	E2	PB0/AD4	G2	VDDOUT
A3	PA24	C3	PA12	E3	PA18/AD1	G3	GND
A4	PB8/XOUT	C4	PB6	E4	PA14	G4	VDDIO
A5	PB9/XIN	C5	PA4	E5	PA10	G5	PA22
A6	PB4	C6	PA3	E6	TST	G6	PA15
A7	VDDIO	C7	PA0	E7	PA7/XIN32	G7	PA6
B1	PB11	D1	PA13	F1	PA20/AD3		
B2	PB5	D2	PB3/AD7	F2	PA19/AD2		
B3	PB7	D3	PB1/AD5	F3	PA17/AD0		
B4	PA2	D4	PB10	F4	PA21		
B5	JTAGSEL	D5	PA1	F5	PA23		
B6	NRST	D6	PA5	F6	PA16		
B7	PB12	D7	VDDCORE	F7	PA8/XOUT32		

4.2 100-lead LQFP Pinout

Table 4-3. SAM G53N19 100-pin LQFP Pinout

1	NC	26	NC	51	NC	76	NC
2	NC	27	NC	52	NC	77	NC
3	NC	28	PA6	53	PA17	78	NC
4	NC	29	VDDIO	54	PA18	79	PA9
5	VDDIO	30	PA16	55	PA19	80	PB5
6	VDDIO	31	PA15	56	PA20	81	GND
7	NRST	32	PA23	57	PB0	82	GND
8	PB12	33	NC	58	PB1	83	GND
9	PA4	34	NC	59	PB2	84	PB6
10	PA3	35	PA22	60	PB3	85	PB7
11	PA0	36	PA21	61	VDDIO	86	PA24
12	PA1	37	VDDIO	62	PA14	87	PB8
13	PA5	38	VDDIO	63	PA13	88	PB9
14	VDDIO	39	GND	64	PA12	89	VDDIO
15	VDDCORE	40	GND	65	PA11	90	PA2
16	VDDCORE	41	GND	66	VDDCORE	91	PB4
17	TEST	42	GND	67	VDDCORE	92	NC
18	PA7	43	GND	68	PB10	93	JTAGSEL
19	PA8	44	VDDOUT	69	PB11	94	VDDIO
20	GND	45	VDDOUT	70	GND	95	VDDIO
21	NC	46	VDDIO	71	GND	96	NC
22	NC	47	VDDIO	72	PA10	97	NC
23	NC	48	VDDIO	73	NC	98	NC
24	NC	49	NC	74	NC	99	NC
25	NC	50	NC	75	NC	100	NC

5. Power Considerations

5.1 Power Supplies

The SAM G53 has several types of power supply pins:

- VDDCORE pins: Power the core, including the processor, the embedded memories and the peripherals. VDDCORE must be connected to VDDOUT.
- VDDIO pins: Power the peripheral I/O lines, voltage regulator and ADC; voltage ranges from 1.62V to 3.6V.

The ground pins GND are common to VDDCORE and VDDIO.

5.2 Voltage Regulator

The SAM G53 embeds a core voltage regulator that is managed by the Supply Controller and that supplies the Cortex-M4 core, internal memories (SRAM and Flash logic) and the peripherals. An internal adaptative biasing adjusts the regulator quiescent current depending on the required load current.

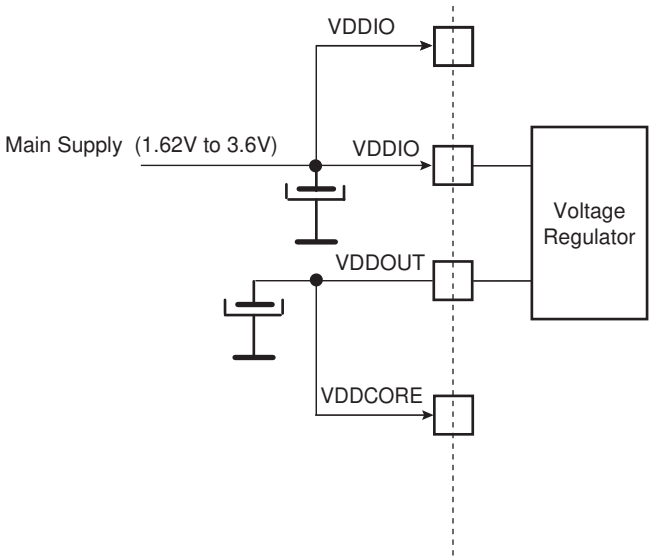
For adequate input and output power supply decoupling/bypassing, refer to Table 37-4 “VDDCORE Voltage Regulator Characteristics” in the Electrical Characteristics section of the datasheet.

5.3 Typical Powering Schematics

The SAM G53 supports a 1.62V to 3.6V single supply mode. The internal regulator input is connected to the source and its output feeds VDDCORE. Power schematics are illustrated in Figure 5-1.

To achieve the system performance levels, the internal regulator must be used.

Figure 5-1. Single Supply



5.4 Functional Modes

5.4.1 Active Mode

Active mode is the normal running mode with the core clock running from the fast RC oscillator, the main crystal oscillator or the PLL. The Power Management Controller can be used to adapt the frequency and to disable the peripheral clocks.

5.4.2 Wait Mode

Wait mode allows the device to achieve very low power consumption levels while remaining in a powered state with a wake-up time of less than 5 µs. Current consumption in Wait mode is typically less than 8 µA (total current consumption). In Wait mode, the clocks of the core, the peripherals and memories are stopped. However, power supplies are maintained to ensure memory and CPU context retention.

The wake-up time of 5 µs is achieved when entry into and exit from Wait mode are performed in internal SRAM. The wake-up time increases to 70 µs if entry into Wake-up mode is performed in internal Flash.

Wait mode is entered using either the WAITMODE bit in the PMC Clock Generator Main Oscillator register (CKGR_MOR) or the Wait for Event (WFE) instruction. Detailed sequences are provided below.

Note that the WFE instruction can add complexity in application state machines due to the fact that the WFE instruction goes along with an event flag of the Cortex core (cannot be managed by the software application). The event flag can be set by interrupts, a debug event or an event signal from another processor. Since an interrupt can take place just before the execution of WFE, WFE takes into account events that happened in the past. As a result, WFE prevents the device from entering Wait mode if an interrupt event has occurred. To work around this complexity, follow the sequence using the WAITMODE bit described below.

The Cortex-M4 processor is able to handle external or internal events in order to wake up the core. This is done by configuring the external lines WKUP0–15 as fast start-up wake-up pins (refer to Section 5.5 “Fast Start-up”) or the RTT and RTC alarms for internal events.

To enter Wait mode using the WAITMODE bit:

1. Select the 8/16/24 MHz fast RC oscillator as the Main Clock. If frequency of 24 MHz is selected and the code is running from the SRAM, wake-up time is less than 5 µs.
2. Program the FLPM field in the PMC Fast Startup Mode Register (PMC_FSMR)(1).
3. Set the number of Flash wait states to 0 by writing a zero to the FWS field in the EEFC Flash Mode Register (EEFC_MR).
4. Write a one to the WAITMODE bit in the PMC Clock Generator Main Oscillator Register (CKGR_MOR).
5. Wait for MCKRDY = 1 in the PMC Status Register (PMC_SR).

To enter Wait mode using the WFE instruction:

1. Select the 8/16/24 MHz fast RC oscillator as the Main Clock. If 24 MHz is selected and the code is running on the SRAM, wake-up time is less than 5 µs.
2. Program the FLPM field in the PMC Fast Startup Mode Register (PMC_FSMR)(1).
3. Set the number of Flash wait states to 0 by writing a zero to the FWS field in the EEFC Flash Mode Register (EEFC_MR).
4. Write a one to the LPM bit in the PMC Fast Startup Mode Register (PMC_FSMR).
5. Ensure that the SLEEPDEEP bit in the System Control Register (SCB_SCR) is cleared.
6. Execute the Wait For Event (WFE) instruction of the processor.

Note: 1. Depending on the value of the field FLPM, the Flash enters three different modes:
- FLPM = 0: Flash in Stand-by mode (low power consumption levels)
- FLPM = 1: Flash in Deep power-down mode (extra low power consumption levels)
- FLPM = 2: Flash in Idle mode. Memory ready for Read access.

5.4.3 Sleep Mode

In Sleep mode, power consumption of the device versus response time is optimized. Only the core clock is stopped. The peripheral clocks can be enabled. The current consumption in Sleep mode is application-dependent.

Sleep mode is entered via Wait for Interrupt (WFI) instructions.

The processor can be awakened from an interrupt if the WFI instruction of the Cortex-M4 is used.

5.4.4 Low-Power Mode Configuration Summary

Table 5-1 summarizes the power consumption, wake-up time and system state in low-power modes.

Table 5-1. Low-Power Mode Configuration Summary

Mode	SUPC 32 kHz Oscillator RTT POR Regulator	POR Supply Monitor on VDDIO	RAM Power Switch	Core Memory Peripherals	Mode Entry	Potential Wake-up Sources	Core at Wake-up	PIO State while in Low-Power Mode	PIO State at Wake-up	Consumption (2) (3)	Wake-up Time (1)
Wait Mode with Flash in Deep-power-down mode	ON	OFF	All RAM powered	Powered (Not clocked)	FLPM = 1 + WAITMODE = 1 or SLEEPDEEP = 0 +FLPM = 1 + LPM = 1 + WFE	Any event from: Fast startup through WKUP0–15 pins RTT alarm RTC alarm	Clocked back	Previous state saved	Unchanged	<12 µA (5)	< 5 µs (4)
			64 Kbytes RAM powered							<10 µA (5)	< 5 µs (4)
			32 Kbytes RAM powered							<8 µA (5)	< 5 µs (4)
Sleep Mode	ON	ON	Powered	Powered (Not clocked)	WFI + SLEEPDEEP = 0 + LPM = 0	Entry mode =WFI interrupt only; any enabled interrupt	Clocked back	Previous state saved	Unchanged	(6)	–

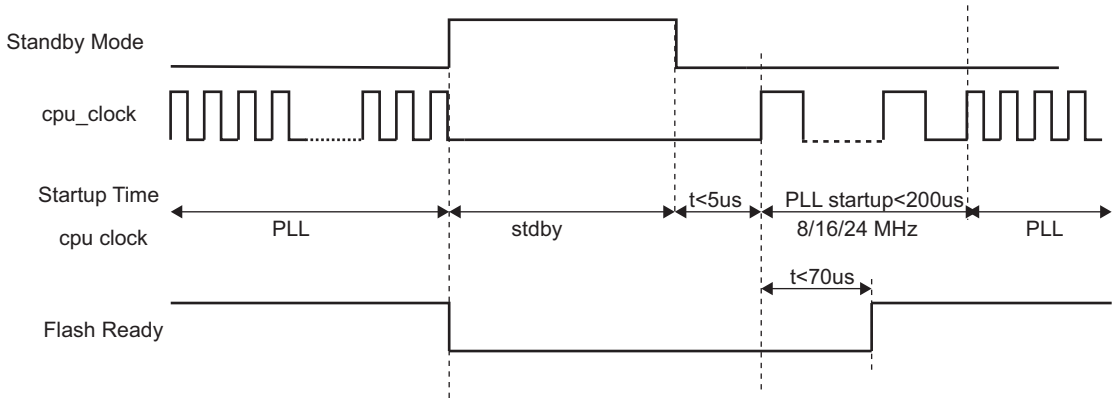
Notes:
1. When considering wake-up time, the time required to start the PLL is not taken into account. Once started, the device works with the 8/16/24 MHz Fast RC oscillator. The user has to add the PLL start-up time if it is needed in the system. The wake-up time is defined as the time taken for wake up until the first instruction is fetched.
2. The external loads on PIOs are not taken into account in the calculation.
3. BOD current consumption is not included.
4. Wake-up from RAM if 24 MHz fast RC oscillator is selected.
5. Values give are typical values.
6. Refer to the section “Power Consumption” in the “Electrical Characteristics”.

5.5 Fast Start-up

The SAM G53 allows the processor to restart in a few microseconds while the processor is in Wait mode. A fast start-up can occur upon detection of a low level on one of the 18 sources of wake-up (2 internal and 16 external).

The fast restart circuitry is fully asynchronous and provides a fast start-up signal to the Power Management Controller. As soon as the fast start-up signal is asserted, the PMC restarts from the last fast RC selected (the embedded 24 MHz fast RC oscillator), switches the master clock on the last clock of RC oscillator and reenables the processor clock. At the wake-up of the Wait mode, the code is executed in the SRAM.

Figure 5-2. Start-up Sequence



Reset signals resynchronized on specific clocks

6. Architecture

6.1 Peripheral DMA Controller

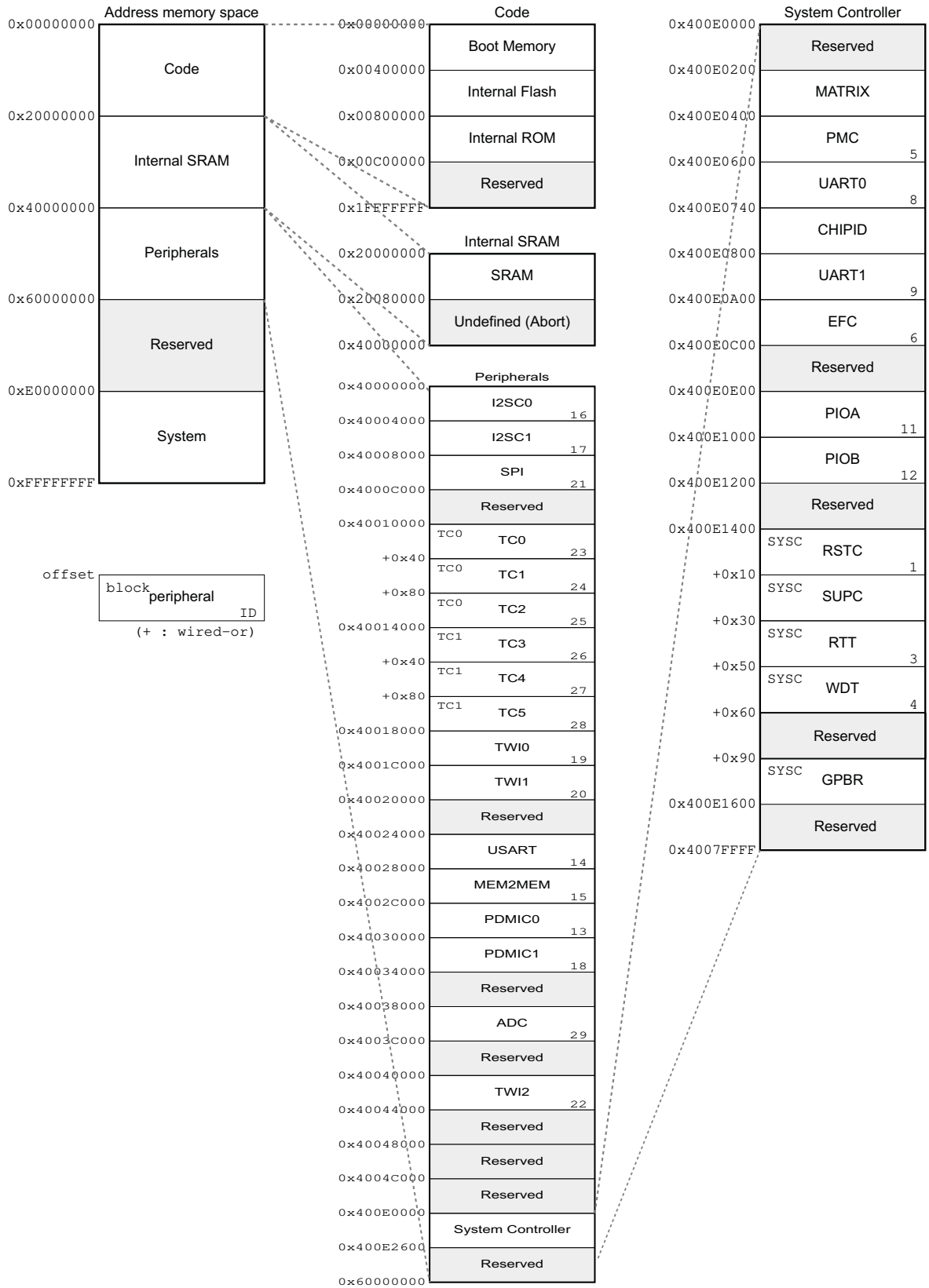
The Peripheral DMA Controller handles transfer requests from the channel. Priorities are defined in Table 6-1, with Channel Number 0 as highest priority.

Table 6-1. Peripheral DMA Controller

Instance Name	Channel T/R	Channel Number
MEM2MEM	Transmit	27
SPI	Transmit	26
TWI1	Transmit	25
TWI2	Transmit	24
UART0	Transmit	23
UART1	Transmit	22
USART	Transmit	21
I2SC1	Transmit	19, 20
I2SC0	Transmit	17, 18
TWI0	Transmit	16
MEM2MEM	Receive	15
TC0::TC0	Receive	14
SPI	Receive	13
TWI1	Receive	12
TWI2	Receive	11
UART0	Receive	10
UART1	Receive	9
USART	Receive	8
PDMIC1	Receive	7
PDMIC0	Receive	6
I2SC1	Receive	4, 5
I2SC0	Receive	2, 3
ADC	Receive	1
TWI0	Receive	0

7. Product Mapping

Figure 7-1. SAM G53 Product Mapping



8. Boot Loader

The SAM G53 devices ship with a factory-programmed boot loader in Flash. The Flash loader downloads code either through the SPI or through the TWI0.

The Boot loader mode is entered automatically on power-up if no valid firmware is detected in the Flash. A valid firmware is detected by performing a CRC on the content of the Flash. If the CRC is correct, the application is started. Otherwise, the Boot loader mode is entered.

Alternatively, the Boot loader mode can be forced by applying low pulses on the NRST line. The NRST should be asserted 10 times for a minimum of 1 µs at an interval less than 50 ms. When the boot loader detects this sequence, it asserts the pin PA01 (NCHG) low as an acknowledge.

The Boot loader mode initializes the TWI0 in Slave Mode with the I2C address 0x26 and the SPI in Slave Mode, 8-bit data length, SPI Mode 1.

Table 8-1 provides information on the pins used by the boot loader.

Table 8-1. Boot Loader Pin Description

Pin Name	Function	Boot Loader Use	Description
PA01	NCHG	Driven at 0 or pulled up	Boot loader handshake
PA03	TWD	Open drain input/output	TWI/I2C data line
PA04	TWCK	Open drain input/output	TWI/I2C clock
PA11	NPCS0/NSS	Input	NSS, SPI slave select
PA12	MISO	Push-pull output	SPI master in slave out
PA13	MOSI	Input	SPI master out slave in
PA14	SPCK	Input	SPI clock

For further details on boot loader operations, refer to the application note AT09002 – Atmel SAM I²C - SPI Bootloader" on www.atmel.com.

9. Memories

9.1 Internal SRAM

The SAM G53 embeds a total of 96 Kbytes of high-speed SRAM.

The SRAM is accessible over the Cortex-M4 system bus at address 0x2000 0000.

The SRAM is in the bit band region. The bit band alias region is from 0x2200 0000 and 0x23FF FFFF.

The SRAM is composed of three blocks of 32 Kbytes. The second and third blocks have a power switch. Each power switch controls the supply of the SRAM block to save power. The control of the power switch (PSWITCHx) is in the SUPC_MR register.

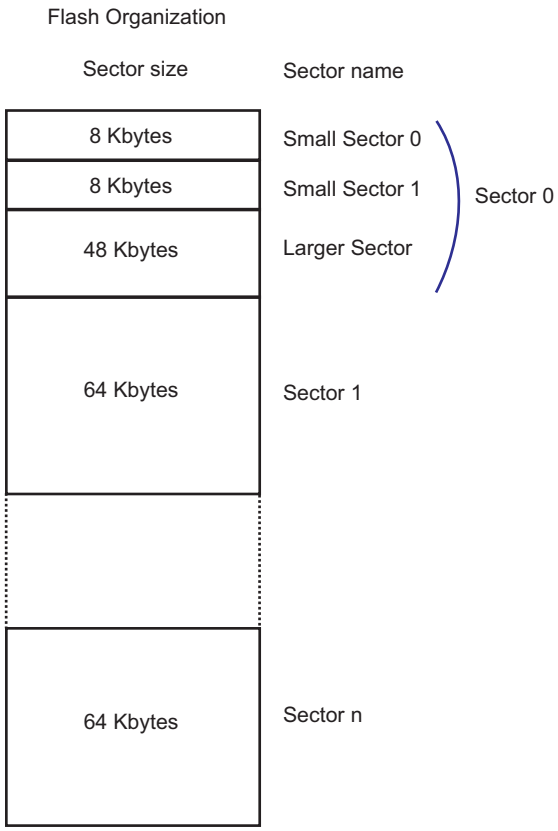
9.2 Embedded Flash

9.2.1 Flash Overview

The memory is organized in sectors. Each sector comprises 64 Kbytes. The first sector of 64 Kbytes is divided into three smaller sectors.

The three smaller sectors are comprised of two sectors of 8 Kbytes and one sector of 48 Kbytes. Refer to Figure 9-1.

Figure 9-1. Global Flash Organization



Each sector is organized in pages of 512 bytes.

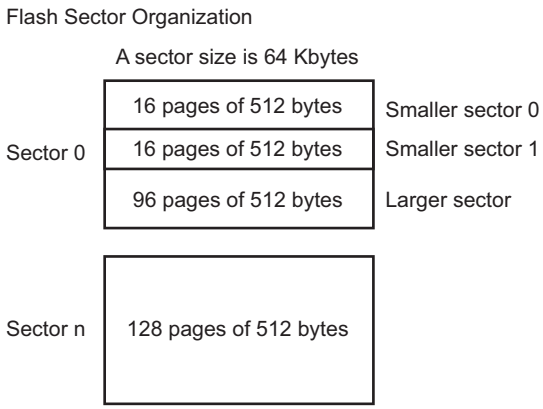
For sector 0:

- The smaller sector 0 has 16 pages of 512 bytes.
- The smaller sector 1 has 16 pages of 512 bytes.
- The larger sector has 96 pages of 512 bytes.

From sector 1 to n:

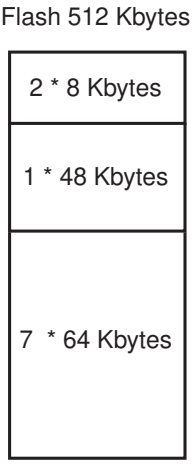
- The rest of the array is composed of 64 Kbytes sectors of 128 pages of 512 bytes each. Refer to Figure 9-2.

Figure 9-2. Flash Sector Organization



The SAM G53 Flash size is 512 Kbytes. Refer to Figure 9-3 for the organization of the Flash.

Figure 9-3. Flash Size



The following erase commands can be used depending on the sector size:

- 8 Kbyte small sector
  - Erase and write page(EWP)
  - Erase and write page and lock (EWPL)
  - Erase sector (ES) with FARG set to a page number in the sector to erase
  - Erase pages (EPA) with FARG [1:0] = 0 to erase four pages or FARG [1:0] = 1 to erase eight pages. FARG [1:0] = 2 and FARG [1:0] = 3 must not be used.

- 48 Kbyte and 64 Kbyte sectors
  - One block of 8 pages inside any sector, with the command Erase pages (EPA) with FARG[1:0] = 1
  - One block of 16 pages inside any sector, with the command Erase pages (EPA) and FARG[1:0] = 2
  - One block of 32 pages inside any sector, with the command Erase pages (EPA) and FARG[1:0] = 3
  - One sector with the command Erase sector (ES) and FARG set to a page number in the sector to erase
- Entire memory plane
  - The entire Flash, with the command Erase all (EA)

The memory has one additional reprogrammable page that can be used as page signature by the user. It is accessible through specific modes, for erase, write and read operations. Erase pin assertion will not erase the user signature page.

9.2.2 Enhanced Embedded Flash Controller

The Enhanced Embedded Flash Controller manages accesses performed by the masters of the system. It enables reading the Flash and writing the write buffer. It also contains a User Interface, mapped on the APB.

The Enhanced Embedded Flash Controller ensures the interface of the Flash block.

It manages the programming, erasing, locking and unlocking sequences of the Flash using a full set of commands.

One of the commands returns the embedded Flash descriptor definition that informs the system about the Flash organization, thus making the software generic.

9.2.3 Flash Speed

The user must set the number of wait states depending on the frequency used:

For more details, refer to the section “AC Characteristics” in the “Electrical Characteristics”.

9.2.4 Lock Regions

Several lock bits are used to protect write and erase operations on lock regions. A lock region is composed of several consecutive pages, and each lock region has its associated lock bit.

Table 9-1. Lock Bit Number

Product	Number of Lock Bits	Lock Region Size
SAM G53	64	8 Kbytes

If the erase or program command of a locked region occurs, the command is aborted and the EEFC triggers an interrupt.

The lock bits are software programmable through the EEFC User Interface. The command “Set Lock Bit” enables the protection. The command “Clear Lock Bit” unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

9.2.5 User Signature

Each device contains a user signature of 512 bytes. It can be used by the user to store user information such as trimming, keys, etc., that the customer does not want to be erased by asserting the ERASE pin or by software ERASE command.

Read, write and erase of this area is allowed.

9.2.6 Unique Identifier

The SAMG53 Flash contains 2 pages of 512bytes called unique identifier. These 2 pages are read-only and cannot be erased even by the Erase pin. Each device integrates its own 128-bit unique identifier. These bits are factory-configured and cannot be changed by the user.

Some bytes of the user signature page are reserved for the trimming information of the 32 kHz RC Oscillator and the internal regulator.

The mapping is as follows:

- Bytes [15..0]: 128 bits for unique identifier
- Bytes [47..16]: Atmel reserved
- Bytes [49..48]: Measured frequency (on tester) of the internal 32 kHz RC with V_{VDDIO} range [1.62V to 2.5V] (measurement performed at 25°C)
- Bytes[511..50]: Atmel reserved.

9.2.7 General-Purpose Non-Volatile Memory Bits

The SAM G53 features three GPNVM bits that can be cleared or set respectively through the commands “Clear GPNVM Bit” and “Set GPNVM Bit” of the EEFC User Interface.

Table 9-2. General-purpose Non-volatile Memory Bits

GPNVM Bit[#]	Function
0	Security bit
1	Flash BOOT mode selection
2	Reserved (do not use, must be always @0x0)

9.2.8 Boot Strategies

The general-purpose NVM, GPNVM bit 1, is used to boot from the Flash.

The GPNVM bits can be cleared or set respectively through the commands “Clear GPNVM Bit” and “Set GPNVM Bit” of the EEFC User Interface.

Setting GPNVM bit 1 selects the boot from the Flash. Asserting ERASE clears the GPNVM bit 1. Thus GPNVM1 must be set to BOOT on Flash and the boot loader is removed from Flash.

9.2.9 Calibration Bits

The GPNVM bits are used to calibrate the POR, the voltage regulator and the 8/16/24 MHz RC oscillator. These bits are factory-configured and cannot be changed by the user. The ERASE pin has no effect on the calibration bits.

9.2.10 Security Bit

The SAM G53 features a security bit, based on a specific general-purpose NVM bit (GPNVM bit 0). When the security is enabled, any access to the Flash, SRAM, core registers and internal peripherals through the ICE interface is forbidden. This ensures the confidentiality of the code programmed in the Flash.

The security bit can only be enabled, through the command “Set GPNVM Bit 0” of the EEFC User Interface. Disabling the security bit can only be achieved by asserting the ERASE pin to 1, and after a full Flash erase is

performed. When the security bit is deactivated, all accesses to the Flash, SRAM, core registers, internal peripherals are permitted.

The ERASE pin integrates a permanent pull-down. Consequently, it can be left unconnected during normal operation. However, it is recommended, in harsh environments, to connect it directly to GND if the erase operation is not used in the application.

To avoid unexpected erase at power-up, a minimum ERASE pin assertion time is required. This time is defined in Table 37-41 “AC Flash Characteristics”.

The erase operation is not performed when the system is in Wait mode with the Flash in Deep-power-down mode.

To make sure that the erase operation is performed after power-up, the system must not reconfigure the ERASE pin as GPIO or enter Wait mode with Flash in Deep-power-down mode before the ERASE pin assertion time has elapsed.

With the following sequence, in any case, the erase operation is performed:

1. Assert the ERASE pin (High)
2. Assert the NRST pin (Low)
3. Power cycle the device

Maintain the ERASE pin high for at least the minimum assertion time.

10. System Controller

The System Controller is a set of peripherals, which allow handling of key elements of the system, such as power, resets, clocks, time, interrupts, watchdog, etc. Refer to the section on the Supply Controller (SUPC).

10.1 System Controller and Peripherals Mapping

Refer to Section 7-1 “SAM G53 Product Mapping”.

All the peripherals are in the bit band region and are mapped in the bit band alias region.

10.2 Power-on Reset, Supply Monitor

The SAM G53 embeds three features to monitor, warn and/or reset the chip:

- Power-on reset on VDDIO
- Power-on reset on VDDCORE
- Supply monitor on VDDIO

10.3 Reset Controller

The Reset Controller is based on a power-on reset cell. The Reset Controller returns the source of the last reset to software: general reset, wake-up reset, software reset, user reset or watchdog reset.

The Reset Controller controls the internal resets of the system and the input/output of the NRST pin. It shapes a reset signal for the external devices, simplifying the connection of a push-button on the NRST pin to implemement a manual reset. By default, the NRST pin is configured as an input.

The configuration of the Reset Controller is saved as supplied on VDDIO.

10.4 Supply Controller (SUPC)

The Supply Controller controls the power supplies of each section of the processor and the peripherals (via voltage regulator control).

The Supply Controller has its own reset circuitry and is clocked by the 32 kHz slow clock generator.

The reset circuitry is based on a zero-power power-on reset cell and a POR (power-on reset) cell. The zero-power power-on reset allows the Supply Controller to start properly, while the software-programmable POR allows detection of either a battery discharge or main voltage loss.

The slow clock generator is based on a 32 kHz crystal oscillator and an embedded 32 kHz RC oscillator. The user can also set the crystal oscillator in Bypass mode instead of connecting a crystal. In this case, the user has to provide the external clock signal on XIN32. The slow clock defaults to the RC oscillator, but the software can enable the crystal oscillator and select it as the slow clock source.

The Supply Controller starts up the device by sequentially enabling the internal power switches and the voltage regulator, then it generates the proper reset signals to the core power supply.

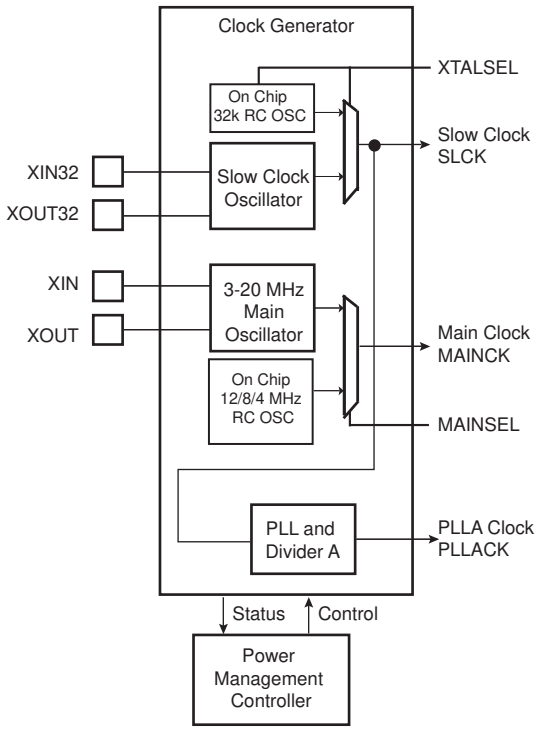
It is also used to set the system in different low power modes and to wake it up from a wide range of events.

10.5 Clock Generator

The Clock Generator is made up of:

- One low-power 32768 Hz slow clock oscillator with Bypass mode
- One low-power RC oscillator
- One factory-programmed fast RC oscillator with three selectable output frequencies: 8, 16 or 24 MHz. At startup, 8 MHz is selected.
- One 24 to 48 MHz programmable PLL that provides the clock MCK to the processor and to the peripherals. The PLL has an input divider to offer a wider range of output frequencies from the main clock input

Figure 10-1. Clock Generator Block Diagram



The 32 kHz RC oscillator frequency is measured at ambient temperature during device test. Its value is stored in the Flash signature page. The frequency accuracy is given in Table 37-16 “32 kHz RC Oscillator Characteristics”.

When the application uses the 32 kHz RC oscillator, the value of the frequency accuracy of the 32 kHz RC oscillator must be read and included in the API to use the 32 kHz RC oscillator at 32 kHz.

10.6 Power Management Controller

The Power Management Controller provides clock signals to the system:

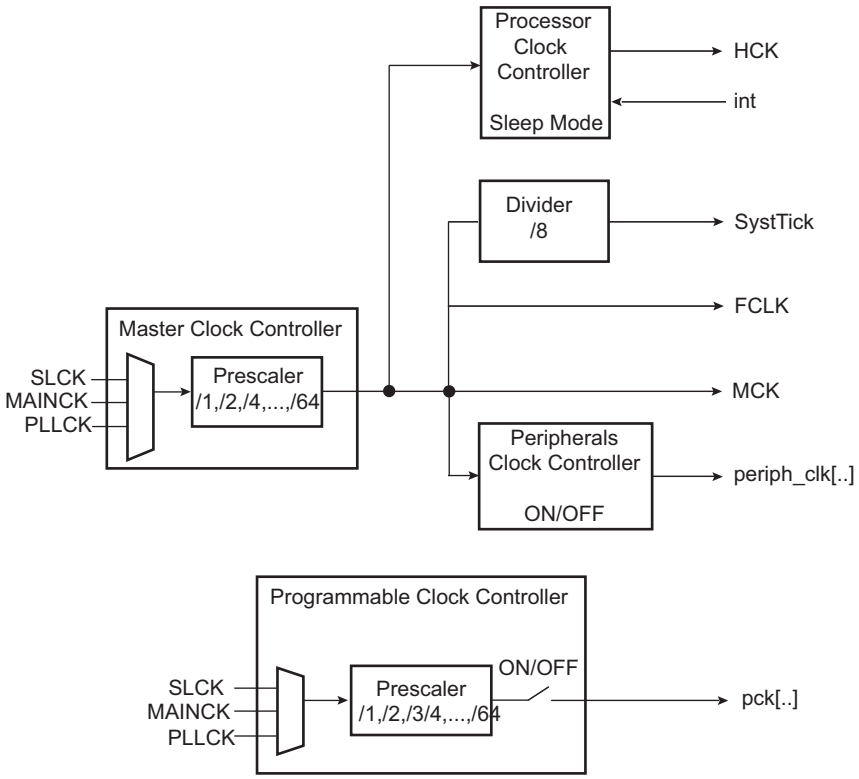
- Processor clock HCLK
- Free-running processor clock FCLK
- Cortex SysTick external clock
- Master clock MCK, specifically to the matrix and the memory interfaces
- Independent peripheral clocks, typically at the frequency of MCK
- Three programmable clock outputs: PCK0, PCK1 and PCK2

The Supply Controller selects either the 32 kHz RC oscillator or the crystal oscillator. The unused oscillator is disabled automatically so that power consumption is optimized.

By default, at start-up the chip runs out of the master clock using the fast RC oscillator running at 8 MHz.

The user can trim the 8, 16 and 24 MHz RC oscillator frequency by software.

Figure 10-2. SAM G53 Power Management Controller Block Diagram



The SysTick calibration value is fixed to 6000 which allows the generation of a time base of 1 ms with SystTick clock to MHz (max HCLK 48 MHz/8 = 6000, so STCALIB = 0x1770).

10.7 Watchdog Timer

- 16-bit key-protected only-once-programmable counter
- Windowed, prevents the processor to be in a dead-lock on the watchdog access

10.8 SysTick Timer

- 24-bit down counter
- Self-reload capability
- Flexible system timer

10.9 Real-Time Timer

- Real-Time Timer, allowing backup of time with different accuracies
  - 32-bit free-running backup counter
  - Integrates a 16-bit programmable prescaler running on slow clock
  - Alarm register generates a wake-up of the system through the Shutdown Controller
  - Wake-up from Wait mode through the Power Management Controller

10.10 Real Time Clock

- Low power consumption
- Full asynchronous design
- Two hundred year calendar
- Programmable periodic interrupt
- Alarm and update parallel load
- Control of alarm and update Time/Calendar Data In

10.11 General-Purpose Registers

- Eight 32-bit general-purpose registers

10.12 Nested Vectored Interrupt Controller

- Forty-seven maskable interrupts, external to NVIC
- Sixteen priority levels
- Dynamic reprioritization of interrupts
- Priority grouping
  - Selection of preempting interrupt levels and non-preempting interrupt levels
- Support for tail-chaining and late arrival of interrupts
  - Back-to-back interrupt processing without the overhead of state saving and restoration between interrupts
- Processor state automatically saved on interrupt entry, and restored on interrupt exit, with no instruction overhead