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SAM L10/L11 Family

Ultra Low-Power, 32-bit Cortex-M23 MCUs with TrustZone, Crypto, and Enhanced PTC

Features

- **Operating Conditions:** 1.62V to 3.63V, -40ºC to +125ºC, DC to 32 MHz
- **Core:** 32 MHz (2.62 CoreMark/MHz and up to 31 DMIPS) ARM® Cortex®-M23 with:
  - Single-cycle hardware multiplier
  - Hardware divider
  - Nested Vector Interrupt Controller (NVIC)
  - Memory Protection Unit (MPU)
  - Stack Limit Checking
  - TrustZone® for ARMv8-M (optional)
- **System**
  - Power-on Reset (POR) and programmable Brown-out Detection (BOD)
  - 8-channel Direct Memory Access Controller (DMAC)
  - 8-channel event system for Inter-peripheral Core-independent Operation
  - CRC-32 generator
- **Memory**
  - 64/32/16 KB Flash
  - 16/8/4 KB SRAM
  - 2 KB Data Flash Write-While-Read (WWR) section for non-volatile data storage
  - 256 bytes TrustRAM with physical protection features
- **Clock Management**
  - Flexible clock distribution optimized for low power
  - 32.768 kHz crystal oscillator
  - 32.768 kHz ultra low-power internal RC oscillator
  - 0.4 to 32 MHz crystal oscillator
  - 16/12/8/4 MHz low-power internal RC oscillator
  - Ultra low-power digital Frequency-Locked Loop (DFLLULP)
  - 48-96 MHz fractional digital Phase-Locked Loop (FDPLL96M)
  - One frequency meter
- **Low Power and Power Management**
  - Active, Idle, Standby with partial or full SRAM retention and off sleep modes:
    - Active mode (< 25 µA/MHz)
    - Idle mode (< 10 µA/MHz) with 1.5 µs wake-up time

        - Standby with Full SRAM Retention (0.5 µA) with 5.3 µs wake-up time
        - Off mode (< 100 nA)
    - Static and dynamic power gating architecture
    - Sleepwalking peripherals
    - Two performance levels
    - Embedded Buck/LDO regulator with on-the-fly selection

- **Security**
    - Up to four tamper pins for static and dynamic intrusion detections
    - Data Flash
        - Optimized for secrets storage
        - Data Scrambling with user-defined key (optional)
        - Rapid Tamper erase on scrambling key and on one user-defined row
        - Silent access for side channel attack resistance
    - TrustRAM
        - Address and Data scrambling with user-defined key
        - Chip-level tamper detection on physical RAM to resist microprobing attacks
        - Rapid Tamper Erase on scrambling key and RAM data
        - Silent access for side channel attack resistance
        - Data remanence prevention
    - Peripherals
        - One True Random Generator (TRNG)
        - AES-128, SHA-256, and GCM cryptography accelerators (optional)
        - Secure pin multiplexing to isolate on dedicated I/O pins a secured communication with external devices from the non-secure application (optional)
    - TrustZone for flexible hardware isolation of memories and peripherals (optional)
        - Up to six regions for the Flash
        - Up to two regions for the Data Flash
        - Up to two regions for the SRAM
        - Individual security attribution for each peripheral, I/O, external interrupt line, and Event System Channel
    - Secure Boot with SHA-based authentication (optional)
    - Up to three debug access levels
    - Up to three Chip Erase commands to erase part of or the entire embedded memories
    - Unique 128-bit serial number

- **Advanced Analog and Touch**
    - One 12-bit 1 Msps Analog-to-Digital Converter (ADC) with up to 10 channels
    - Two Analog Comparators (AC) with window compare function
    - One 10-bit 350 kSPS Digital-to-Analog Converter (DAC) with external and internal outputs
    - Three Operational Amplifiers (OPAMP)
    - One enhanced Peripheral Touch Controller (PTC):
        - Up to 20 self-capacitance channels
        - Up to 100 (10 x 10) mutual-capacitance channels
        - Low-power, high-sensitivity, environmentally robust capacitive touch buttons, sliders, and wheels

        - Hardware noise filtering and noise signal desynchronization for high conducted immunity
        - Driven Shield Plus for better noise immunity and moisture tolerance
        - Parallel Acquisition through Polarity control
        - Supports wake-up on touch from Standby Sleep mode

- **Communication Interfaces**
    - Up to three Serial Communication Interfaces (SERCOM) that can operate as:
        - USART with full-duplex and single-wire half-duplex configuration
        - I^2C up to 3.4 Mbit/s (High-Speed mode) on one instance and up to 1 Mbit/s (Fast-mode Plus) on the second instance
        - Serial Peripheral Interface (SPI)
        - ISO7816 on one instance
        - RS-485 on one instance
        - LIN Slave on one instance

- **Timers/Output Compare/Input Capture**
    - Three 16-bit Timers/Counters (TC), each configurable as:
        - One 16-bit TC with two compare/capture channels
        - One 8-bit TC with two compare/capture channels
        - One 32-bit TC with two compare/capture channels, by using two TCs
    - 32-bit Real-Time Counter (RTC) with clock/calendar functions
    - Watchdog Timer (WDT) with Window mode

- **Input/Output (I/O)**
    - Up to 25 programmable I/O lines
    - Eight external interrupts (EIC)
    - One non-maskable interrupt (NMI)
    - One Configurable Custom Logic (CCL) that supports:
        - Combinatorial logic functions, such as AND, NAND, OR, and NOR
        - Sequential logic functions, such as Flip-Flop and Latches

- **Qualification and Class-B Support**
    - AEC-Q100 REVH (Grade 1 [-40ºC to +125ºC]) (planned)
    - Class-B safety library, IEC 60730 (future)

- **Debugger Development Support**
    - Two-pin Serial Wire Debug (SWD) programming and debugging interface

- **Packages**

Type	VQFN		TQFP	SSOP	WLCSP(1)
Pin Count	24	32	32	24	32
I/O Pins (up to)	17	25	25	17	25
Contact/Lead Pitch	0.5 mm	0.5 mm	0.8 mm	0.65 mm	0.4 mm
Dimensions	4x4x0.9 mm	5x5x1 mm	7x7x1.2 mm	8.2x5.3x2.0 mm	2.79x2.79x0.482 mm

Note:

1. Contact local sales for availability.

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1. Configuration Summary

Table 1-1. SAM L10/L11 Device-specific Features

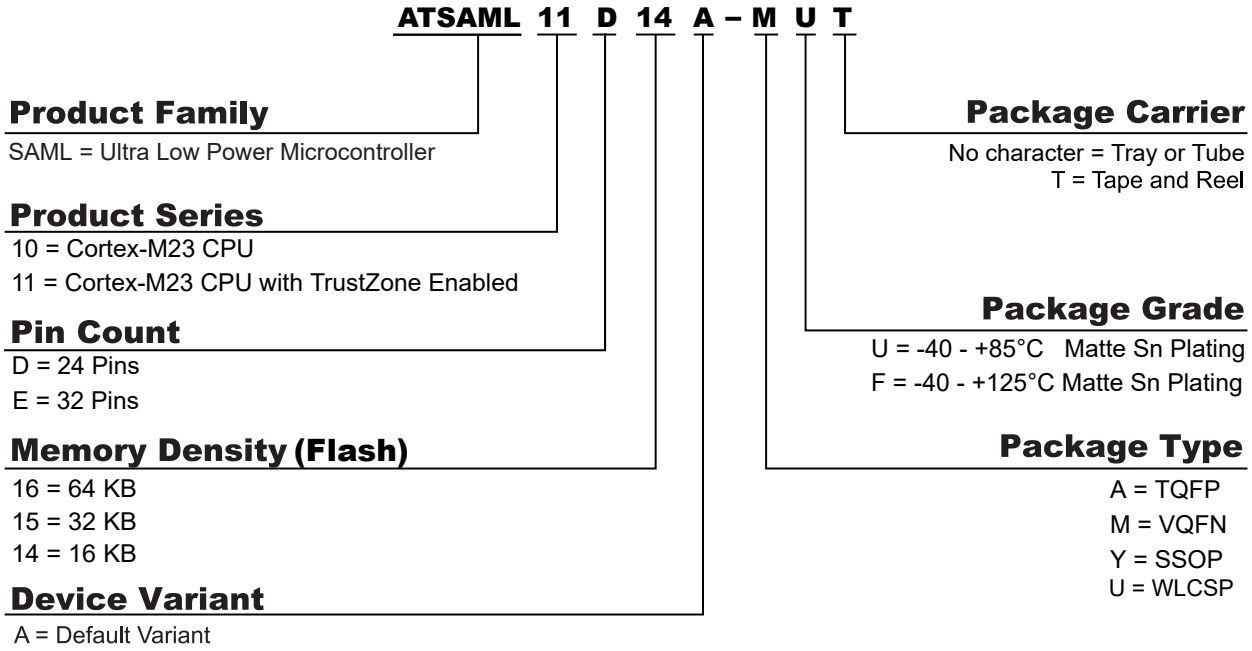
Device	Flash + Data Flash Memory (KB)	SRAM (KB)	Pins	SERCOM	ADC Channels	Analog Comparators Inputs	PTC Self-capacitance/ Mutual-capacitance Channels	I/O Pins	Tamper Pins	Packages
SAML10D14	16+2	4	24	2	5	2	16/64	17	3	VQFN, SSOP
SAML10D15	32+2	8								
SAML10D16	64+2	16								
SAML10E14	16+2	4	32	3	10	4	20/100	25	4	VQFN, TQFP, WLCSP
SAML10E15	32+2	8								
SAML10E16	64+2	16								
SAML11D14	16+2	8	24	2	5	2	16/64	17	3	VQFN, SSOP
SAML11D15	32+2	8								
SAML11D16	64+2	16								
SAML11E14	16+2	8	32	3	10	4	20/100	25	4	VQFN, TQFP, WLCSP
SAML11E15	32+2	8								
SAML11E16	64+2	16								

Table 1-2. SAM L10/L11 Family Features

Feature	SAM L10 Family	SAM L11 Family
MPU	1	2
TrustZone for ARMv8-M	No	Yes
Secure Boot	No	Yes
TrustRAM (Bytes)	256	256
DMA Channels	8	8
Data Scrambling	TrustRAM	TrustRAM, Data Flash
Event System Channels	8	8
External Interrupt Lines/NMI	8/1	8/1
Brown-out Detection	V_{DDIO} and V_{DDCORE}	V_{DDIO} and V_{DDCORE}
Secure Pin Multiplexing (on SERCOM)	No	Yes
TC/Compare	3	3
RTC	1	1
Watchdog	1	1
DAC Channels	1	1
OPAMP	3	3
CCL Look-up Tables	2	2
Frequency Meter	1	1
Crypto Accelerators	No	Yes
TRNG	Yes	Yes

Feature	SAM L10 Family	SAM L11 Family
CRC	Yes	Yes
Debug Access Levels (DAL)	2	3

2. Ordering Information

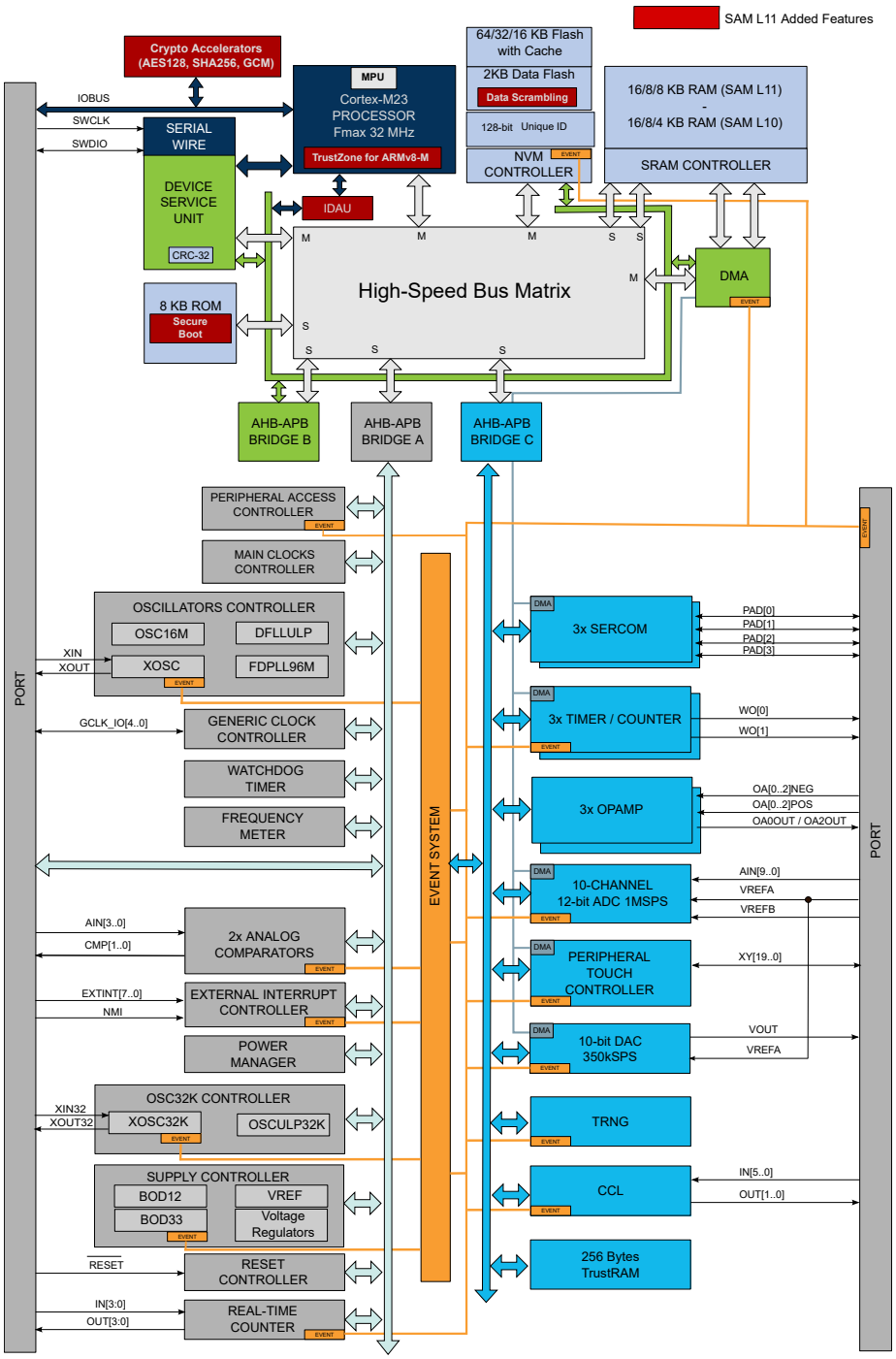


Note:

1. Devices in the WLCSP package include a factory programmed bootloader. Contact your local Microchip sales office for more information.
2. Devices can be factory programmed with securely key provisioned software. Contact your local Microchip sales office for more information.

3. Block Diagram

Figure 3-1. SAM L10/L11 Block Diagram



Note: Number of SERCOM instances, PTC/ADC channels, Tamper input pins, and Analog Compare inputs differ on the packages pinout.

4. Pinouts

Figure 4-1. SAM L10/L11 24-pin VQFN Pinout

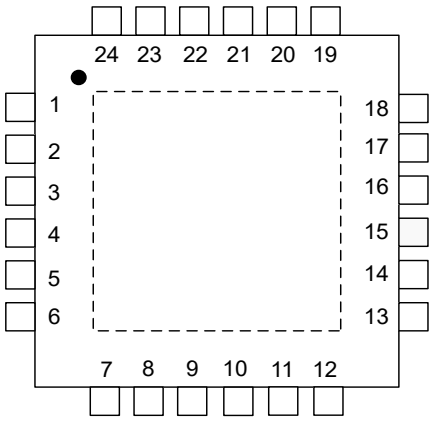


Figure 4-2. SAM L10/L11 24-pin SSOP Pinout

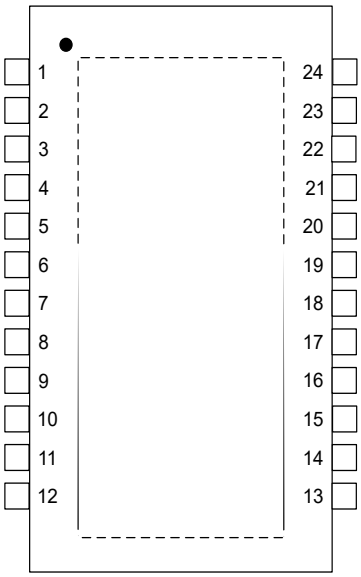


Figure 4-3. SAM L10/L11 32-pin VQFN and TQFP Pinout

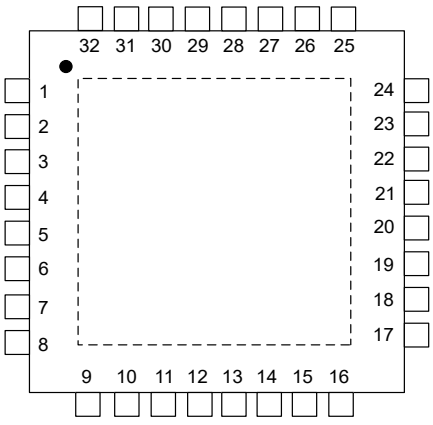
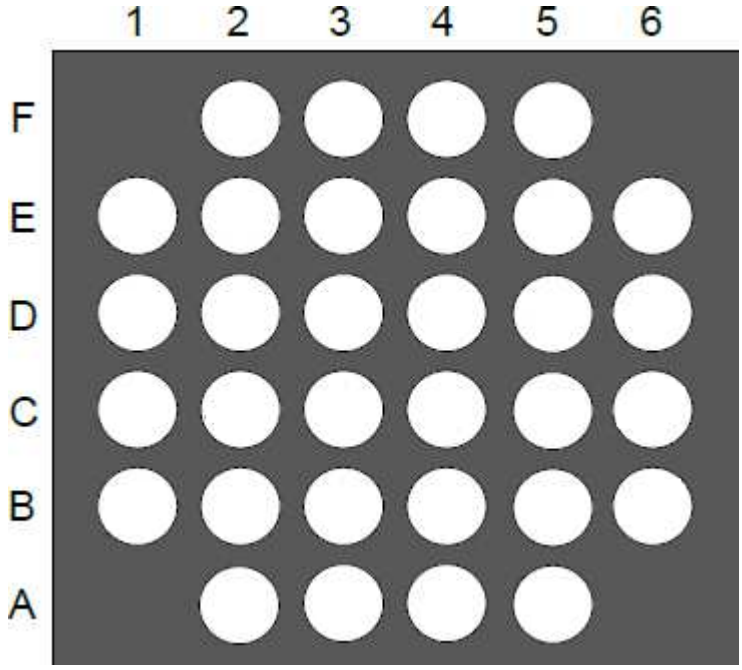


Figure 4-4. SAM L10/L11 32-pin WLCSP Pinout



4.1 Multiplexed Signals

Each pin is controlled by the I/O Pin Controller (PORT) as a general purpose I/O and alternatively can be assigned to one of the peripheral functions: A, B, C, D, E, G, H, or I.

The following table describes the peripheral signals multiplexed to the PORT I/O pins.

The column “Reset State” indicates the reset state of the line with mnemonics:

- "I/O" or "Function" indicates whether the I/O pin resets in I/O mode or in peripheral function mode.
- “I” / ”O” / "Hi-Z" indicates whether the I/O is configured as an input, output or is tri-stated.
- “PU” / “PD” indicates whether pullup, pulldown or nothing is enabled.

Table 4-1. Pinout Multiplexing

Pin				Pin Name	Supply	A	B(1)						C(2)(3)	D(2)(3)	E	G	H	I	Reset State
SSOP24	VQFN24	WLCSP32	TQFP32 / VQFN32			EIC	REF	ADC	AC	PTC	DAC	OPAMP	SERCOM	SERCOM ALTERNATIVE	TC	RTC/ Debug	AC/ GCLK	CCL	
5	2	A2	1	PA00 / XIN32	VDDANA	EXTINT[0]				XY[0]		OA1NEG		SERCOM1/ PAD[0]	TC2/ WO[0]				I/O, Hi-Z
6	3	A3	2	PA01 / XOUT32	VDDANA	EXTINT[1]				XY[1]		OA1POS		SERCOM1/ PAD[1]	TC2/ WO[1]				I/O, Hi-Z
7	4	A4	3	PA02	VDDANA	EXTINT[2]		AIN[0]		XY[2]	VOUT	OA0NEG		SERCOM0/ PAD[2]					I/O, Hi-Z
8	5	B3	4	PA03	VDDANA	EXTINT[3]	VREFA	AIN[1]		XY[3]		OA2NEG		SERCOM0/ PAD[3]					I/O, Hi-Z
9	6	B4	5	PA04	VDDANA	EXTINT[4]	VREFB	AIN[2]	AIN[0]			OA2OUT		SERCOM0/ PAD[0]	TC0/ WO[0]			IN[0]	I/O, Hi-Z
10	7	A5	6	PA05	VDDANA	EXTINT[5]		AIN[3]	AIN[1]	XY[4]		OA2POS		SERCOM0/ PAD[1]	TC0/ WO[1]			IN[1]	I/O, Hi-Z

Pin				Pin Name	Supply	A	B[1]						C[2][3]	D[2][3]	E	G	H	I	Reset State
SSOP24	VQFN24	WLCSP32	TQFP32 / VQFN32			EIC	REF	ADC	AC	PTC	DAC	OPAMP	SERCOM	SERCOM ALTERNATIVE	TC	RTC/ Debug	AC/ GCLK	CCL	
		C4	7	PA06	VDDANA	EXTINT[6]		AIN[4]	AIN[2]	XY[5]		OA0POS		SERCOM0/ PAD[2]	TC1/ WO[0]			IN[2]	I/O, Hi-Z
		B5	8	PA07	VDDANA	EXTINT[7]		AIN[5]	AIN[3]			OA0OUT		SERCOM0/ PAD[3]	TC1/ WO[1]			OUT[0]	I/O, Hi-Z
11	8	B6	9	VDDANA															-
12	9	C6	10	GNDANA															-
13	10	D4	11	PA08	VDDIO	NMI		AIN[6]		XY[6]			SERCOM1/ PAD[0]	SERCOM2/ PAD[0]		RTC/ IN[0]		IN[3]	I/O, Hi-Z
		D6	12	PA09	VDDIO	EXTINT[0]		AIN[7]		XY[7]			SERCOM1/ PAD[1]	SERCOM2/ PAD[1]		RTC/ IN[1]		IN[4]	I/O, Hi-Z
		C5	13	PA10	VDDIO	EXTINT[1]		AIN[8]		XY[8]			SERCOM1/ PAD[2]	SERCOM2/ PAD[2]			GCLK_IO[4]	IN[5]	I/O, Hi-Z
		D5	14	PA11	VDDIO	EXTINT[2]		AIN[9]		XY[9]			SERCOM1/ PAD[3]	SERCOM2/ PAD[3]			GCLK_IO[3]	OUT[1]	I/O, Hi-Z
14	11	E6	15	PA14 / XOSC	VDDIO	EXTINT[3]				XY[10]			SERCOM2/ PAD[2]	SERCOM0/ PAD[2]	TC0/ WO[0]		GCLK_IO[0]		I/O, Hi-Z
15	12	E5	16	PA15 / XOUT	VDDIO	EXTINT[4]				XY[11]			SERCOM2/ PAD[3]	SERCOM0/ PAD[3]	TC0/ WO[1]		GCLK_IO[1]		I/O, Hi-Z
16	13	D3	17	PA16[4]	VDDIO	EXTINT[5]				XY[12]			SERCOM1/ PAD[0]	SERCOM0/ PAD[0]		RTC/ IN[2]	GCLK_IO[2]	IN[0]	I/O, Hi-Z
17	14	F5	18	PA17[4]	VDDIO	EXTINT[6]				XY[13]			SERCOM1/ PAD[1]	SERCOM0/ PAD[1]		RTC/ IN[3]	GCLK_IO[3]	IN[1]	I/O, Hi-Z
18	15	E4	19	PA18	VDDIO	EXTINT[7]				XY[14]			SERCOM1/ PAD[2]	SERCOM0/ PAD[2]	TC2/ WO[0]	RTC/ OUT[0]	AC/ CMP[0]	IN[2]	I/O, Hi-Z
19	16	E3	20	PA19	VDDIO	EXTINT[0]				XY[15]			SERCOM1/ PAD[3]	SERCOM0/ PAD[3]	TC2/ WO[1]	RTC/ OUT[1]	AC/ CMP[1]	OUT[0]	I/O, Hi-Z
20	17	F4	21	PA22[4]	VDDIO	EXTINT[1]				XY[16]			SERCOM0/ PAD[0]	SERCOM2/ PAD[0]	TC0/ WO[0]	RTC/ OUT[2]	GCLK_IO[2]		I/O, Hi-Z
21	18	F3	22	PA23[4]	VDDIO	EXTINT[2]				XY[17]			SERCOM0/ PAD[1]	SERCOM2/ PAD[1]	TC0/ WO[1]	RTC/ OUT[3]	GCLK_IO[1]		I/O, Hi-Z
		F2	23	PA24	VDDIO	EXTINT[3]							SERCOM0/ PAD[2]	SERCOM2/ PAD[2]	TC1/ WO[0]				I/O, Hi-Z
		E2	24	PA25	VDDIO	EXTINT[4]							SERCOM0/ PAD[3]	SERCOM2/ PAD[3]	TC1/ WO[1]				I/O, Hi-Z
		D2	25	PA27	VDDIO	EXTINT[5]											GCLK_IO[0]		I/O, Hi-Z
22	19	C2	26	$\overline{\text{RESET}}$	VDDIO														I, PU
23	20	E1	27	VDDCORE															-
24	21	D1	28	GND															-
1	22	C1	29	VDDOUT															-
2	23	B1	30	VDDIO															-

Pin				Pin Name	Supply	A	B[1]						C[2][3]	D[2][3]	E	G	H	I	Reset State
SSOP24	VQFN24	WLCSP32	TQFP32 / VQFN32			EIC	REF	ADC	AC	PTC	DAC	OPAMP	SERCOM	SERCOM ALTERNATIVE	TC	RTC/ Debug	AC/ GCLK	CCL	
3	24	B2	31	PA30 / SWCLK	VDDIO	EXTINT[6]				XY[18]				SERCOM1/ PAD[2]	TC1/ WO[0]	SWCLK	GCLK_IO[0]	IN[3]	SWCLK, I, PU
4	1	C3	32	PA31 / SWDIO(4)	VDDIO	EXTINT[7]				XY[19]				SERCOM1/ PAD[3]	TC1/ WO[1]			OUT[1]	I/O, Hi-Z

1. All analog pin functions are on the peripheral function B. The peripheral function B must be selected to disable the digital control of the pin.
2. Refer to SERCOM Configurations to get the list of the supported features for each SERCOM instance.
3. 24-pin packages only have two SERCOM instances: SERCOM0 and SERCOM1.
4. The following pins are High Sink pins and have different properties than standard pins: PA16, PA17, PA22, PA23 and PA31.

4.2 Oscillators Pinout

The oscillators are not mapped to the I/O Pin Controller (PORT) functions and their multiplexing is controlled by the Oscillators Controller (OSCCTRL) and 32 kHz Oscillators Controller (OSC32KCTRL) registers.

Table 4-2. Oscillator Pinout

Oscillator	Supply	Signal	I/O pin
XOSC	VDDIO	XIN	PA14
		XOUT	PA15
XOSC32K	VDDANA	XIN32	PA00
		XOUT32	PA01

To improve the cycle-to-cycle jitter of the XOSC32 oscillator, it is recommended to keep the neighboring pins of XIN32 and the following pins of XOUT32 as static as possible:

Table 4-3. XOSC32 Jitter Minimization

Package Pin Count	Static Signal Recommended
32	PA02, PA03
24	PA02, PA03

4.3 Serial Wire Debug Interface Pinout

The SWCLK pin is by default assigned to the SWCLK peripheral function G to allow debugger probe detection.

A debugger probe detection (cold-plugging or hot-plugging) will automatically switch the SWDIO I/O pin to the SWDIO function, as long as the SWLCK peripheral function is selected.

Table 4-4. Serial Wire Debug Interface Pinout

Signal	Supply	I/O pin
SWCLK	VDDIO	PA30
SWDIO	VDDIO	PA31

4.4 SERCOM Configurations

The following table lists the supported features for each SERCOM instance:

Table 4-5. SERCOM Features Summary

	SERCOM Instance		
Protocol	**SERCOM0**	**SERCOM1**	**SERCOM2**
SPI	Yes	Yes	Yes
I^2C (1)	Yes High-speed mode (≤ 3,4 Mbit/s)	Yes Fast plus Mode (≤ 1 Mbit/s)	No
USART	Yes including: Hardware Handshaking IrDA	Yes including: Hardware Handshaking IrDA	Yes including: Hardware Handshaking IrDA RS-485 Auto-baud mode LIN Slave ISO7816
USART/SPI Receive Buffer Size	Two-level	Four-level	Two-level
Secure Pin Multiplexing (**SAM L11 only**)	No	Yes	No

Note:

1. I^2C is not supported on all SERCOM pins. Refer to the SERCOM I^2C Pins table for more details.

4.4.1 SERCOM I2C Pins

The following table lists the SERCOM pins which support I^2C:

Table 4-6. SERCOM I^2C Pins

Pin Name	SERCOM0 I^2C Pad Name	SERCOM1 I^2C Pad Name
PA16	SERCOM0/PAD[0]	SERCOM1/PAD[0]
PA17	SERCOM0/PAD[1]	SERCOM1/PAD[1]
PA22	SERCOM0/PAD[0]	N/A
PA23	SERCOM0/PAD[1]	N/A

4.4.2 Secure Pin Multiplexing (on SERCOM) Pins

The Secure Pin Multiplexing feature can be used on dedicated SERCOM I/O pins to isolate a secure communication with external devices from the non-secure application.

Refer to 13.6 Secure Pin Multiplexing on SERCOM for more details.

The following table lists the SERCOM pins that support the Secure Pin Multiplexing feature:

Table 4-7. Secure Pin Multiplexing on SERCOM Pins

Pin Name	Secure Pin Multiplexing Pad Name
PA16	SERCOM1/PAD[0]
PA17	SERCOM1/PAD[1]
PA18	SERCOM1/PAD[2]
PA19	SERCOM1/PAD[3]

4.5 General Purpose I/O (GPIO) Clusters

Table 4-8. GPIO Clusters

Package	Cluster	GPIO	Supply Pins Connected to the Cluster
32-pin	1	PA00 PA01 PA02 PA03 PA04 PA05 PA06 PA07	V_{DDANA}/GNDANA
	2	PA08 PA09 PA10 PA11 PA14 PA15 PA16 PA17 PA18 PA19 PA22 PA23 PA24 PA25 PA27 PA30 PA31	V_{DDIO}/GND
24-pin	1	PA00 PA01 PA02 PA03 PA04 PA05	V_{DDANA}/GND
	2	PA08 PA14 PA15 PA16 PA17 PA18 PA19 PA22 PA23 PA30 PA31	V_{DDIO}/GND

5. Signal Descriptions List

The following table provides details on signal names classified by peripherals.

Table 5-1. Signal Descriptions List

Signal Name	Function	Type
Generic Clock Generator - GCLK		
GCLK_IO[4:0]	Generators Clock Source (Input) or Generic Clock Signal (Output)	Digital I/O
Oscillators Control - OSCCTRL		
XIN	Crystal Oscillator or External Clock Input	Analog Input (Crystal Oscillator)/Digital Input (External Clock)
XOUT	Crystal Oscillator Output	Analog Output
32 kHz Oscillators Control - OSC32KCTRL		
XIN32	32.768 kHz Crystal Oscillator or External Clock Input	Analog Input (Crystal Oscillator)/Digital Input (External Clock)
XOUT32	32.768 kHz Crystal Oscillator Output	Analog Output
Serial Communication Interface - SERCOMx		
PAD[3:0]	General SERCOM Pins	Digital I/O
Timer Counter - TCx		
WO[1:0]	Capture Inputs or Waveform Outputs	Digital I/O
Real Timer Clock - RTC		
IN[3:0]	Tamper Detection Inputs	Digital Input
OUT[3:0]	Tamper Detection Outputs	Digital Output
Analog Comparators - AC		
AIN[3:0]	AC Comparator Inputs	Analog Input
CMP[1:0]	AC Comparator Outputs	Digital Output
Analog Digital Converter - ADC		
AIN[9:0]	ADC Input Channels	Analog Input
VREFA(1)	ADC External Reference Voltage A	Analog Input
VREFB	ADC External Reference Voltage B	Analog Input
Digital Analog Converter - DAC		
VOUT	DAC Voltage Output	Analog Output
VREFA(1)	DAC External Reference Voltage A	Analog Input
Operational Amplifier - OPAMP		
OA[2:0]NEG	OPAMP Negative Inputs	Analog Input
OA[2:0]POS	OPAMP Positive Inputs	Analog Input
OA0OUT / OA2OUT	OPAMP Outputs	Analog Output
Peripheral Touch Controller - PTC		
XY[19:0]	X-lines and Y-lines	Digital Output (X-line) /Analog I/O (Y-line)
Custom Control Logic - CCL		
IN[5:0]	Inputs to lookup table	Digital Output
OUT[1:0]	Outputs from lookup table	Digital Input

Signal Name	Function	Type
External Interrupt Controller - EIC		
EXTINT[7:0]	External Interrupts Pins	Digital Input
NMI	Non-Maskable Interrupt Pin	Digital Input
General Purpose I/O - PORT		
PA11-PA00 / PA19-PA14 / PA25-PA22 / PA27 / PA31-PA30	General Purpose I/O Pin in Port A	Digital I/O
Reset Controller - RSTC		
$\overline{\text{RESET}}$	External Reset Pin (Active Level: LOW)	Digital Input
Debug Service Unit - DSU		
SWCLK	Serial Wire Clock	Digital Input
SWDIO	Serial Wire Bidirectional Data Pin	Digital I/O

1. VREFA is shared between the ADC and DAC peripherals.