



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from Europe, America and south Asia, supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts, Customers Priority, Honest Operation, and Considerate Service", our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip, ALPS, ROHM, Xilinx, Pulse, ON, Everlight and Freescale. Main products comprise IC, Modules, Potentiometer, IC Socket, Relay, Connector. Our parts cover such applications as commercial, industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

SAM L21E / SAM L21G / SAM L21J

DATASHEET COMPLETE

Introduction

Atmel® | SMART SAM L21 is a series of Ultra low-power microcontrollers using the 32-bit ARM® Cortex®-M0+ processor at max. 48MHz (2.46 CoreMark®/MHz) and up to 256KB Flash and 40KB of SRAM in a 32, 48, and 64 pin package. The sophisticated power management technologies, such as power domain gating, SleepWalking, Ultra low-power peripherals and more, allow for very low current consumptions. The highly configurable peripherals include a touch controller supporting capacitive interfaces with proximity sensing.

Features

- Processor
 - ARM Cortex-M0+ CPU running at up to 48MHz
 - Single-cycle hardware multiplier
 - Micro Trace Buffer
- Memories
 - 32/64/128/256KB in-system self-programmable Flash
 - 1/2/4/8KB Flash Read-While-Write section
 - 4/8/16/32KB SRAM Main Memory
 - 2/4/8/8KB SRAM Low power Memory
- System
 - Power-on reset (POR) and brown-out detection (BOD)
 - Internal and external clock options
 - External Interrupt Controller (EIC)
 - 16 external interrupts
 - One non-maskable interrupt
 - Two-pin Serial Wire Debug (SWD) programming, test and debugging interface
- Low Power
 - Idle, Standby, Backup, and Off sleep modes
 - SleepWalking peripherals

- Static and Dynamic Power Gating Architecture
 - Battery backup support
 - Two Performance Levels
 - Embedded Buck/LDO regulator supporting on-the-fly selection
- Peripherals
 - 16-channel Direct Memory Access Controller (DMAC)
 - 12-channel Event System
 - Up to five 16-bit Timer/Counters (TC) including one low-power TC, each configurable as:
 - 16-bit TC with two compare/capture channels
 - 8-bit TC with two compare/capture channels
 - 32-bit TC with two compare/capture channels, by using two TCs
 - Two 24-bit and one 16-bit Timer/Counters for Control (TCC), with extended functions:
 - Up to four compare channels with optional complementary output
 - Generation of synchronized pulse width modulation (PWM) pattern across port pins
 - Deterministic fault protection, fast decay and configurable dead-time between complementary output
 - Dithering that increase resolution with up to 5 bit and reduce quantization error
 - 32-bit Real Time Counter (RTC) with clock/calendar function
 - Watchdog Timer (WDT)
 - CRC-32 generator
 - One full-speed (12Mbps) Universal Serial Bus (USB) 2.0 interface
 - Embedded host and device function
 - Eight endpoints
 - Up to six Serial Communication Interfaces (SERCOM) including one low-power SERCOM, each configurable to operate as either:
 - USART with full-duplex and single-wire half-duplex configuration
 - I²C up to 3.4MHz
 - SPI
 - LIN slave
 - One AES encryption engine
 - One True Random Generator (TRNG)
 - One Configurable Custom Logic (CCL)
 - One 12-bit, 1MSPS Analog-to-Digital Converter (ADC) with up to 20 channels
 - Differential and single-ended input
 - Automatic offset and gain error compensation
 - Oversampling and decimation in hardware to support 13-, 14-, 15-, or 16-bit resolution
 - Two 12-bit, 1MSPS Dual Output Digital-to-Analog Converter (DAC)
 - Two Analog Comparators (AC) with window compare function
 - Three Operational Amplifiers (OPAMP)
 - Peripheral Touch Controller (PTC)
 - 169-Channel capacitive touch and proximity sensing
 - Wake-up on touch in standby mode
- Oscillators
 - 32.768kHz crystal oscillator (XOSC32K)

- 0.4-32MHz crystal oscillator (XOSC)
 - 32.768kHz internal oscillator (OSC32K)
 - 32.768kHz ultra-low-power internal oscillator (OSCULP32K)
 - 16/12/8/4MHz high-accuracy internal oscillator (OSC16M)
 - 48MHz Digital Frequency Locked Loop (DFLL48M)
 - 96MHz Fractional Digital Phased Locked Loop (FDPLL96M)
- I/O
 - Up to 51 programmable I/O pins
- Easy migration from SAM D family
- Packages
 - 64-pin TQFP, QFN, WLCSP
 - 48-pin TQFP, QFN
 - 32-pin TQFP, QFN
- Operating Voltage
 - 1.62V – 3.63V

Table of Contents

Introduction.....	1
Features.....	1
1. Description.....	14
2. Configuration Summary.....	16
3. Ordering Information.....	19
3.1. SAM L21J.....	19
3.2. SAM L21G.....	20
3.3. SAM L21E.....	20
3.4. Device Identification.....	20
4. Block Diagram.....	22
5. Pinout.....	24
5.1. SAM L21J.....	24
5.2. SAM L21J WLCSP64.....	25
5.3. SAM L21G.....	26
5.4. SAM L21E.....	27
6. Signal Descriptions List.....	28
7. I/O Multiplexing and Considerations.....	30
7.1. Multiplexed Signals.....	30
7.2. Other Functions.....	32
8. Analog Connections of Peripherals.....	35
8.1. Block Diagram.....	35
8.2. Analog Connections.....	35
8.3. Reference Voltages.....	36
8.4. Analog ONDEMAND Function.....	36
9. Power Supply and Start-Up Considerations.....	38
9.1. Power Domain Overview.....	38
9.2. Power Supply Considerations.....	38
9.3. Power-Up.....	41
9.4. Power-On Reset and Brown-Out Detector.....	42
9.5. Performance Level Overview.....	43
10. Product Mapping.....	45
11. Memories.....	46
11.1. Embedded Memories.....	46
11.2. Physical Memory Map.....	46

11.3. NVM User Row Mapping.....	47
11.4. NVM Software Calibration Area Mapping.....	48
11.5. NVM Temperature Log Row.....	49
11.6. Serial Number.....	49
12. Processor and Architecture.....	50
12.1. Cortex M0+ Processor.....	50
12.2. Nested Vector Interrupt Controller.....	52
12.3. Micro Trace Buffer.....	53
12.4. High-Speed Bus System.....	54
13. PAC - Peripheral Access Controller.....	59
13.1. Overview.....	59
13.2. Features.....	59
13.3. Block Diagram.....	59
13.4. Product Dependencies.....	59
13.5. Functional Description.....	60
13.6. Register Summary.....	64
13.7. Register Description.....	65
14. Peripherals Configuration Summary.....	85
15. DSU - Device Service Unit.....	88
15.1. Overview.....	88
15.2. Features.....	88
15.3. Block Diagram.....	89
15.4. Signal Description.....	89
15.5. Product Dependencies.....	89
15.6. Debug Operation.....	90
15.7. Chip Erase.....	92
15.8. Programming.....	92
15.9. Intellectual Property Protection.....	93
15.10. Device Identification.....	94
15.11. Functional Description.....	95
15.12. Register Summary.....	101
15.13. Register Description.....	103
16. Clock System.....	127
16.1. Clock Distribution.....	127
16.2. Synchronous and Asynchronous Clocks.....	128
16.3. Register Synchronization.....	129
16.4. Enabling a Peripheral.....	131
16.5. On Demand Clock Requests.....	131
16.6. Power Consumption vs. Speed.....	132
16.7. Clocks after Reset.....	132
17. GCLK - Generic Clock Controller.....	133
17.1. Overview.....	133
17.2. Features.....	133

17.3. Block Diagram.....	133
17.4. Signal Description.....	134
17.5. Product Dependencies.....	134
17.6. Functional Description.....	135
17.7. Register Summary.....	141
17.8. Register Description.....	145
18. MCLK – Main Clock.....	154
18.1. Overview.....	154
18.2. Features.....	154
18.3. Block Diagram.....	154
18.4. Signal Description.....	154
18.5. Product Dependencies.....	154
18.6. Functional Description.....	156
18.7. Register Summary.....	161
18.8. Register Description.....	161
19. RSTC – Reset Controller.....	180
19.1. Overview.....	180
19.2. Features.....	180
19.3. Block Diagram.....	180
19.4. Signal Description.....	181
19.5. Product Dependencies.....	181
19.6. Functional Description.....	182
19.7. Register Summary.....	185
19.8. Register Description.....	185
20. PM – Power Manager.....	192
20.1. Overview.....	192
20.2. Features.....	192
20.3. Block Diagram.....	193
20.4. Signal Description.....	193
20.5. Product Dependencies.....	193
20.6. Functional Description.....	194
20.7. Register Summary.....	217
20.8. Register Description.....	217
21. OSCCTRL – Oscillators Controller.....	226
21.1. Overview.....	226
21.2. Features.....	226
21.3. Block Diagram.....	226
21.4. Signal Description.....	226
21.5. Product Dependencies.....	227
21.6. Functional Description.....	228
21.7. Register Summary.....	239
21.8. Register Description.....	240
22. OSC32KCTRL – 32KHz Oscillators Controller.....	273
22.1. Overview.....	273

22.2. Features.....	273
22.3. Block Diagram.....	274
22.4. Signal Description.....	274
22.5. Product Dependencies.....	274
22.6. Functional Description.....	276
22.7. Register Summary.....	280
22.8. Register Description.....	280
23. SUPC – Supply Controller.....	292
23.1. Overview.....	292
23.2. Features.....	292
23.3. Block Diagram.....	293
23.4. Signal Description.....	293
23.5. Product Dependencies.....	293
23.6. Functional Description.....	295
23.7. Register Summary.....	303
23.8. Register Description.....	304
24. WDT – Watchdog Timer.....	327
24.1. Overview.....	327
24.2. Features.....	327
24.3. Block Diagram.....	328
24.4. Signal Description.....	328
24.5. Product Dependencies.....	328
24.6. Functional Description.....	329
24.7. Register Summary.....	335
24.8. Register Description.....	335
25. RTC – Real-Time Counter.....	347
25.1. Overview.....	347
25.2. Features.....	347
25.3. Block Diagram.....	347
25.4. Signal Description.....	348
25.5. Product Dependencies.....	348
25.6. Functional Description.....	350
25.7. Register Summary - COUNT32.....	356
25.8. Register Description - COUNT32.....	357
25.9. Register Summary - COUNT16.....	371
25.10. Register Description - COUNT16.....	372
25.11. Register Summary - CLOCK.....	388
25.12. Register Description - CLOCK.....	389
26. DMAC – Direct Memory Access Controller.....	406
26.1. Overview.....	406
26.2. Features.....	406
26.3. Block Diagram.....	408
26.4. Signal Description.....	408
26.5. Product Dependencies.....	408
26.6. Functional Description.....	409

26.7. Register Summary.....	429
26.8. Register Description.....	430
26.9. Register Summary - LP SRAM.....	462
26.10. Register Description - LP SRAM.....	462
27. EIC – External Interrupt Controller.....	470
27.1. Overview.....	470
27.2. Features.....	470
27.3. Block Diagram.....	470
27.4. Signal Description.....	471
27.5. Product Dependencies.....	471
27.6. Functional Description.....	472
27.7. Register Summary.....	477
27.8. Register Description.....	477
28. NVMCTRL – Non-Volatile Memory Controller.....	489
28.1. Overview.....	489
28.2. Features.....	489
28.3. Block Diagram.....	489
28.4. Signal Description.....	490
28.5. Product Dependencies.....	490
28.6. Functional Description.....	491
28.7. Register Summary.....	498
28.8. Register Description.....	498
29. PORT - I/O Pin Controller.....	512
29.1. Overview.....	512
29.2. Features.....	512
29.3. Block Diagram.....	513
29.4. Signal Description.....	513
29.5. Product Dependencies.....	513
29.6. Functional Description.....	516
29.7. Register Summary.....	522
29.8. Register Description.....	524
30. EVSYS – Event System.....	544
30.1. Overview.....	544
30.2. Features.....	544
30.3. Block Diagram.....	544
30.4. Signal Description.....	545
30.5. Product Dependencies.....	545
30.6. Functional Description.....	546
30.7. Register Summary.....	550
30.8. Register Description.....	551
31. SERCOM – Serial Communication Interface.....	568
31.1. Overview.....	568
31.2. Features.....	568
31.3. Block Diagram.....	569

31.4. Signal Description.....	569
31.5. Product Dependencies.....	569
31.6. Functional Description.....	571
32. SERCOM USART – SERCOM Universal Synchronous and Asynchronous Receiver and Transmitter.....	577
32.1. Overview.....	577
32.2. USART Features.....	577
32.3. Block Diagram.....	578
32.4. Signal Description.....	578
32.5. Product Dependencies.....	578
32.6. Functional Description.....	580
32.7. Register Summary.....	592
32.8. Register Description.....	592
33. SERCOM SPI – SERCOM Serial Peripheral Interface.....	615
33.1. Overview.....	615
33.2. Features.....	615
33.3. Block Diagram.....	616
33.4. Signal Description.....	616
33.5. Product Dependencies.....	616
33.6. Functional Description.....	618
33.7. Register Summary.....	627
33.8. Register Description.....	628
34. SERCOM I²C – SERCOM Inter-Integrated Circuit.....	648
34.1. Overview.....	648
34.2. Features.....	648
34.3. Block Diagram.....	649
34.4. Signal Description.....	649
34.5. Product Dependencies.....	649
34.6. Functional Description.....	651
34.7. Register Summary - I ² C Slave.....	670
34.8. Register Description - I ² C Slave.....	670
34.9. Register Summary - I ² C Master.....	690
34.10. Register Description - I ² C Master.....	691
35. TC – Timer/Counter.....	713
35.1. Overview.....	713
35.2. Features.....	713
35.3. Block Diagram.....	714
35.4. Signal Description.....	714
35.5. Product Dependencies.....	715
35.6. Functional Description.....	716
35.7. Register Summary.....	731
35.8. Register Description.....	735
36. TCC – Timer/Counter for Control Applications.....	765
36.1. Overview.....	765

36.2. Features.....	765
36.3. Block Diagram.....	766
36.4. Signal Description.....	766
36.5. Product Dependencies.....	767
36.6. Functional Description.....	768
36.7. Register Summary.....	802
36.8. Register Description.....	804
37. TRNG – True Random Number Generator.....	849
37.1. Overview.....	849
37.2. Features.....	849
37.3. Block Diagram.....	849
37.4. Signal Description.....	849
37.5. Product Dependencies.....	849
37.6. Functional Description.....	850
37.7. Register Summary.....	853
37.8. Register Description.....	853
38. AES – Advanced Encryption Standard.....	860
38.1. Overview.....	860
38.2. Features.....	860
38.3. Block Diagram.....	861
38.4. Signal Description.....	862
38.5. Product Dependencies.....	862
38.6. Functional Description.....	863
38.7. Register Summary.....	872
38.8. Register Description.....	874
39. USB – Universal Serial Bus.....	891
39.1. Overview.....	891
39.2. Features.....	891
39.3. USB Block Diagram.....	892
39.4. Signal Description.....	892
39.5. Product Dependencies.....	892
39.6. Functional Description.....	894
39.7. Register Summary.....	912
39.8. Register Description.....	916
40. CCL – Configurable Custom Logic.....	991
40.1. Overview.....	991
40.2. Features.....	991
40.3. Block Diagram.....	992
40.4. Signal Description.....	992
40.5. Product Dependencies.....	992
40.6. Functional Description.....	993
40.7. Register Summary.....	1004
40.8. Register Description.....	1004
41. OPAMP – Operational Amplifier Controller.....	1009

41.1. Overview.....	1009
41.2. Features.....	1009
41.3. Block Diagram.....	1010
41.4. Signal Description.....	1010
41.5. Product Dependencies.....	1011
41.6. Functional Description.....	1012
41.7. Register Summary.....	1024
41.8. Register Description.....	1025
42. ADC – Analog-to-Digital Converter.....	1032
42.1. Overview.....	1032
42.2. Features.....	1032
42.3. Block Diagram.....	1033
42.4. Signal Description.....	1033
42.5. Product Dependencies.....	1033
42.6. Functional Description.....	1035
42.7. Register Summary.....	1047
42.8. Register Description.....	1048
43. AC – Analog Comparators.....	1076
43.1. Overview.....	1076
43.2. Features.....	1076
43.3. Block Diagram.....	1077
43.4. Signal Description.....	1077
43.5. Product Dependencies.....	1077
43.6. Functional Description.....	1079
43.7. Register Summary.....	1088
43.8. Register Description.....	1088
44. DAC – Digital-to-Analog Converter.....	1106
44.1. Overview.....	1106
44.2. Features.....	1106
44.3. Block Diagram.....	1106
44.4. Signal Description.....	1107
44.5. Product Dependencies.....	1107
44.6. Functional Description.....	1109
44.7. Register Summary.....	1117
44.8. Register Description.....	1117
45. PTC - Peripheral Touch Controller.....	1139
45.1. Overview.....	1139
45.2. Features.....	1139
45.3. Block Diagram.....	1140
45.4. Signal Description.....	1141
45.5. Product Dependencies.....	1141
45.6. Functional Description.....	1142
46. Electrical Characteristics.....	1144
46.1. Disclaimer.....	1144

46.2. Absolute Maximum Ratings.....	1144
46.3. General Operating Ratings.....	1144
46.4. Supply Characteristics.....	1145
46.5. Maximum Clock Frequencies.....	1146
46.6. Power Consumption.....	1148
46.7. Wake-Up Time.....	1153
46.8. I/O Pin Characteristics.....	1154
46.9. Injection Current.....	1155
46.10. Analog Characteristics.....	1156
46.11. NVM Characteristics.....	1174
46.12. Oscillators Characteristics.....	1175
46.13. Timing Characteristics.....	1182
46.14. USB Characteristics.....	1187
47. Typical Characteristics.....	1188
47.1. Power Consumption over Temperature in Sleep Modes.....	1188
48. Packaging Information.....	1190
48.1. Thermal Considerations.....	1190
48.2. Package Drawings.....	1191
48.3. Soldering Profile.....	1200
49. Schematic Checklist.....	1201
49.1. Introduction.....	1201
49.2. Power Supply.....	1201
49.3. External Analog Reference Connections.....	1204
49.4. External Reset Circuit.....	1205
49.5. Unused or Unconnected Pins.....	1207
49.6. Clocks and Crystal Oscillators.....	1207
49.7. Programming and Debug Ports.....	1209
49.8. USB Interface.....	1213
50. Errata.....	1215
50.1. Die Revision A.....	1215
50.2. Die Revision B.....	1226
50.3. Die Revision C.....	1229
51. Conventions.....	1233
51.1. Numerical Notation.....	1233
51.2. Memory Size and Type.....	1233
51.3. Frequency and Time.....	1233
51.4. Registers and Bits.....	1234
52. Acronyms and Abbreviations.....	1235
53. Datasheet Revision History.....	1238
53.1. Rev J - 06/2016.....	1238
53.2. Rev I - 02/2016.....	1239
53.3. Rev H - 12/2015.....	1241

53.4. Rev G - 11/2015.....	1242
53.5. Rev F - 09/2015.....	1245
53.6. Rev E - 07/2015.....	1248
53.7. Rev D - 06/2015.....	1249
53.8. Rev C - 03/2015.....	1250
53.9. Rev B - 02/2015.....	1253
53.10. Rev A - 01/2015.....	1254

1. Description

Atmel® | SMART SAM L21 is a series of Ultra low-power microcontrollers using the 32-bit ARM® Cortex®-M0+ processor, and ranging from 32- to 64-pins with up to 256KB Flash and 40KB of SRAM. The SAM L21 devices operate at a maximum frequency of 48MHz and reach 2.46 CoreMark®/MHz. They are designed for simple and intuitive migration with identical peripheral modules, hex compatible code, identical linear address map and pin compatible migration paths between all devices in the product series. All devices include intelligent and flexible peripherals, Atmel Event System for inter-peripheral signaling, and support for capacitive touch button, slider and wheel user interfaces.

The Atmel SAM L21 devices provide the following features: In-system programmable Flash, 16-channel direct memory access (DMA) controller, 12-channel Event System, programmable interrupt controller, up to 51 programmable I/O pins, 32-bit real-time clock and calendar, up to five 16-bit Timer/Counters (TC) and three Timer/Counters for Control (TCC) where each TC/TCC can be configured to perform frequency and waveform generation, accurate program execution timing or input capture with time and frequency measurement of digital signals. The TCs can operate in 8- or 16-bit mode, selected TCs can be cascaded to form a 32-bit TC, and three timer/counters have extended functions optimized for motor, lighting and other control applications. Two TCC can operate in 24-bit mode, the third TCC can operate in 16-bit mode. The series provide one full-speed USB 2.0 embedded host and device interface; up to six Serial Communication Modules (SERCOM) that each can be configured to act as an USART, UART, SPI, I²C up to 3.4MHz, SMBus, PMBus, and LIN slave; up to twenty channel 1MSPS 12-bit ADC with programmable gain and optional oversampling and decimation supporting up to 16-bit resolution, two 12-bit 1MSPS DACs, two analog comparators with window mode, three independent cascadable OPAMPs supporting internal connection with others analog features, Peripheral Touch Controller supporting up to 192 buttons, sliders, wheels and proximity sensing; programmable Watchdog Timer, brown-out detector and power-on reset and two-pin Serial Wire Debug (SWD) program and debug interface.

All devices have accurate and low-power external and internal oscillators. All oscillators can be used as a source for the system clock. Different clock domains can be independently configured to run at different frequencies, enabling power saving by running each peripheral at its optimal clock frequency, and thus maintaining a high CPU frequency while reducing power consumption.

The SAM L21 devices have four software-selectable sleep modes, idle, standby, backup and off. In idle mode the CPU is stopped while all other functions can be kept running. In standby all clocks and functions are stopped except those selected to continue running. In this mode all RAMs and logic contents are retained. The device supports SleepWalking. This feature allows the peripheral to wake up from sleep based on predefined conditions, and thus allows some internal operation like DMA transfer and/or the CPU to wake up only when needed, e.g. when a threshold is crossed or a result is ready. The Event System supports synchronous and asynchronous events, allowing peripherals to receive, react to and send events even in standby mode.

The SAM L21 devices have two software-selectable performance levels (PL0 and PL2) allowing the user to scale the lowest core voltage level that will support the operating frequency. To further minimize consumption, specifically leakage dissipation, the SAM L21 devices utilizes power domain gating technique with retention to turn off some logic area while keeping its logic state. This technique is fully handled by hardware.

The Flash program memory can be reprogrammed in-system through the SWD interface. The same interface can be used for nonintrusive on-chip debugging of application code. A boot loader running in the device can use any communication interface to download and upgrade the application program in the Flash memory.

The Atmel SAM L21 devices are supported with a full suite of programs and system development tools, including C compilers, macro assemblers, program debugger/simulators, programmers and evaluation kits.

2. Configuration Summary

	SAM L21J	SAM L21G	SAM L21E
Pins	64	48	32
General Purpose I/O-pins (GPIOs)	51	37	25
Flash	256/128/64KB	256/128/64KB	256/128/64/32KB
Flash RWW section	8/4/2KB	8/4/2KB	8/4/2/1KB
System SRAM	32/16/8KB	32/16/8KB	32/16/8/4KB
Low Power SRAM	8/8/4KB	8/8/4KB	8/8/4/2KB
Timer Counter (TC) instances ⁽¹⁾	5	3	3
Waveform output channels per TC instance	2	2	2
Timer Counter for Control (TCC) instances	3	3	3
Waveform output channels per TCC	8/4/2	8/4/2	6/4/2
DMA channels	16	16	16
USB interface	1	1	1
AES engine	1	1	1
Configurable Custom Logic (CCL) (LUTs)	4	4	4
True Random Generator (TRNG)	1	1	1
Serial Communication Interface (SERCOM) instances	6	6	6
Analog-to-Digital Converter (ADC) channels	20	14	10
Analog Comparators (AC)	2	2	2
Digital-to-Analog Converter (DAC) channels	2	2	2
Operational Amplifier (OPAMP)	3	3	3

	SAM L21J	SAM L21G	SAM L21E
Real-Time Counter (RTC)	Yes	Yes	Yes
RTC alarms	1	1	1
RTC compare values	One 32-bit value or two 16-bit values	One 32-bit value or two 16-bit values	One 32-bit value or two 16-bit values
External Interrupt lines	16	16	16
Peripheral Touch Controller (PTC) channels (X- x Y-Lines) for mutual capacitance (2)	169 (13x13)	81 (9x9)	42 (7x6)
Peripheral Touch Controller (PTC) channels for self capacitance (Y-Lines only) (3)	16	10	7
Maximum CPU frequency	48MHz		
Packages	QFN TQFP WLCSP(4)	QFN TQFP	QFN TQFP
Oscillators	32.768kHz crystal oscillator (XOSC32K) 0.4-32MHz crystal oscillator (XOSC) 32.768kHz internal oscillator (OSC32K) 32KHz ultra-low-power internal oscillator (OSCULP32K) 16/12/8/4MHz high-accuracy internal oscillator (OSC16M) 48MHz Digital Frequency Locked Loop (DFLL48M) 96MHz Fractional Digital Phased Locked Loop (FDPLL96M)		
Event System channels	12	12	12
SW Debug Interface	Yes	Yes	Yes
Watchdog Timer (WDT)	Yes	Yes	Yes

Note:

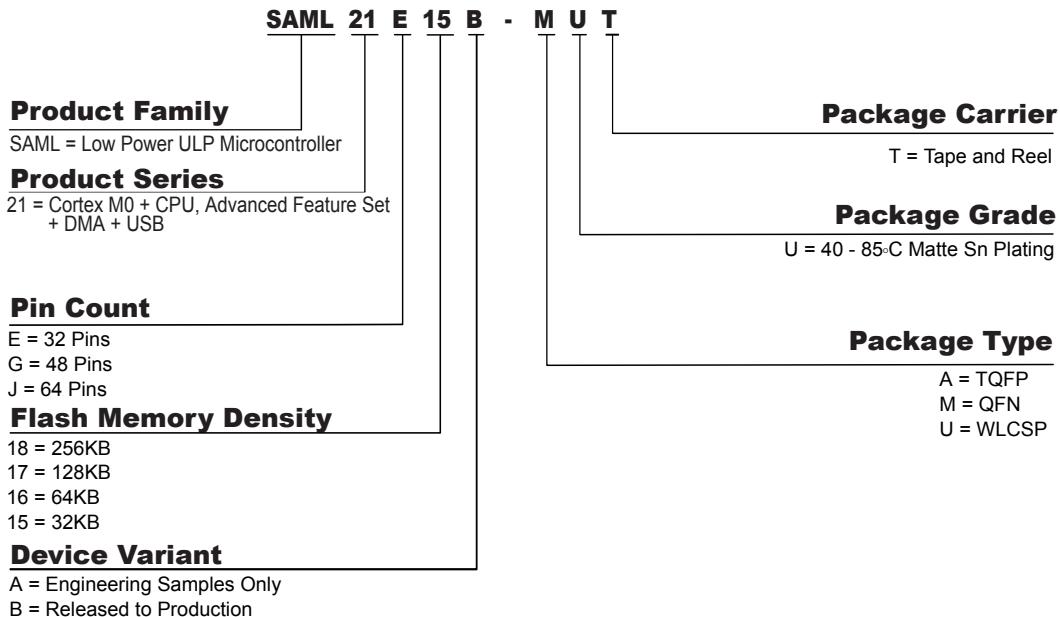
1. For SAM L21E and SAM L21G, only TC0, TC1 and TC4 are available.
2. The number of X- and Y-lines depends on the configuration of the device, as some I/O lines can be configured as either X-lines or Y-lines. Refer to *Multiplexed Signals* for details. The number in the Configuration Summary is the maximum number of channels that can be obtained.

3. The number of Y-lines depends on the configuration of the device, as some I/O lines can be configured as either X-lines or Y-lines. The number given here is the maximum number of Y-lines that can be obtained.
4. WLCSP parts are programmed with a specific SPI bootloader. Refer to Application Note AT09002 for details.

Related Links

[Multiplexed Signals](#) on page 30

3. Ordering Information



Note: The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die.

3.1. SAM L21J

Table 3-1. SAM L21J Ordering Codes

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAML21J16B-AUT	64K	8K	TQFP64	Tape & Reel
ATSAML21J16B-MUT			QFN64	
ATSAML21J17B-AUT	128K	16K	TQFP64	Tape & Reel
ATSAML21J17B-MUT			QFN64	
ATSAML21J17B-UUT			WLCSP64	
ATSAML21J18B-AUT	256K	32K	TQFP64	Tape & Reel
ATSAML21J18B-MUT			QFN64	
ATSAML21J18B-UUT			WLCSP64	

3.2. SAM L21G

Table 3-2. SAM L21G Ordering Codes

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAML21G16B-AUT	64K	8K	TQFP48	Tape & Reel
ATSAML21G16B-MUT			QFN48	
ATSAML21G17B-AUT	128K	16K	TQFP48	Tape & Reel
ATSAML21G17B-MUT			QFN48	
ATSAML21G18B-AUT	256K	32K	TQFP48	Tape & Reel
ATSAML21G18B-MUT			QFN48	

3.3. SAM L21E

Table 3-3. SAM L21E

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAML21E15B-AUT	32K	4K	TQFP32	Tape & Reel
ATSAML21E15B-MUT			QFN32	
ATSAML21E16B-AUT	64K	8K	TQFP32	Tape & Reel
ATSAML21E16B-MUT			QFN32	
ATSAML21E17B-AUT	128K	16K	TQFP32	Tape & Reel
ATSAML21E17B-MUT			QFN32	
ATSAML21E18B-AUT	256K	32K	TQFP32	Tape & Reel
ATSAML21E18B-MUT			QFN32	

3.4. Device Identification

The DSU - Device Service Unit peripheral provides the Device Selection bits in the Device Identification register (DID.DEVSEL) in order to identify the device by software. The SAM L21 variants have a reset value of DID=0x1081drxx, with the LSB identifying the die number ('d'), the die revision ('r') and the device selection ('xx').

Table 3-4. SAM L21 Device Identification Values

DEVSEL (DID[7:0])	Device
0x00	SAML21J18A
0x01	SAML21J17A
0x02	SAML21J16A
0x03-0x04	Reserved
0x05	SAML21G18A

DEVSEL (DID[7:0])	Device
0x06	SAML21G17A
0x07	SAML21G16A
0x08-0x09	Reserved
0x0A	SAML21E18A
0x0B	SAML21E17A
0x0C	SAML21E16A
0x0D	SAML21E15A
0x0E	Reserved
0x0F	SAML21J18B
0x10	SAML21J17B
0x11	SAML21J16B
0x12-0x13	Reserved
0x14	SAML21G18B
0x15	SAML21G17B
0x16	SAML21G16B
0x17-0x18	Reserved
0x19	SAML21E18B
0x1A	SAML21E17B
0x1B	SAML21E16B
0x1C	SAML21E15B
0x1D-0xFF	Reserved

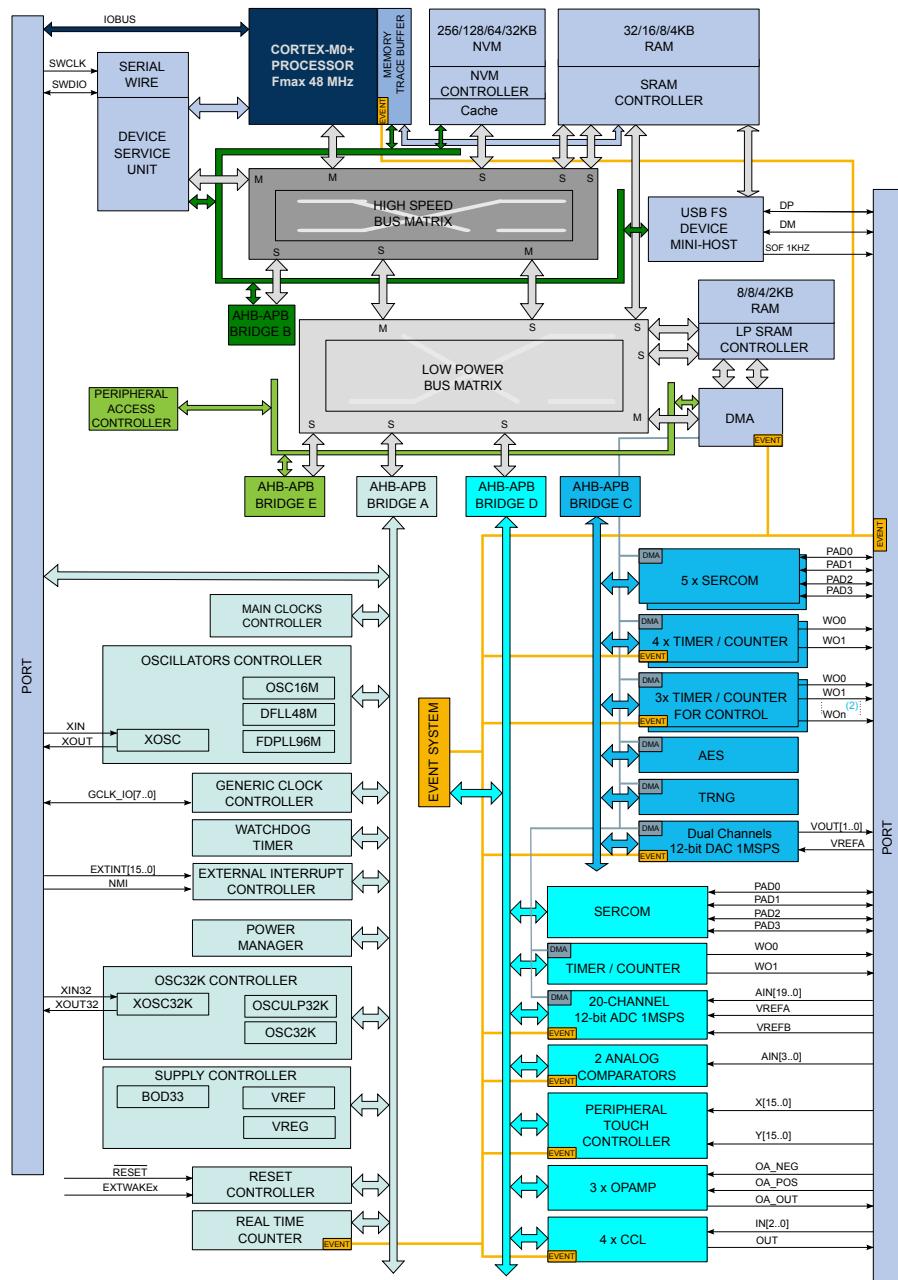
Note: The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die.

Related Links

[DSU - Device Service Unit](#) on page 88

[DID](#) on page 112

4. Block Diagram



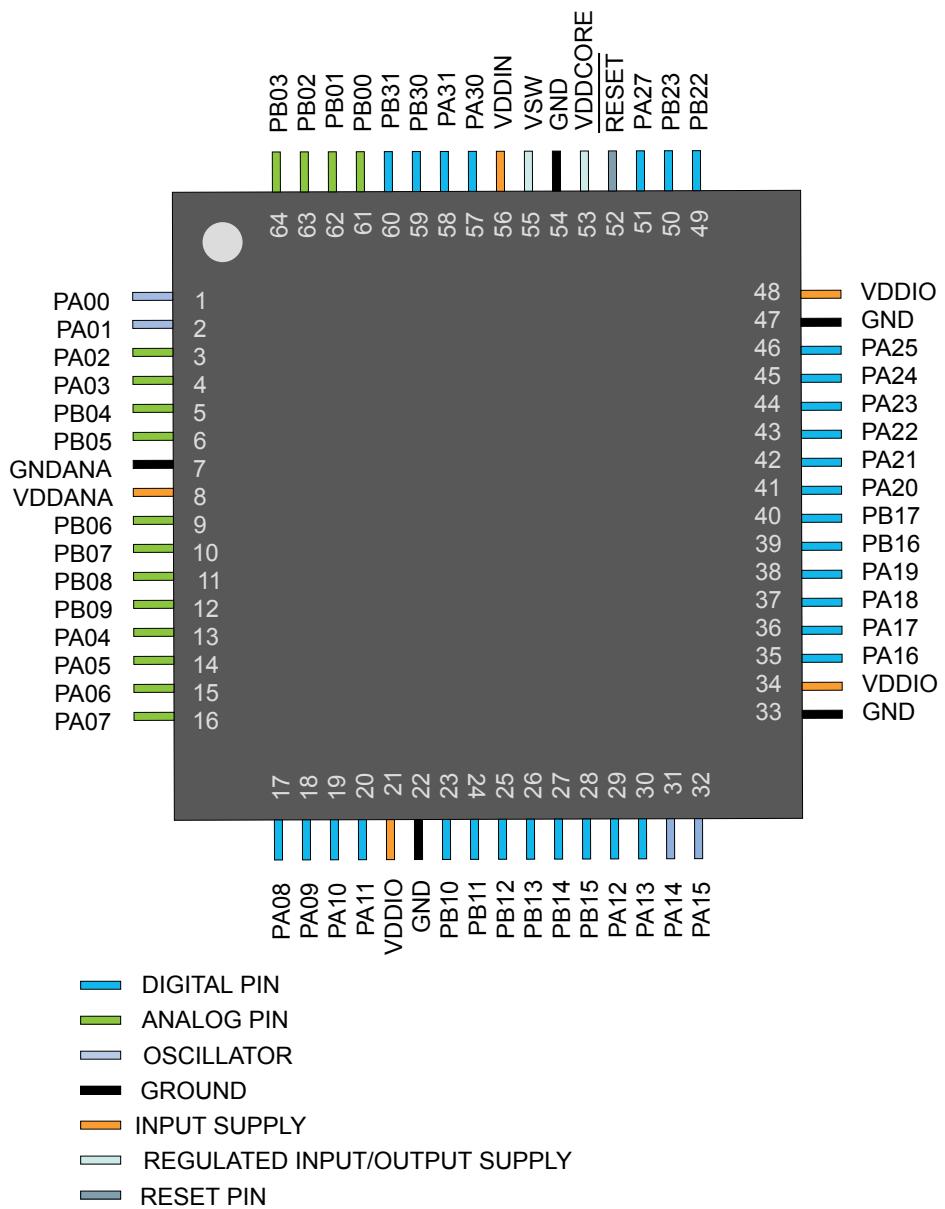
Note:

1. Some products have different number of SERCOM instances, Timer/Counter instances, PTC signals and ADC signals. Refer to [Peripherals Configuration Summary](#) for details.

2. The three TCC instances have different configurations, including the number of Waveform Output (WO) lines.

5. Pinout

5.1. SAM L21J



5.2. SAM L21J WLCSP64

