Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Atmel SAM R21E / SAM R21G

SMART ARM-Based Wireless Microcontroller

DATASHEET

Description

The Atmel® | SMART™ SAM R21 is a series of low-power microcontrollers using the 32-bit ARM® Cortex®-M0+ processor and an integrated ultra-low power 2.4GHz ISM band transceiver. SAM R21 devices are available in 32- and 48-pin packages with up to 256KB Flash, 32KB of SRAM and are operating at a maximum frequency of 48MHz and reach 2.46 Coremark/MHz. They are designed for simple and intuitive migration with identical peripheral modules, hex compatible code, identical linear address map and pin compatible migration paths between all devices in the product series. All devices include intelligent and flexible peripherals, Atmel Event System for inter-peripheral signaling, and support for capacitive touch button, slider and wheel user interfaces.

The Atmel SAM R21 devices provide the following features: In-system programmable Flash, optional 512KB serial Flash,12-channel direct memory access (DMA) controller, 12-channel Event System, programmable interrupt controller, up to 28 programmable I/O pins, ultra-low power 2.4GHz ISM band transceiver with a data rate of 250kb/s, 32-bit real-time clock and calendar, three 16-bit Timer/Counters (TC) and three 16-bit Timer/Counters for Control (TCC), where each TC can be configured to perform frequency and waveform generation, accurate program execution timing or input capture with time and frequency measurement of digital signals. The TCs can operate in 8- or 16-bit mode, selected TCs can be cascaded to form a 32-bit TC, and the three Timer/Counters for Control have extended functions optimized for motor, lighting and other control applications. The series provide one full-speed USB 2.0 embedded host and device interface; up to five Serial Communication Modules (SERCOM) that each can be configured to act as an USART, UART, SPI, I2C up 3.4MHz and LIN slave; up to eight channel 350ksps 12-bit ADC with programmable gain and optional oversampling and decimation supporting up to 16-bit resolution, two analog comparators with window mode, Peripheral Touch Controller supporting up to 48 buttons, sliders, wheels and proximity sensing; programmable Watchdog Timer, brown-out detector and power-on reset and two-pin Serial Wire Debug (SWD) program and debug interface.

All devices have accurate and low-power external and internal oscillators. All oscillators can be used as a source for the system clock. Different clock domains can be independently configured to run at different frequencies, enabling power saving by running each peripheral at its optimal clock frequency, and thus maintaining a high CPU frequency while reducing power consumption.

The SAM R21 devices have two software-selectable sleep modes, idle and standby. In idle mode the CPU is stopped while all other functions can be kept running. In standby all clocks and functions are stopped expect those selected to continue running. The device supports SleepWalking, which is the module's ability to wake itself up and wake up its own clock, and hence perform predefined tasks without waking up the CPU. The CPU can then be only woken on a need basis, e.g. a threshold is crossed or a result is ready. The Event System supports synchronous and asynchronous events, allowing peripherals to receive, react to and send events even in standby mode.

The Flash program memory can be reprogrammed in-system through the SWD interface. The same interface can be used for non-intrusive on-chip debug of application code. A boot loader running in the device can use any communication interface to download and upgrade the application program in the Flash memory.

The SAM R21 devices are supported with a full suite of program and system development tools, including C compilers, macro assemblers, program debugger/simulators, programmers and evaluation kits.

Features

- Processor
  - ARM Cortex-M0+ CPU running at up to 48MHz
    - Single-cycle hardware multiplier
    - Micro Trace Buffer (MTB)
- Memories
  - 768[1]/256/128/64KB in-system self-programmable Flash
  - 32/16/8KB SRAM
- System
  - Power-on reset (POR) and brown-out detection (BOD)
  - Internal and external clock options with 48MHz Digital Frequency Locked Loop (DFLL48M) and 48MHz to 96MHz Fractional Digital Phase Locked Loop (FDPLL96M)
  - External Interrupt Controller (EIC)
  - Up to 15 external interrupts
  - One non-maskable interrupt
  - Two-pin Serial Wire Debug (SWD) programming, test and debugging interface
- Low Power
  - Idle and standby sleep modes
  - SleepWalking peripherals
- Peripherals
  - 12-channel Direct Memory Access Controller (DMAC)
  - 12-channel Event System
  - Integrated Ultra Low Power Transceiver for 2.4GHz ISM Band
    - Supported PSDU Data rates: 250kb/s, 500kb/s, 1000kb/s and 2000kb/s[2]
    - -99dBm RX Sensitivity; TX Output Power up to +4dBm
    - Hardware Assisted MAC (Auto-Acknowledge, Auto-Retry)
    - SFD-Detection; Spreading; De-Spreading; Framing; CRC-16 Computation
    - Antenna Diversity and TX/RX Control
    - 128 Byte TX/RX Frame Buffer
    - Integrated 16MHz Crystal Oscillator (external crystal needed)
    - PLL synthesizer with 5 MHz and 500 kHz channel spacing for 2.4GHz ISM band
    - Hardware Security (AES, True Random Generator)
  - Three 16-bit Timer/Counters (TC), configurable as either:
    - One 16-bit TC with compare/capture channels
    - One 8-bit TC with compare/capture channels
    - One 32-bit TC with compare/capture channels, by using two TCs
  - Three 16-bit Timer/Counters for Control (TCC), with extended functions:
    - Up to four compare channels with optional complementary output
    - Generation of synchronized pulse width modulation (PWM) pattern across port pins
    - Deterministic fault protection, fast decay and configurable dead-time between complementary output
    - Dithering that increase resolution with up to 5 bit and reduce quantization error
  - 32-bit Real Time Counter (RTC) with clock/calendar function
  - Watchdog Timer (WDT)
  - CRC-32 generator
  - One full-speed (12Mbps) Universal Serial Bus (USB) 2.0 interface
    - Embedded host and device function
    - Eight endpoints
  - Up to five Serial Communication Interfaces (SERCOM), each configurable to operate as either:
    - USART with full-duplex and single-wire half-duplex configuration
    - I^2C up to 3.4MHz
    - SPI
    - LIN slave
  - One 12-bit, 350ksps Analog-to-Digital Converter (ADC) with up to eight external channels
    - Differential and single-ended input
    - 1/2x to 16x programmable gain stage
    - Automatic offset and gain error compensation
    - Oversampling and decimation in hardware to support 13-, 14-, 15- or 16-bit resolution
  - Two Analog Comparators (AC) with window compare function
  - Peripheral Touch Controller (PTC)
    - 48-channel capacitive touch and proximity sensing
- I/O and Package
  - 16/28 programmable I/O pins
  - 32-pin and 48-pin QFN

- Operating Voltage
  - 1.8V – 3.6V
- Temperature Range
  - -40°C to 85°C Industrial
  - -40°C to 125°C Industrial

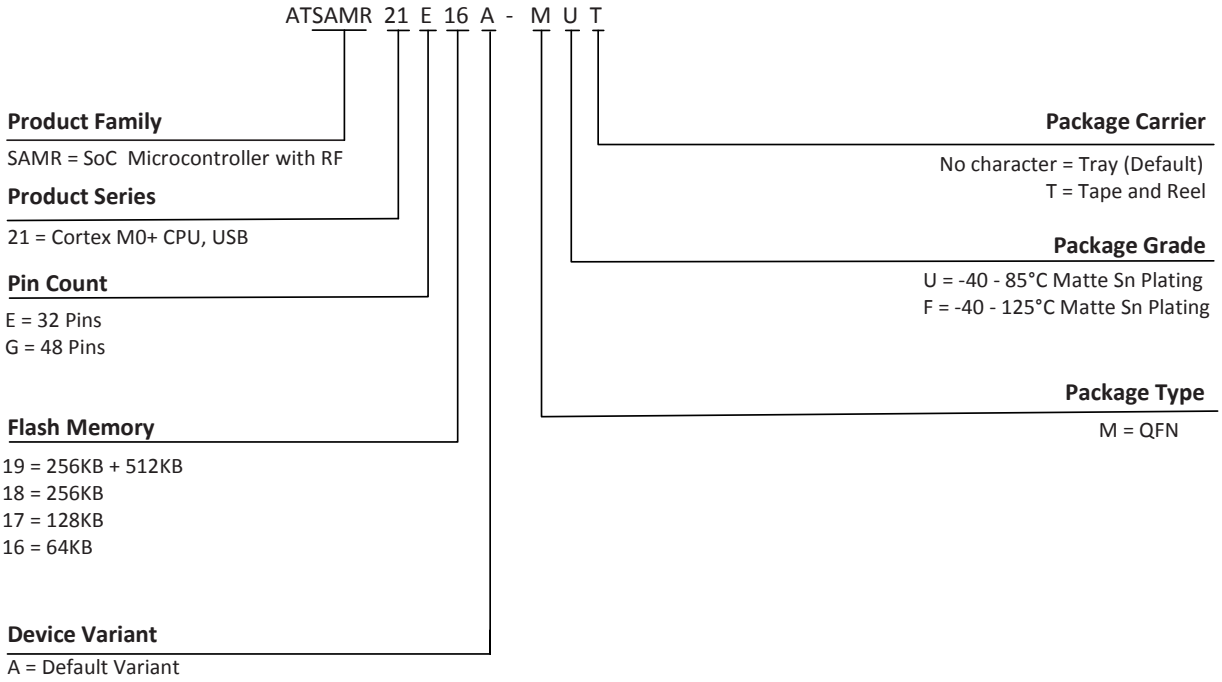
Notes:
1. Only applicable for SAM R21E19: 256KB embedded + 512KB serial Flash.
2. High data rates (500kb/s, 1000kb/s and 2000kb/s) only applicable for T=-40°C to 85°C.

1. Configuration Summary

	SAM R21G	SAM R21E
Pins	48	32
General Purpose I/O-pins (GPIOs)	28	16
Flash	256/128/64KB	256/128/64KB
SRAM	32/16/8KB	32/16/8KB
Timer Counter (TC) instances	3	3
Waveform output channels per TC instance	2	2
Timer Counter for Control (TCC) instances	3	3
Waveform output channels per TCC	4/4/2	4/4/2
DMA channels	12	12
USB interface	1	1
Serial Communication Interface (SERCOM) instances	5+1(1)	4+1(1)
Inter-IC Sound (I^2S) interface	No	No
Analog-to-Digital Converter (ADC) channels	8	4
Analog Comparators (AC)	2	2
Digital-to-Analog Converter (DAC) channels	No	No
Real-Time Counter (RTC)	Yes	Yes
RTC alarms	1	1
RTC compare values	1 32-bit value or 2 16-bit values	1 32-bit value or 2 16-bit values
External Interrupt lines	15	14
Peripheral Touch Controller (PTC) X and Y lines	8x6	6x2
Maximum CPU frequency	48MHz	
Packages	QFN	QFN
32.768kHz crystal oscillator (XOSC32K)	Yes	No
Oscillators	16MHz crystal oscillator for 2.4GHz TRX (XOSCRF) 0.4-32MHz crystal oscillator (XOSC) 32.768kHz internal oscillator (OSC32K) 32kHz ultra-low-power internal oscillator (OSCULP32K) 8MHz high-accuracy internal oscillator (OSC8M) 48MHz Digital Frequency Locked Loop (DFLL48M) 96MHz Fractional Digital Phased Locked Loop (FDPLL96M)	
Event System channels	12	12
SW Debug Interface	Yes	Yes
Watchdog Timer (WDT)	Yes	Yes

Note: 1. SERCOM4 is internally connected to the AT86RF233.

2. Ordering Information



2.1 SAM R21E

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMR21E16A-MF	64K	8K	QFN32	Tray
ATSAMR21E16A-MFT				Tape & Reel
ATSAMR21E16A-MU				Tray
ATSAMR21E16A-MUT				Tape & Reel
ATSAMR21E17A-MF	128K	16K	QFN32	Tray
ATSAMR21E17A-MFT				Tape & Reel
ATSAMR21E17A-MU				Tray
ATSAMR21E17A-MUT				Tape & Reel
ATSAMR21E18A-MF	256K	32K	QFN32	Tray
ATSAMR21E18A-MFT				Tape & Reel
ATSAMR21E18A-MU				Tray
ATSAMR21E18A-MUT				Tape & Reel
ATSAMR21E19A-MF	256K + 512K(1)	32K	QFN32	Tray
ATSAMR21E19A-MFT				Tape & Reel

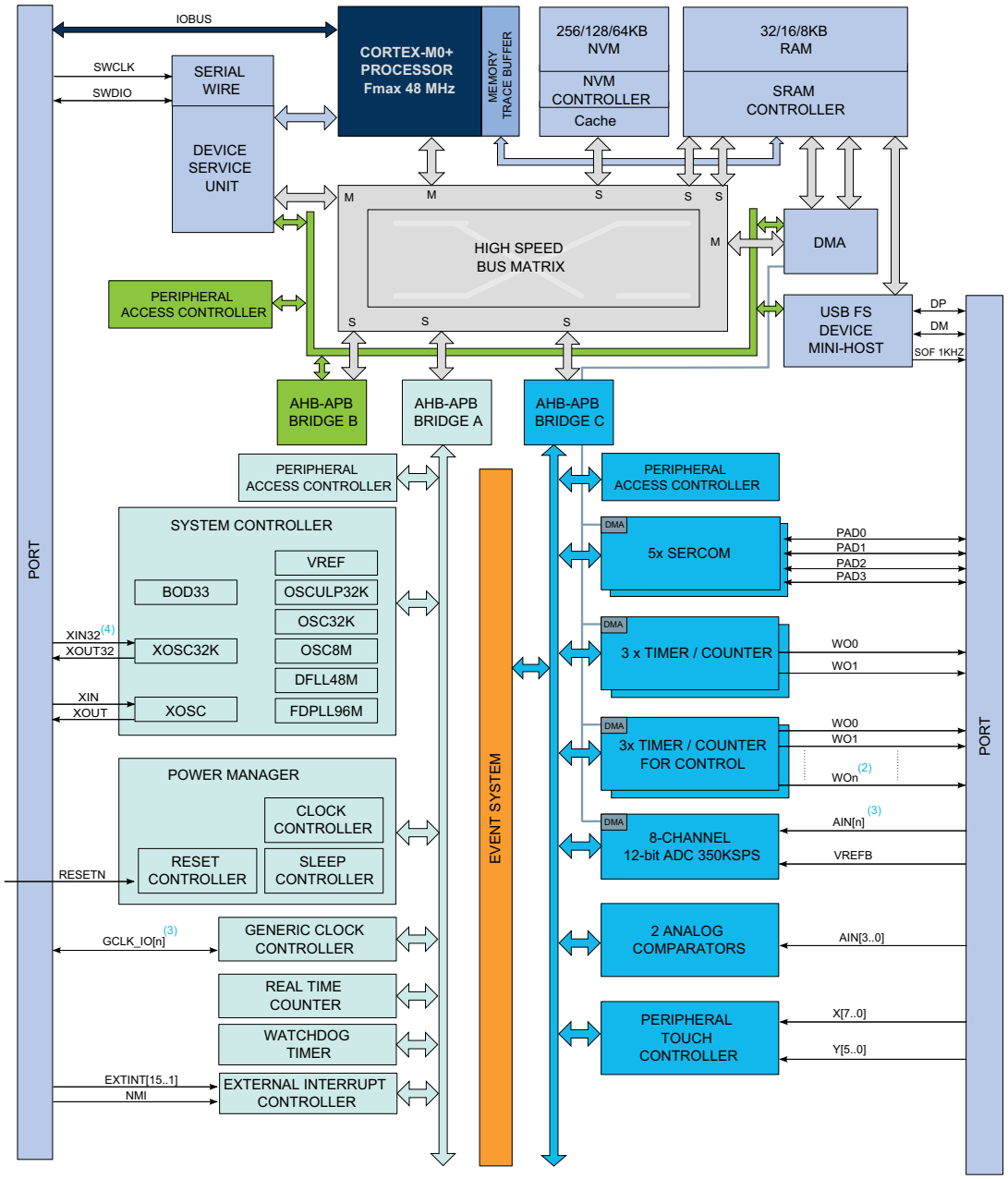
Note: 1. Serial Flash MX25V4006EWSK. For more information, see http://www.macronix.com.

2.2 SAM R21G

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMR21G16A-MF	64K	8K	QFN48	Tray
ATSAMR21G16A-MFT				Tape & Reel
ATSAMR21G16A-MU				Tray
ATSAMR21G16A-MUT				Tape & Reel
ATSAMR21G17A-MF	128K	16K	QFN48	Tray
ATSAMR21G17A-MFT				Tape & Reel
ATSAMR21G17A-MU				Tray
ATSAMR21G17A-MUT				Tape & Reel
ATSAMR21G18A-MF	256K	32K	QFN48	Tray
ATSAMR21G18A-MFT				Tape & Reel
ATSAMR21G18A-MU				Tray
ATSAMR21G18A-MUT				Tape & Reel

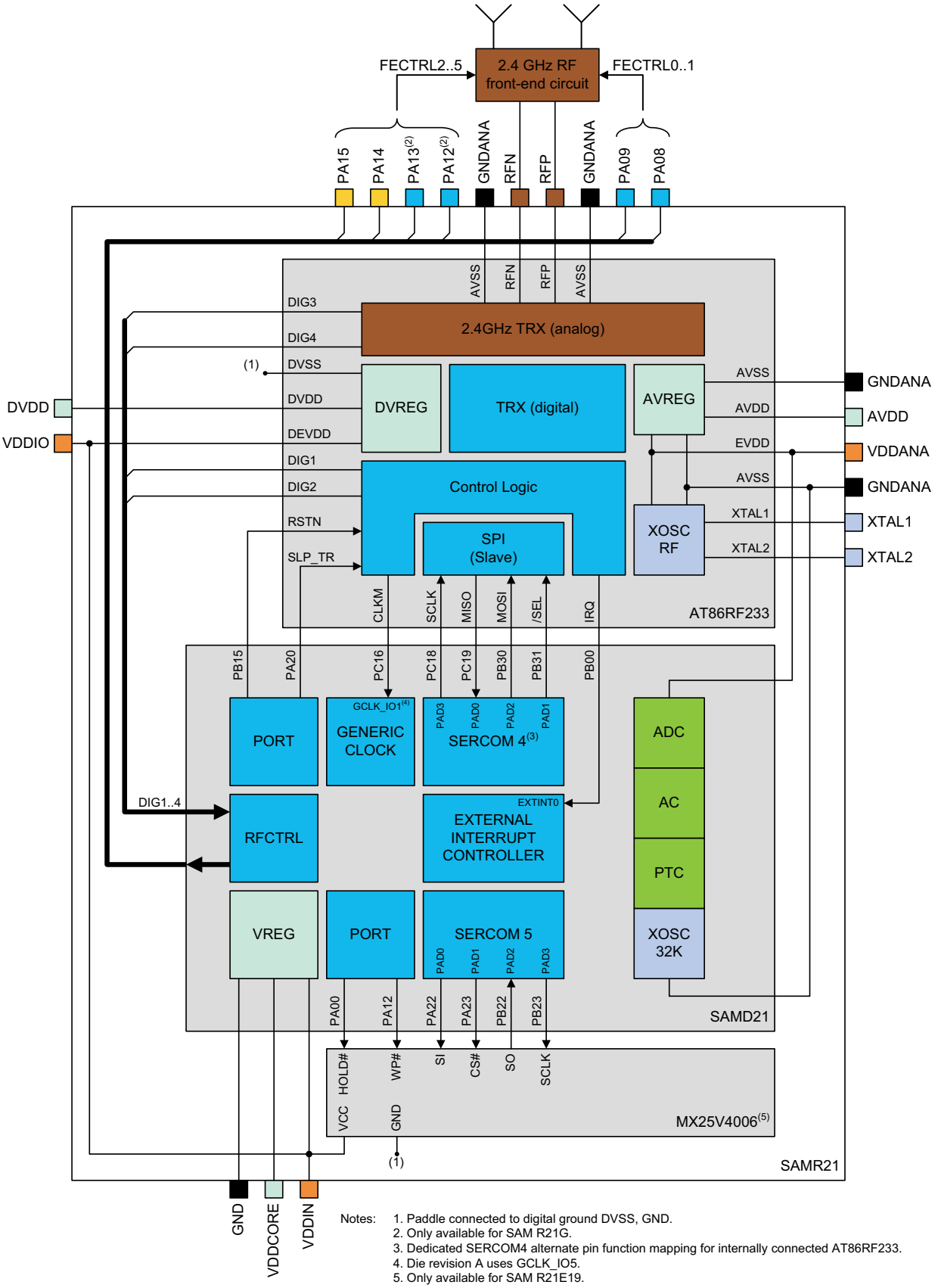
3. Block Diagrams

3.1 MCU Block Diagram



Notes:
1. Some products have different number of SERCOM instances, Timer/Counter instances, PTC signals and ADC signals. Refer to "Ordering Information" on page 6 for details.
2. The three TCC instances have different configurations, including the number of Waveform Output (WO) lines. Refer to "Peripherals Configuration Summary" on page 43 for details.
3. Refer to the PORT Function Multiplexing Table 5-1 for details about the available GCLK_IO and ADC signals.
4. Only available for SAM R21G.

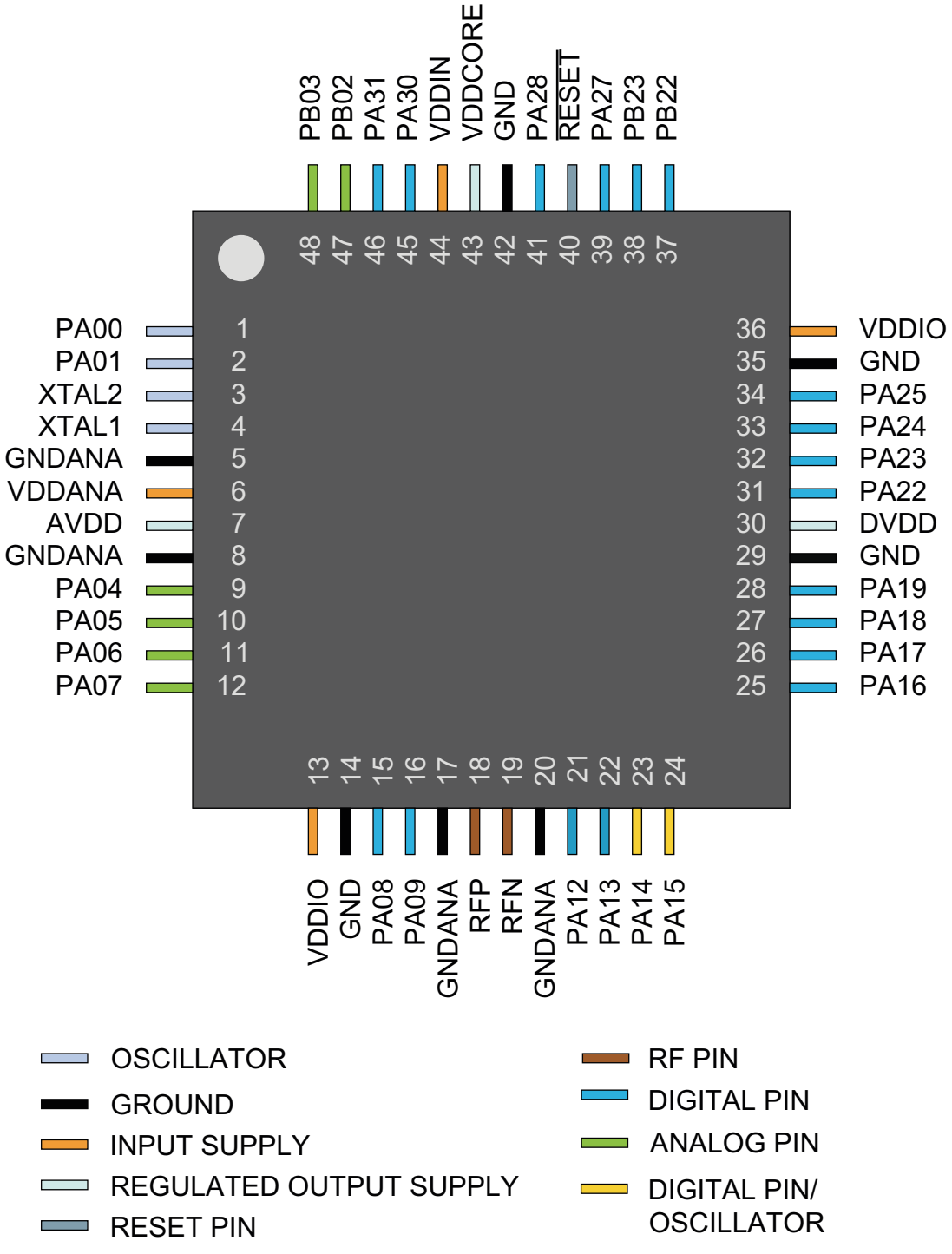
3.2 SAM R21 Interconnection



Notes:
1. Paddle connected to digital ground DVSS, GND.
2. Only available for SAM R21G.
3. Dedicated SERCOM4 alternate pin function mapping for internally connected AT86RF233.
4. Die revision A uses GCLK_IO5.
5. Only available for SAM R21E19.

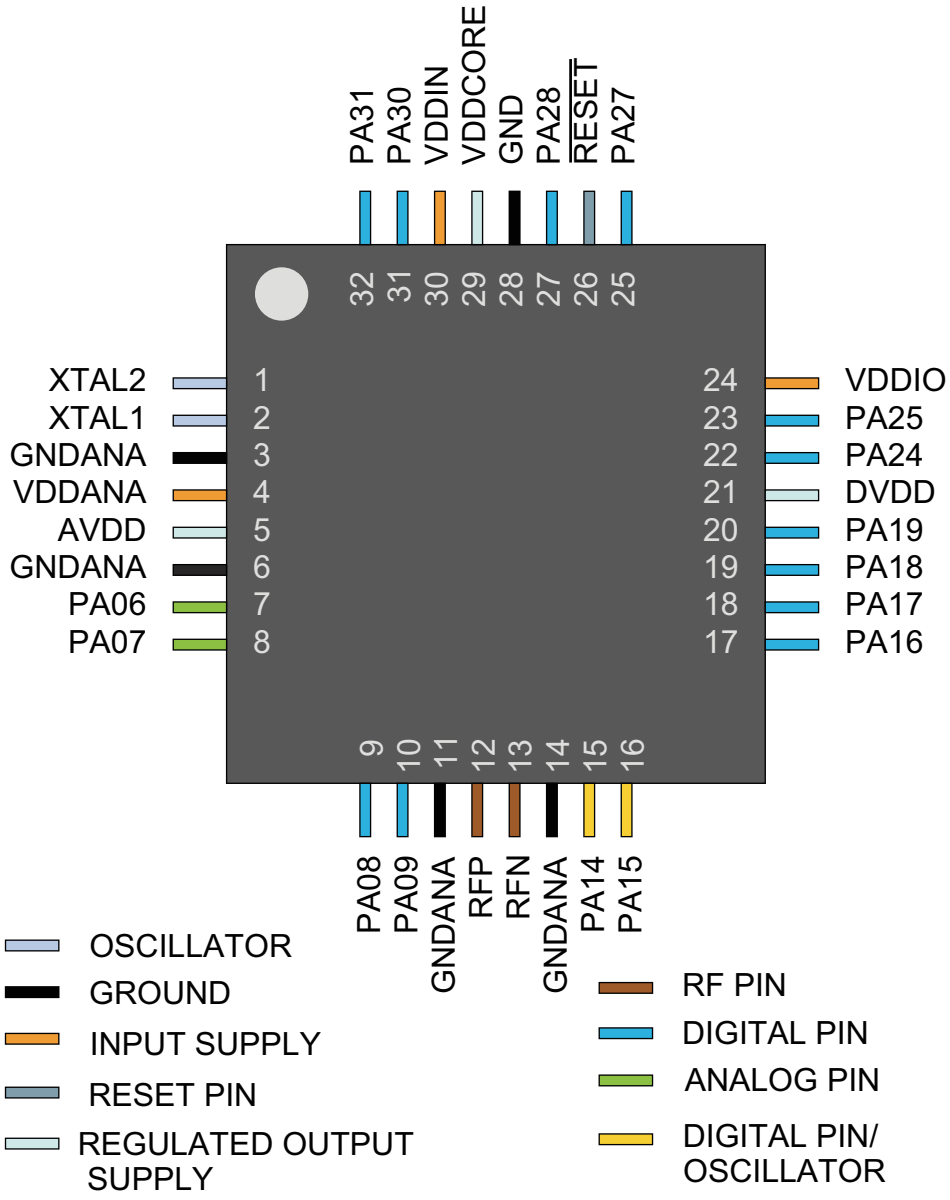
4. Pinout

4.1 SAM R21G - QFN48



Note: The large center pad underneath the QFN package is made of metal and internally connected to GND. It should be soldered and connected to the digital ground on the board to ensure good mechanical stability. It is not recommended to use the exposed paddle as a replacement of the regular GND pin.

4.2 SAM R21E - QFN32



Note: The large center pad underneath the QFN package is made of metal and internally connected to GND. It should be soldered and connected to the digital ground on the board to ensure good mechanical stability. It is not recommended to use the exposed paddle as a replacement of the regular GND pin.

5. I/O Multiplexing and Considerations

5.1 Multiplexed Signals

Each pin is by default controlled by the PORT as a general purpose I/O and alternatively it can be assigned to one of the peripheral functions A, B, C, D, E, F, G or H. To enable a peripheral function on a pin, the Peripheral Multiplexer Enable bit in the Pin Configuration register corresponding to that pin (PINCFGn.PMUXEN, n = 0..31) in the PORT must be written to one. The selection of peripheral function A to H is done by writing to the Peripheral Multiplexing Odd and Even bits in the Peripheral Multiplexing register (PMUXn.PMUXE/O) in the PORT.

Table 5-1 describes the peripheral signals multiplexed to the PORT I/O pins.

Table 5-1. PORT Function Multiplexing

Pin					A	B[1][2]				C	D	E	F	G	H
SAMR21E	SAMR21G	I/O Pin	Supply	Type	EIC	REF	ADC	AC	PTC	SERCOM[1][2]	SERCOM-ALT	TC TCC	FECTRL TCC SERCOM	COM	AC/ GCLK
	1	PA00	VDDANA								SERCOM1/ PAD[0]	TCC2/WO[0]			
	2	PA01	VDDANA		EXTINT[1]						SERCOM1/ PAD[1]	TCC2/WO[1]			
	9	PA04	VDDANA		EXTINT[4]	ADC/ VREFB	AIN[4]	AIN[0]	Y[2]		SERCOM0/ PAD[0]	TCC0/WO[0]			
	10	PA05	VDDANA		EXTINT[5]		AIN[5]	AIN[1]	Y[3]		SERCOM0/ PAD[1]	TCC0/WO[1]			
7	11	PA06	VDDANA		EXTINT[6]		AIN[6]	AIN[2]	Y[4]		SERCOM0/ PAD[2]	TCC1/WO[0]			
8	12	PA07	VDDANA		EXTINT[7]		AIN[7]	AIN[3]	Y[5]		SERCOM0/ PAD[3]	TCC1/WO[1]			
9	15	PA08	VDDIO	I^2C	NMI		AIN[16]		X[0]	SERCOM0/ PAD[0]	SERCOM2/ PAD[0]	TCC0/WO[0]	FECTRL[0]		
10	16	PA09	VDDIO	I^2C	EXTINT[9]		AIN[17]		X[1]	SERCOM0/ PAD[1]	SERCOM2/ PAD[1]	TCC0/WO[1]	FECTRL[1]		
	21	PA12	VDDIO	I^2C	EXTINT[12]					SERCOM2/ PAD[0]		TCC2/WO[0]	FECTRL[2]		AC/ CMP[0]
	22	PA13	VDDIO	I^2C	EXTINT[13]					SERCOM2/ PAD[1]		TCC2/WO[1]	FECTRL[3]		AC/ CMP[1]
15	23	PA14	VDDIO		EXTINT[14]					SERCOM2/ PAD[2]		TC3/WO[0]	FECTRL[4]		GCLK_IO[0]
16	24	PA15	VDDIO		EXTINT[15]					SERCOM2/ PAD[3]		TC3/WO[1]	FECTRL[5]		GCLK_IO[1]
17	25	PA16	VDDIO	I^2C					X[4]	SERCOM1/ PAD[0]	SERCOM3/ PAD[0]	TCC2/WO[0]	TCC0/ WO[0]		GCLK_IO[2]
18	26	PA17	VDDIO	I^2C	EXTINT[1]				X[5]	SERCOM1/ PAD[1]	SERCOM3/ PAD[1]	TCC2/WO[1]	TCC0/ WO[1]		GCLK_IO[3]
19	27	PA18	VDDIO		EXTINT[2]				X[6]	SERCOM1/ PAD[2]	SERCOM3/ PAD[2]	TC3/WO[0]	TCC0/ WO[2]		AC/ CMP[0]
20	28	PA19	VDDIO		EXTINT[3]				X[7]	SERCOM1/ PAD[3]	SERCOM3/ PAD[3]	TC3/WO[1]	TCC0/ WO[3]		AC/ CMP[1]
	31	PA22	VDDIO	I^2C	EXTINT[6]				X[10]	SERCOM3/ PAD[0]	SERCOM5/ PAD[0]	TC4/WO[0]	TCC0/ WO[4]		GCLK_IO[6]
	32	PA23	VDDIO	I^2C	EXTINT[7]				X[11]	SERCOM3/ PAD[1]	SERCOM5/ PAD[1]	TC4/WO[1]	TCC0/ WO[5]	USB/ SOF1kHz	GCLK_IO[7]
22	33	PA24	VDDIO		EXTINT[12]					SERCOM3/ PAD[2]	SERCOM5/ PAD[2]	TC5/WO[0]	TCC1/ WO[2]	USB_DM	
23	34	PA25	VDDIO		EXTINT[13]					SERCOM3/ PAD[3]	SERCOM5/ PAD[3]	TC5/WO[1]	TCC1/ WO[3]	USB_DP	

Table 5-1. PORT Function Multiplexing (Continued)

Pin		I/O Pin	Supply	Type	A	B[1][2]				C	D	E	F	G	H
SAMR21E	SAMR21G				EIC	REF	ADC	AC	PTC	SERCOM[1][2]	SERCOM-ALT	TC TCC	FECTRL TCC SERCOM	COM	AC/ GCLK
	37	PB22	VDDIO		EXTINT[6]						SERCOM5/ PAD[2]				GCLK_IO[0]
	38	PB23	VDDIO		EXTINT[7]						SERCOM5/ PAD[3]				GCLK_IO[1]
25	39	PA27	VDDIO		EXTINT[15]								SERCOM3/ PAD[0]		GCLK_IO[0]
27	41	PA28	VDDIO		EXTINT[8]								SERCOM3/ PAD[1]		GCLK_IO[0]
31	45	PA30	VDDIO		EXTINT[10]						SERCOM1/ PAD[2]	TCC1/WO[0]		SWCLK	GCLK_IO[0]
32	46	PA31	VDDIO		EXTINT[11]						SERCOM1/ PAD[3]	TCC1/WO[1]		SWDIO[3]	
	47	PB02	VDDANA		EXTINT[2]		AIN[10]		Y[8]		SERCOM5/ PAD[0]				
	48	PB03	VDDANA		EXTINT[3]		AIN[11]		Y[9]		SERCOM5/ PAD[1]				

Notes:
1. All analog pin functions are on peripheral function B. Peripheral function B must be selected to disable the digital control of the pin.
2. Only some pins can be used in SERCOM I^2C mode. See the Type column for using a SERCOM pin in I^2C mode. Refer to "Electrical Characteristics" on page 1055 for details on the I^2C pin characteristics.
3. This function is only activated in the presence of a debugger.

5.2 Internal Multiplexed Signals

PA20, PB00, PB15, PB30, PB31, PC16, PC18 and PC19 are by default controlled by the PORT as a general purpose I/O and alternatively it can be assigned to one of the peripheral functions A, B, C, D, E, F, G or H. To enable a peripheral function on a pin, the Peripheral Multiplexer Enable bit in the Pin Configuration register corresponding to that pin (PINCFGn.PMUXEN, n = 0-31) in the PORT must be written to one. The selection of peripheral function A to H is done by writing to the Peripheral Multiplexing Odd and Even bits in the Peripheral Multiplexing register (PMUXn.PMUXE/O) in the PORT.

PA10, PA11, PB16 and PB17 cannot be configured as output ports. These ports are always connected to the RFCTRL inputs.

Internal Signal	I/O Pin	Supply	Type	A	B				C	D	E	F	G	H
				EIC	REF	ADC	AC	PTC	SERCOM	SERCOM-ALT	TC	FECTRL TCC SERCOM	COM	AC/ GCLK
DIG3	PA10	VDDIO	Input	EXTINT[10]										
DIG4	PA11	VDDIO	Input	EXTINT[11]										
SLP_TR	PA20	VDDIO	I/O											
IRQ	PB00	VDDANA	I/O	EXTINT[0]										
RSTN	PB15	VDDIO	I/O											
DIG1	PB16	VDDIO	Input	EXTINT[0]										
DIG2	PB17	VDDIO	Input	EXTINT[1]										
MOSI	PB30	VDDIO	I/O									SERCOM4/ PAD[2]		
SEL	PB31	VDDIO	I/O									SERCOM4/ PAD[1]		

Internal Signal	I/O Pin	Supply	Type	A	B				C	D	E	F	G	H
				EIC	REF	ADC	AC	PTC	SERCOM	SERCOM-ALT	TC	FECTRL TCC SERCOM	COM	AC/ GCLK
CLKM	PC16	VDDIO	I/O									GCLK/ IO[1](1)		
SCLK	PC18	VDDIO	I/O									SERCOM4/ PAD[3]		
MISO	PC19	VDDIO	I/O									SERCOM4/ PAD[0]		

Note: 1. Die revision A uses GCLK/IO[5].

5.3 Other Functions

5.3.1 Oscillator Pinout

The oscillators are not mapped to the normal PORT functions and their multiplexing are controlled by registers in the System Controller (SYSCTRL). Refer to "SYSCTRL – System Controller" on page 143 for more information.

Oscillator	Supply	Signal	I/O Pin
XOSC	VDDIO	XIN	PA14
		XOUT	PA15
XOSC32K	VDDANA	XIN32	PA00
		XOUT32	PA01

The integrated AT86RF233 16 MHz crystal oscillator is directly connected to pins and has no multiplexing functionality.

Oscillator	Supply	Signal	I/O Pin
XOSCRF	EVDD/VDDANA	XTAL1	XTAL1
		XTAL2	XTAL2

5.3.2 Serial Wire Debug Interface Pinout

Only the SWCLK pin is mapped to the normal PORT functions. A debugger cold-plugging or hot-plugging detection will automatically switch the SWDIO port to the SWDIO function. Refer to "DSU – Device Service Unit" on page 45 for more information.

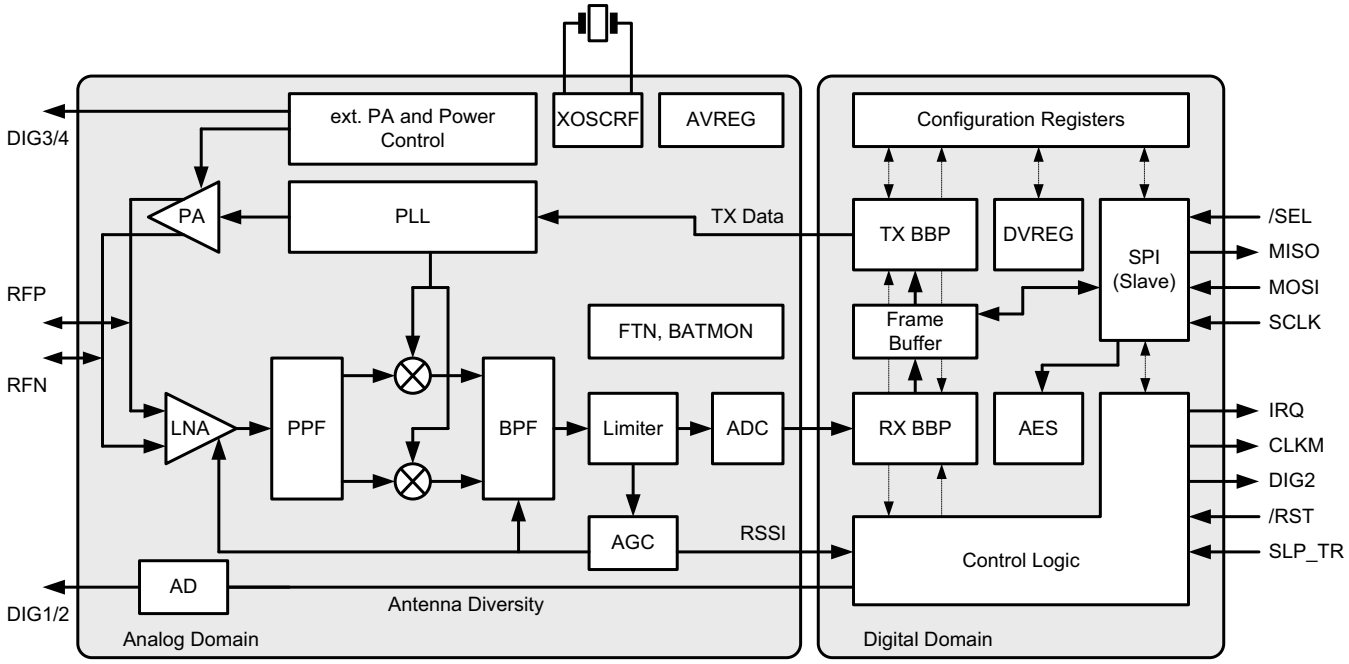
Signal	Supply	I/O Pin
SWCLK	VDDIO	PA30
SWDIO	VDDIO	PA31

5.3.3 General Circuit Description

The Atmel AT86RF233 single-chip radio transceiver provides a complete radio transceiver interface between an antenna and the SAM D21 microcontroller. It comprises the analog radio, digital modulation and demodulation including time and frequency synchronization, as well as data buffering. A single 128-byte TRX buffer stores receive or transmit data. Communication between transmitter and receiver is based on direct sequence spread spectrum with different modulation schemes and spreading codes.

The AT86RF233 block diagram is shown in Figure 5-1.

Figure 5-1. AT86RF233 Block Diagram



The number of external components is minimized such that only the antenna, the crystal and decoupling capacitors are required. The bidirectional differential antenna pins (RFP, RFN) are used for transmission and reception, thus no external antenna switch is needed. Control of an external power amplifier is supported by two digital control signals (differential operation).

The received RF signal at SAM R21 pin 13/19 (RFN) and pin 12/18 (RFP) is differentially fed through the low-noise amplifier (LNA) to the RF filter (PPF) to generate a complex signal, driving the integrated channel filter (BPF). The limiting amplifier provides sufficient gain to drive the succeeding analog-to-digital converter (ADC) and generates a digital RSSI signal. The ADC output signal is sampled by the digital base band receiver (RX BBP).

The transmit modulation scheme is offset-QPSK (O-QPSK) with half-sine pulse shaping and 32-length block coding (spreading) according to [1], [2] and [3]. The modulation signal is generated in the digital transmitter (TX BBP) and applied to the fractional-N frequency synthesis (PLL), to ensure the coherent phase modulation required for demodulation of O-QPSK signals. The frequency-modulated signal is fed to the power amplifier (PA).

Two on-chip low-dropout voltage regulators (A|DVREG) provide regulated analog and digital 1.8V supply outputs.

An internal 128-byte RAM for RX and TX (Frame Buffer) buffers the data to be transmitted or the received data.

The configuration of the internal AT86RF233, reading and writing of Frame Buffer is controlled by the SPI interface and additional control lines.

The AT86RF233 further contains comprehensive hardware-MAC support (Extended Operating Mode) and a security engine (AES) to improve the overall system power efficiency and timing. The stand-alone 128-bit AES engine can be

accessed in parallel to all PHY operational transactions and states using the SPI interface, except during SLEEP and DEEP_SLEEP states.

For long-range applications or to improve the reliability of a RF connection the RF performance can further be improved by using an external RF front-end or Antenna Diversity. Both operation modes are supported by the AT86RF233 with dedicated control signals DIG1, …, DIG4 which can be activated as alternate pin output functions FECTRL[0..5] by the integrated microcontroller.

Additional features of the Extended Feature Set, see “AT86RF233 Extended Feature Set” on page 1005, are provided to simplify the interaction between radio transceiver and microcontroller.

5.4 Analog and RF Pins

5.4.1 Supply and Ground Pins

5.4.1.1 EVDD, DEVDD

EVDD and DEVDD are analog and digital supply voltage pins of the AT86RF233 radio transceiver.

5.4.1.2 AVDD, DVDD

AVDD and DVDD are outputs of the internal voltage regulators and require bypass capacitors for stable operation. The voltage regulators are controlled independently by the radio transceivers state machine and are activated depending on the current radio transceiver state. The voltage regulators can be configured for external supply; for details, refer to “Voltage Regulators (AVREG, DVREG)” on page 983.

5.4.1.3 AVSS, DVSS

AVSS and DVSS are analog and digital ground pins respectively. The analog and digital power domains should be separated on the PCB.

5.4.2 RF Pins

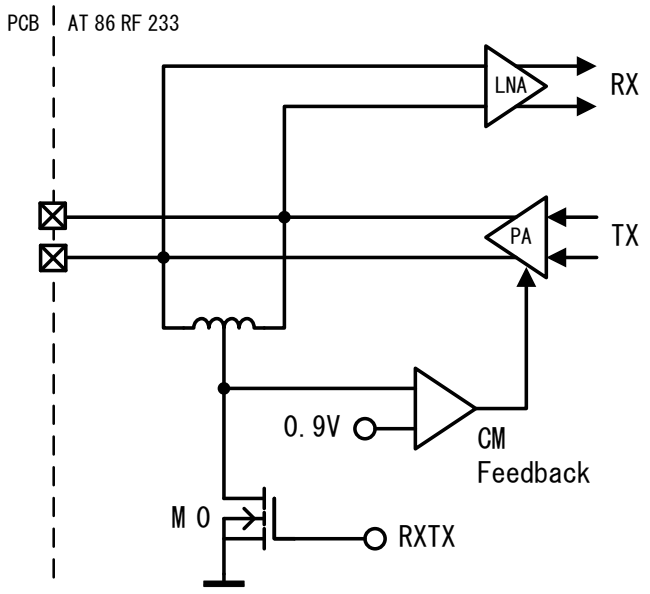
5.4.2.1 RFN, RFP

A differential RF port (RFP/RFN) provides common-mode rejection to suppress the switching noise of the internal digital signal processing blocks. At board-level, the differential RF layout ensures high receiver sensitivity by reducing spurious emissions originated from other digital ICs such as a microcontroller.

The RF port is designed for a 100Ω differential load. A DC path between the RF pins is allowed; a DC path to ground or supply voltage is not allowed.

A simplified schematic of the RF front end is shown in Figure 5-2.

Figure 5-2. Simplified RF Front-end Schematic.



The RF port DC values depend on the operating state; refer to “AT86RF233 Operating Modes” on page 902. In TRX_OFF state, when the analog front-end is disabled (see “TRX_OFF – Clock State” on page 904), the RF pins are pulled to ground, preventing a floating voltage larger than 1.8V which is not allowed for the internal circuitry.

In transmit mode, a control loop provides a common-mode voltage of 0.9V. Transistor M0 is off, allowing the PA to set the common-mode voltage. The common-mode capacitance at each pin to ground shall be < 30pF to ensure the stability of this common-mode feedback loop.

In receive mode, the RF port provides a low-impedance path to ground when transistor M0, (see Figure 5-2) pulls the inductor center tap to ground. A DC voltage drop of 20mV across the on-chip inductor can be measured at the RF pins.

5.4.3 Crystal Oscillator Pins

5.4.3.1 XTAL1, XTAL2

The pin 2/4 (XTAL1) of SAM R21 is the input of the reference oscillator amplifier (XOSCRF), the pin 1/3 (XTAL2) is the output. A detailed description of the crystal oscillator setup and the related XTAL1/XTAL2 pin configuration can be found in “Crystal Oscillator (XOSCRF)” on page 989.

When using an external clock reference signal, XTAL1 shall be used as input pin. For further details, refer to “External Reference Frequency Setup” on page 990.

5.4.4 Analog Pin Summary

Table 5-2. Analog Pin Behavior - DC values

Pin	Values and Conditions	Description
RFP/RFN	V_{DC} = 0.9V (BUSY_TX) V_{DC} = 20mV (receive states) V_{DC} = 0mV (otherwise)	DC level at pins RFP/RFN for various transceiver states. AC coupling is required if a circuitry with a DC path to ground or supply is used. Serial capacitance and capacitance of each pin to ground must be < 30pF.
XTAL1/XTAL2	V_{DC} = 0.9V at both pins C_{PAR} = 3pF	DC level at pins XTAL1/XTAL2 for various transceiver states. Parasitic capacitance (C_{PAR}) of the pins must be considered as additional load capacitance to the crystal.
DVDD	V_{DC} = 1.8V (all states, except SLEEP and DEEP_SLEEP) V_{DC} = 0mV (DEEP_SLEEP) V_{DC} = 1.5V (SLEEP)	DC level at pin DVDD for various transceiver states. Supply pins (voltage regulator output) for the digital 1.8V voltage domain. The outputs shall be bypassed by 100nF.
AVDD	V_{DC} = 1.8V (all states, except P_ON, SLEEP, DEEP_SLEEP, RESET, and TRX_OFF) V_{DC} = 0mV (otherwise)	DC level at pin AVDD for various transceiver states. Supply pin (voltage regulator output) for the analog 1.8V voltage domain. The outputs shall be bypassed by 100nF.

5.5 Digital I/O Signals

The AT86RF233 provides a digital microcontroller interface. The interface comprises a slave SPI (/SEL, SCLK, MOSI, and MISO) and additional control signals (CLKM, IRQ, SLP_TR, /RST, and DIG2). The microcontroller interface is described in detail in “AT86RF233 Microcontroller Interface” on page 883.

Additional digital output signals DIG1, …, DIG4 are provided to control external blocks, that is for Antenna Diversity RF switch control or as an RX/TX Indicator, see “Antenna Diversity” on page 1020 and “RX/TX Indicator” on page 1025 respectively.

5.5.1 Driver Strength Settings

The driver strength of all digital output signals (MISO, IRQ, DIG1,..., DIG4 and CLKM) to the microcontroller are fixed.

5.5.2 Pull-up and Pull-down Configuration

Pulling transistors are internally connected to all digital inputs from the microcontroller in radio transceiver states P_ON (including reset during P_ON) and DEEP_SLEEP, refer to “P_ON – Power-On after VDD” on page 903 and “DEEP_SLEEP – Deep Sleep State” on page 904.

Table 5-3 summarizes the pull-up and pull-down configuration.

Table 5-3. Pull-Up / Pull-Down Configuration of Digital Input Signals from the Microcontroller

Signal	H = pull-up, L = pull-down
/RST	H
/SEL	H
SCLK	L
MOSI	L
SLP_TR(1))	L

Note: 1. Except SLP_TR pin for DEEP_SLEEP state.

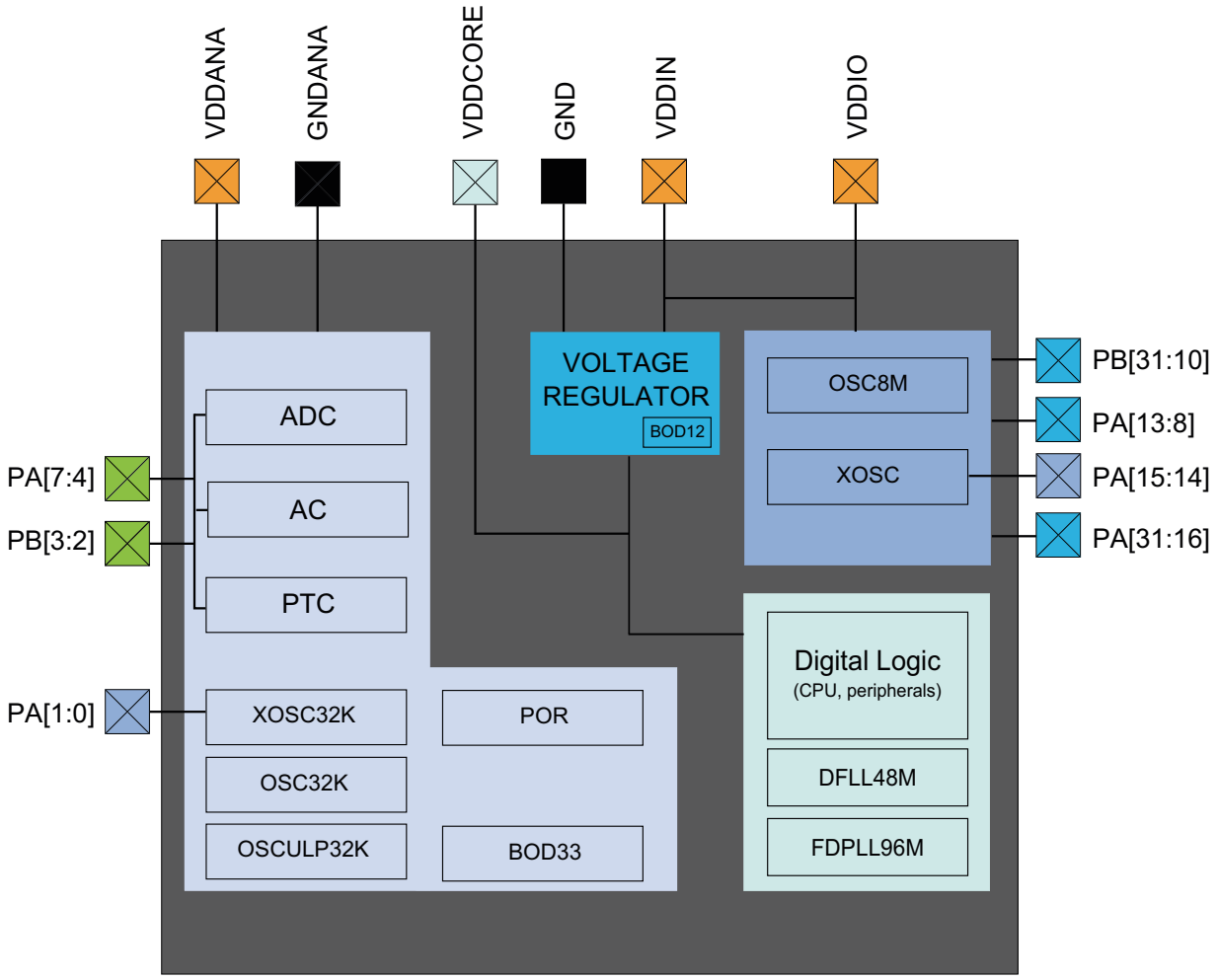
In all other radio transceiver states, including RESET, no pull-up or pull-down transistors are connected to any of the digital inputs mentioned in Table 5-3.

In all other states, external circuitry should guaranty defined levels at all input pins. Floating input signals may cause unexpected functionality and increased power consumption, for example in SLEEP state.

If the additional digital output signals DIG1, …, DIG4 are not activated, they are pulled-down to digital ground (DIG1/DIG2) or analog ground (DIG3/DIG4).

6. Power Supply and Start-Up Considerations

6.1 Power Domain Overview



6.2 Power Supply Considerations

6.2.1 Power Supplies

The Atmel® SAM R21 has several different power supply pins:

- VDDIO: Powers I/O lines, OSC8M and XOSC. Voltage is 1.8V to 3.6V.
- VDDIN: Powers I/O lines, the internal regulator and the stacked 512KB serial Flash. Voltage is 1.8V to 3.6V.
- VDDANA: Powers I/O lines and the ADC, AC, PTC, OSCULP32K, OSC32K, XOSC32K. Voltage is 1.8V to 3.6V.
- VDDCORE: Internal regulated voltage output. Powers the core, memories, peripherals, DFLL48M and FDPLL96M. Voltage is 1.2V.

The same voltage must be applied to both VDDIN, VDDIO and VDDANA. This common voltage is referred to as V_{DD} in the datasheet.

The ground pins, GND, are common to VDDCORE, VDDIO and VDDIN. The ground pin for VDDANA is GNDANA.

For decoupling recommendations for the different power supplies, refer to the schematic checklist.

Refer to “Schematic Checklist” on page 1112 for details.

6.2.2 Voltage Regulator

The SAM R21 voltage regulator has two different modes:

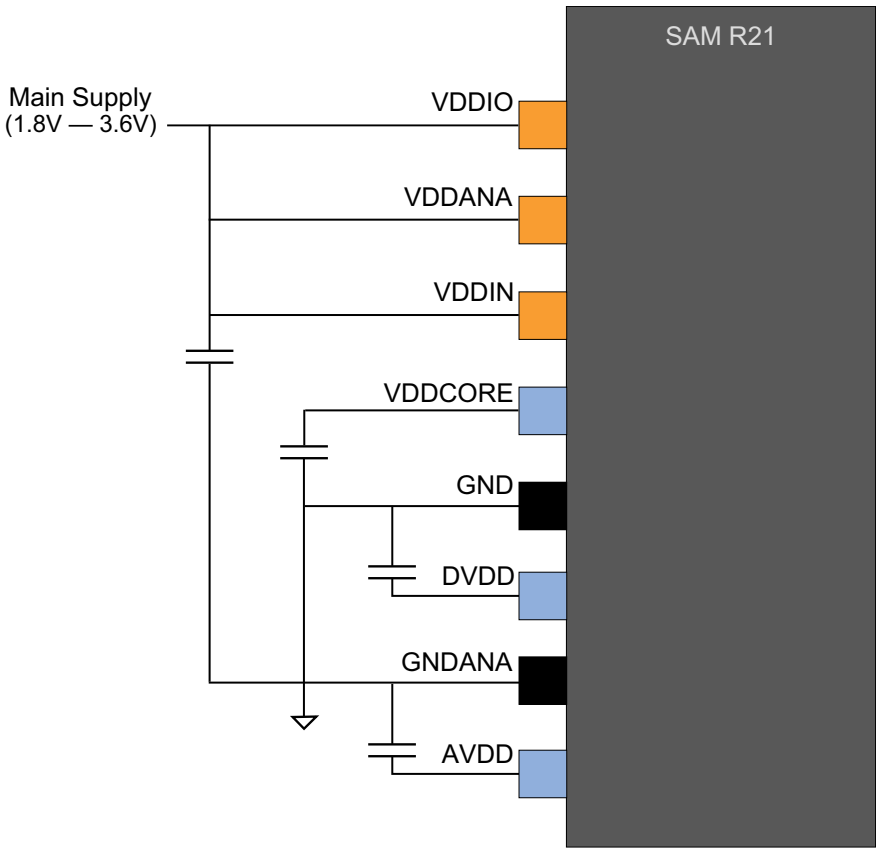
- Normal mode: To be used when the CPU and peripherals are running
- Low Power (LP) mode: To be used when the regulator draws small static current. It can be used in standby mode

6.2.3 Typical Powering Schematics

The SAM R21 uses a single supply from 1.8V to 3.6V.

The following figure shows the recommended power supply connection.

Figure 6-1. Power Supply Connection



6.2.4 Power-Up Sequence

6.2.4.1 Minimum Rise Rate

The integrated power-on reset (POR) circuitry monitoring the VDDANA power supply requires a minimum rise rate. Refer to the “Electrical Characteristics” on page 1055 for details.

6.2.4.2 Maximum Rise Rate

The rise rate of the power supply must not exceed the values described in Electrical Characteristics. Refer to the “Electrical Characteristics” on page 1055 for details.

6.3 Power-Up

This section summarizes the power-up sequence of the SAM R21. The behavior after power-up is controlled by the Power Manager. Refer to “PM – Power Manager” on page 112 for details.

6.3.1 Starting of Clocks

After power-up, the device is set to its initial state and kept in reset, until the power has stabilized throughout the device. Once the power has stabilized, the device will use a 1MHz clock. This clock is derived from the 8MHz Internal Oscillator (OSC8M), which is divided by eight and used as a clock source for generic clock generator 0. Generic clock generator 0 is the main clock for the Power Manager (PM).

Some synchronous system clocks are active, allowing software execution.

Refer to the “Clock Mask Register” section in “PM – Power Manager” on page 112 for the list of default peripheral clocks running. Synchronous system clocks that are running are by default not divided and receive a 1MHz clock through generic clock generator 0. Other generic clocks are disabled except GCLK_WDT, which is used by the Watchdog Timer (WDT).

6.3.2 I/O Pins

After power-up, the I/O pins are tri-stated.

6.3.3 Fetching of Initial Instructions

After reset has been released, the CPU starts fetching PC and SP values from the reset address, which is 0x00000000. This address points to the first executable address in the internal flash. The code read from the internal flash is free to configure the clock system and clock sources. Refer to “PM – Power Manager” on page 112, “GCLK – Generic Clock Controller” on page 90 and “SYSCTRL – System Controller” on page 143 for details. Refer to the ARM Architecture Reference Manual for more information on CPU startup (http://www.arm.com).

6.4 Power-On Reset and Brown-Out Detector

The SAM R21 embeds three features to monitor, warn and/or reset the device:

- POR: Power-on reset on VDDANA
- BOD33: Brown-out detector on VDDANA
- BOD12: Voltage Regulator Internal Brown-out detector on VDDCORE. The Voltage Regulator Internal BOD is calibrated in production and its calibration configuration is stored in the NVM User Row. This configuration should not be changed if the user row is written to assure the correct behavior of the BOD12.

6.4.1 Power-On Reset on VDDANA

POR monitors VDDANA. It is always activated and monitors voltage at startup and also during all the sleep modes. If VDDANA goes below the threshold voltage, the entire chip is reset.

6.4.2 Brown-Out Detector on VDDANA

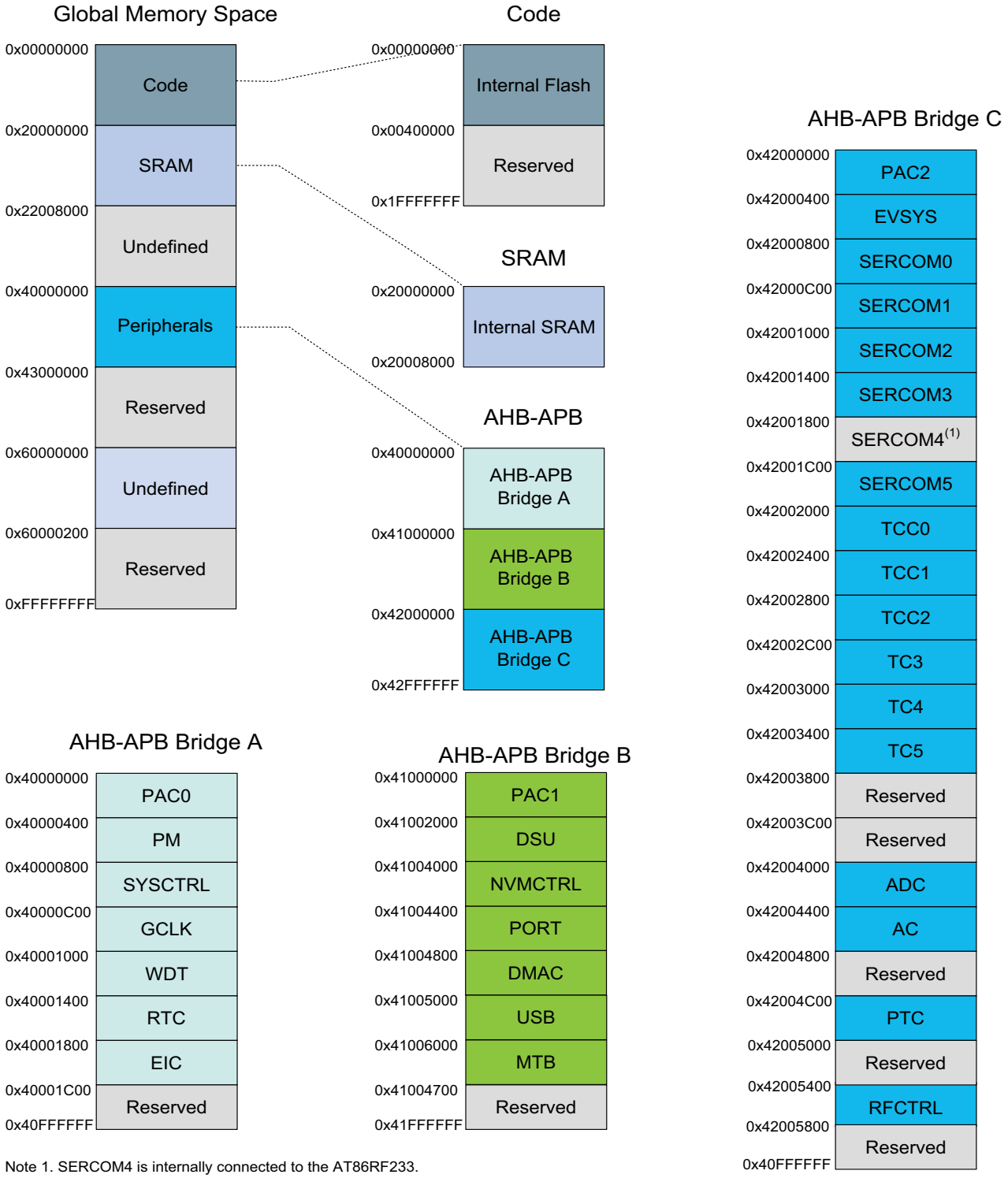
BOD33 monitors VDDANA. Refer to “SYSCTRL – System Controller” on page 143 for details.

6.4.3 Brown-Out Detector on VDDCORE

Once the device has started up, BOD12 monitors the internal VDDCORE.

7. Product Mapping

Figure 7-1. Atmel | SMART SAM R21 Product Mapping



Note 1. SERCOM4 is internally connected to the AT86RF233.

This figure represents the full configuration of the Atmel | SMART SAM R21 with maximum Flash and SRAM capabilities and a full set of peripherals. Refer to the "Configuration Summary" on page 4 for details.

8. Memories

8.1 Embedded Memories

- Internal high-speed flash
- Internal high-speed RAM, single-cycle access at full speed
- Stacked 512KB serial Flash (SAMR21E19A)

8.2 Physical Memory Map

The High-Speed bus is implemented as a bus matrix. All High-Speed bus addresses are fixed, and they are never remapped in any way, even during boot. The 32-bit physical address space is mapped as follow:

Table 8-1. SAM R21 physical memory map(1)

Memory	Start address	Size			
		SAMR21x19	SAMR21x18	SAMR21x17	SAMR21x16
Embedded Flash	0x00000000	256Kbytes	256Kbytes	128Kbytes	64Kbytes
Embedded SRAM	0x20000000	32Kbytes	32Kbytes	16Kbytes	8Kbytes
Peripheral Bridge A	0x40000000	64Kbytes	64Kbytes	64Kbytes	64Kbytes
Peripheral Bridge B	0x41000000	64Kbytes	64Kbytes	64Kbytes	64Kbytes
Peripheral Bridge C	0x42000000	64Kbytes	64Kbytes	64Kbytes	64Kbytes

Note: 1. x = G or E. Refer to "Ordering Information" on page 6 for details.

Table 8-2. Flash memory parameters(1)

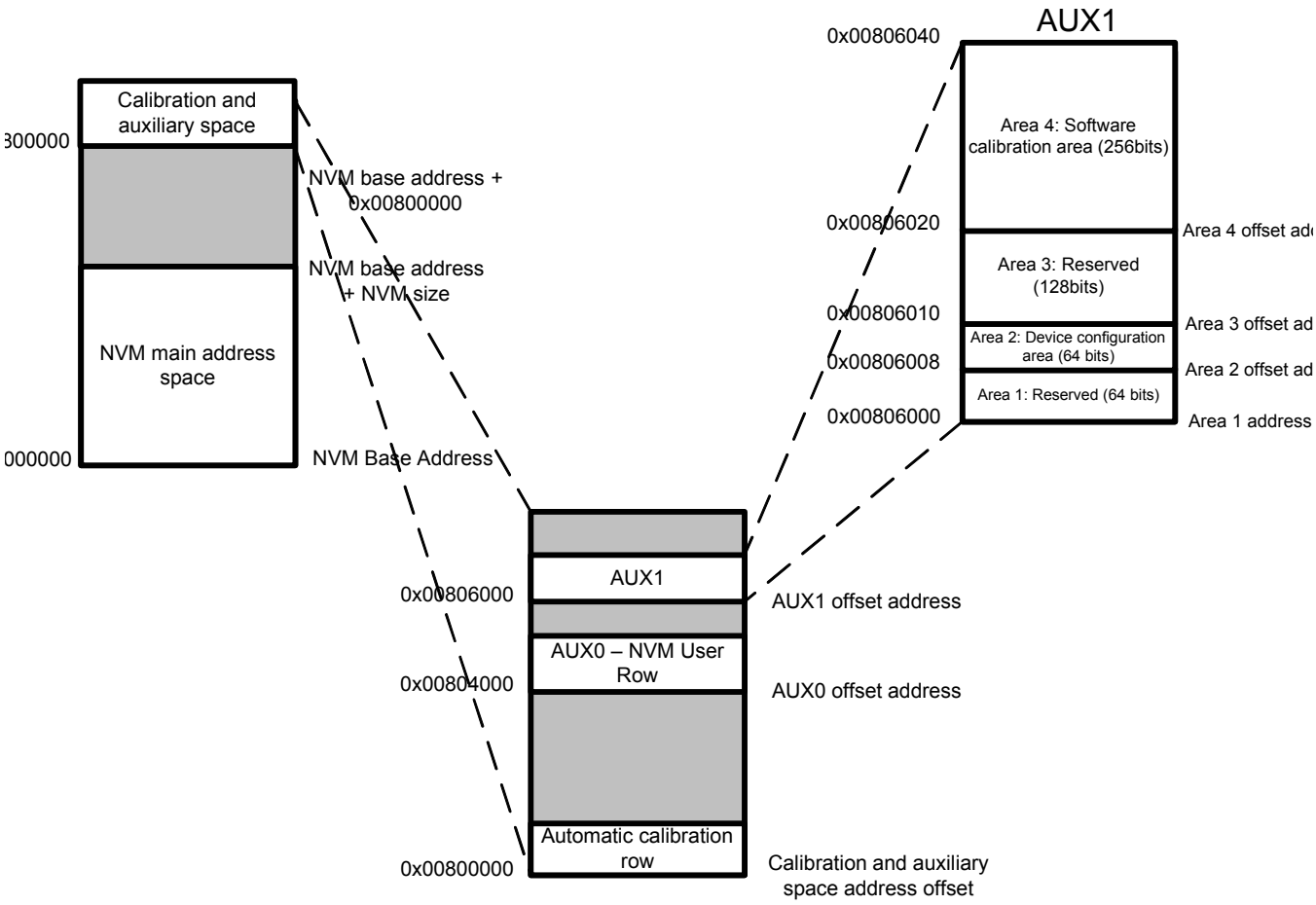
Device	Flash size	Number of pages	Page size
SAMR21x19(3)	256Kbytes	4096	64 bytes
SAMR21x18	256Kbytes	4096	64 bytes
SAMR21x17	128Kbytes	2046	64 bytes
SAMR21x16	64Kbytes	1024	64 bytes

Note: 1. x = G or E. Refer to "Ordering Information" on page 6 for details.
2. The number of pages (NVMP) and page size (PSZ) can be read from the NVM Pages and Page Size bits in the NVM Parameter register in the NVMCTRL (PARAM.NVMP and PARAM.PSZ, respectively). Refer to PARAM for details.
3. The Flash memory parameters refers to the embedded memories: SAMR21x19 shares same embedded memories as SAMR21x18.

8.3 NVM Calibration and Auxiliary Space

The device calibration data are stored in different sections of the NVM calibration and auxiliary space presented in Figure 8-1.

Figure 8-1. Calibration and Auxiliary Space



The values from the automatic calibration row are loaded into their respective registers at startup.

8.3.1 NVM User Row Mapping

The NVM User Row contains calibration data that are automatically read at device power on.

The NVM User Row can be read at address 0x804000.

To write the NVM User Row refer to “NVMCTRL – Non-Volatile Memory Controller” on page 350.

Note that when writing to the user row the values do not get loaded by the other modules on the device until a device reset occurs.