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SAM E70/S70/V70/V71 Family

32-bit ARM Cortex-M7 MCUs with FPU, Audio and Graphics Interfaces, High-Speed USB, Ethernet, and Advanced Analog

Features

Core

- ARM® Cortex®-M7 running at up to 300 MHz
- 16 Kbytes of I-Cache and 16 Kbytes of D-Cache with Error Code Correction (ECC)
- Single-precision and double-precision HW Floating Point Unit (FPU)
- Memory Protection Unit (MPU) with 16 zones
- DSP Instructions, Thumb®-2 Instruction Set
- Embedded Trace Module (ETM) with instruction trace stream, including Trace Port Interface Unit (TPIU)

Memories

- Up to 2048 Kbytes embedded Flash with unique identifier and user signature for user-defined data
- Up to 384 Kbytes embedded Multi-port SRAM
- Tightly Coupled Memory (TCM)
- 16 Kbytes ROM with embedded Bootloader routines (UART0, USB) and IAP routines
- 16-bit Static Memory Controller (SMC) with support for SRAM, PSRAM, LCD module, NOR and NAND Flash with on-the-fly scrambling
- 16-bit SDRAM Controller (SDRAMC) interfacing up to 256 MB and with on-the-fly scrambling

System

- Embedded voltage regulator for single-supply operation
- Power-on-Reset (POR), Brown-out Detector (BOD) and Dual Watchdog for safe operation
- Quartz or ceramic resonator oscillators: 3 to 20 MHz main oscillator with failure detection, 12 MHz or 16 MHz needed for USB operations. Optional low-power 32.768 kHz for RTC or device clock
- RTC with Gregorian calendar mode, waveform generation in low-power modes
- RTC counter calibration circuitry compensates for 32.768 kHz crystal frequency variations
- 32-bit low-power Real-time Timer (RTT)
- High-precision Main RC oscillator with 12 MHz default frequency.
- 32.768 kHz crystal oscillator or Slow RC oscillator as source of low-power mode device clock (SLCK)
- One 500 MHz PLL for system clock, one 480 MHz PLL for USB high-speed operations
- Temperature Sensor
- One dual-port 24-channel central DMA Controller (XDMAC)

Low-Power Features

- Low-power Sleep, Wait and Backup modes, with typical power consumption down to 1.1 µA in Backup mode with RTC, RTT and wakeup logic enabled
- Ultra low-power RTC and RTT
- 1 Kbyte of backup RAM (BRAM) with dedicated regulator

Peripherals

- One Ethernet MAC (GMAC) 10/100 Mbps in MII mode and RMII with dedicated DMA. IEEE1588 PTP frames and 802.3az Energy-efficiency support. Ethernet AVB support with IEEE802.1AS Timestamping and IEEE802.1Qav credit-based traffic-shaping hardware support.
- USB 2.0 Device/Mini Host High-speed (USBHS) at 480 Mbps, 4-Kbyte FIFO, up to 10 bidirectional endpoints, dedicated DMA
- 12-bit ITU-R BT. 601/656 Image Sensor Interface (ISI)
- Two master Controller Area Networks (MCAN) with Flexible Data Rate (CAN-FD) with SRAM-based mailboxes, time- and event-triggered transmission
- MediaLB® device with 3-wire mode, up to 1024 x Fs speed, supporting MOST25 and MOST50 networks
- Three USARTs. USART0/1/2 support LIN mode, ISO7816, IrDA®, RS-485, SPI, Manchester and Modem modes; USART1 supports LON mode.
- Five 2-wire UARTs with SleepWalking™ support
- Three Two-Wire Interfaces (TWIHS) (I^2C-compatible) with SleepWalking support
- Quad I/O Serial Peripheral Interface (QSPI) interfacing up to 256 MB Flash and with eXecute-In-Place and on-the-fly scrambling
- Two Serial Peripheral Interfaces (SPI)
- One Serial Synchronous Controller (SSC) with I^2S and TDM support
- Two Inter-IC Sound Controllers (I2SC)
- One High-speed Multimedia Card Interface (HSMCI) (SDIO/SD Card/e.MMC)
- Four Three-Channel 16-bit Timer/Counters (TC) with Capture, Waveform, Compare and PWM modes, constant on time. Quadrature decoder logic and 2-bit Gray Up/Down Counter for stepper motor
- Two 4-channel 16-bit PWMs with complementary outputs, Dead Time Generator and eight fault inputs per PWM for motor control, two external triggers to manage power factor correction (PFC), DC-DC and lighting control.
- Two Analog Front-End Controllers (AFEC), each supporting up to 12 channels with differential input mode and programmable gain stage, allowing dual sample-and-hold at up to 1.7 Msps. Offset and gain error correction feature.
- One 2-channel 12-bit 1 Msps-per-channel Digital-to-Analog Controller (DAC) with Differential and Over Sampling modes
- One Analog Comparator Controller (ACC) with flexible input selection, selectable input hysteresis

Cryptography

- True Random Number Generator (TRNG)
- AES: 256-, 192-, 128-bit Key Algorithm, Compliant with FIPS PUB-197 Specifications
- Integrity Check Monitor (ICM). Supports Secure Hash Algorithm SHA1, SHA224 and SHA256.

I/O

- Up to 114 I/O lines with external interrupt capability (edge- or level-sensitivity), debouncing, glitch filtering and On-die Series Resistor Termination
- Five Parallel Input/Output Controllers (PIO)

Voltage

- Single supply voltage from 3.0V to 3.6V for Qualification AEC - Q100 Grade 2 Devices
- Single Supply voltage from 1.7V to 3.6V for Industrial Temperature Devices

Packages

- LQFP144, 144-lead LQFP, 20x20 mm, pitch 0.5 mm
- LFBGA144, 144-ball LFBGA, 10x10 mm, pitch 0.8 mm
- TFBGA144, 144-ball TFBGA, 10x10mm, pitch 0.8 mm
- UFBGA144, 144-ball UFBGA, 6x6 mm, pitch 0.4 mm
- LQFP100, 100-lead LQFP, 14x14 mm, pitch 0.5 mm
- TFBGA100, 100-ball TFBGA, 9x9 mm, pitch 0.8 mm
- VFBGA100, 100-ball VFBGA, 7x7 mm, pitch 0.65 mm
- LQFP64, 64-lead LQFP, 10x10 mm, pitch 0.5 mm
- QFN64, 64-pad QFN 9x9 mm, pitch 0.5 mm, with wettable flanks

Table of Contents

1. Configuration Summary

The SAM E70/S70/V70/V71 devices differ in memory size, package and features. The following tables summarize the different configurations.

Table 1-1. SAM V71 Family Features (With CAN-FD, Ethernet AVB and Media LB)

Device	Flash Memory (KB)	Multi-port SRAM Memory (KB)	Pins	Packages	Digital Peripherals																					Analog		
					USB (see Note)	USART/UART	QSPI	USART/SPI	TWIHS	HSMCI port/bits	CAN-FD	Ethernet AVB	Media LB	Image Sensor Interface (ISI)	SPI0	SPI1	External Bus Interface (EBI)	SDRAM Interface	DMA Channels	SSC	ETM	Timer Counter Channels	Timer Counter Channels I/O	I2SC	I/O Pins	12-bit ADC Channels	Analog Comparators	DAC (Channels)
SAMV71Q19	512	256	144	LQFP, TFBGA	HS	3/5	Y	3	3	1/4	2	MII, RMII	Y	12 - bit	Y	Y	Y	Y	24	Y	Y	12	36	2	114	24	Y	2
SAMV71Q20	1024	384																										
SAMV71Q21	2048																											
SAMV71N19	512	256	100	LQFP, TFBGA	HS	3/5	Y	3	3	1/4	2	MII, RMII	Y	12 - bit	Y	N	N	N	24	Y	Y	12	9	1	75	10	Y	2
SAMV71N20	1024	384																										
SAMV71N21	2048																											
SAMV71J19	512	256	64	LQFP	FS	2/3	SPI only	0	2	N	1	RMII	Y	8-bit	N	N	N	N	24	Y	Y	12	3	0	44	5	Y	1
SAMV71J20	1024	384																										
SAMV71J21	2048																											

Note: HS = High-Speed; FS = Full-Speed.

Table 1-2. SAM E70 Family Features (With CAN-FD and Ethernet AVB)

Device	Flash Memory (KB)	Multi-port SRAM Memory (KB)	Pins	Packages	Digital Peripherals																				Analog		
					USB (see Note)	USART/UART	QSPI	USART/SPI	TWIHS	HSMCI port/bits	CAN-FD	Ethernet AVB	Image Sensor Interface (ISI)	SPI0	SPI1	External Bus Interface (EBI)	SDRAM Interface	DMA Channels	SSC	ETM	Timer Counter Channels	Timer Counter Channels I/O	I2SC	I/O Pins	12-bit ADC Channels	Analog Comparators	DAC (Channels)
SAME70Q19	512	256	144	LQFP, LFBGA, UFBGA	HS	3/5	Y	3	3	1/4	2	MII, RMII	12 -bit	Y	Y	Y	Y	24	Y	Y	12	36	2	114	24	Y	2
SAME70Q20	1024	384																									
SAME70Q21	2048																										
SAME70N19	512	256	100	LQFP, TFBGA	HS	3/5	Y	3	3	1/4	2	MII, RMII	12 -bit	Y	N	N	N	24	Y	Y	12	9	1	75	10	Y	2
SAME70N20	1024	384																									
SAME70N21	2048																										
SAME70J19	512	256	64	LQFP	FS	2/3	SPI only	0	2	N	1	RMII	8-bit	N	N	N	N	24	Y	Y	12	3	0	44	5	Y	1
SAME70J20	1024	384																									
SAME70J21	2048																										

Note: HS = High-Speed; FS = Full-Speed.

Table 1-3. SAM V70 Family Features (Without CAN-FD, Ethernet Control)

Device	Flash Memory (KB)	Multi-port SRAM Memory (KB)	Pins	Packages	Digital Peripherals																					Analog		
					USB (see Note	USART/UART	QSPI	USART/SPI	TWIHS	HSMCI port/bits	CAN-FD	Media LB	Image Sensor Interface (ISI)	SPI0	SPI1	External Bus Interface (EBI)	SDRAM Interface	DMA Channels	SSC	ETM	Timer Counter Channels	Timer Counter Channels I/O	I2SC	I/O Pins	12-bit ADC Channels	Analog Comparators	DAC (Channels)
SAMV70Q19	512	256	144	LQFP, TFBGA	HS	3/5	Y	3	3	1/4	2	Y	12 -bit	Y	Y	Y	Y	24	Y	Y	12	36	2	114	24	Y	2
SAMV70Q20	1024	384																									
SAMV70N19	512	256	100	LQFP, TFBGA	HS	3/5	Y	3	3	1/4	2	Y	12 -bit	Y	N	N	N	24	Y	Y	12	9	1	75	10	Y	2
SAMV70N20	1024	384																									
SAMV70J19	512	256	64	LQFP	FS	2/3	SPI only	0	2	N	1	N	8-bit	N	N	N	N	24	Y	Y	12	3	0	44	5	Y	1
SAMV70J20	1024	384																									

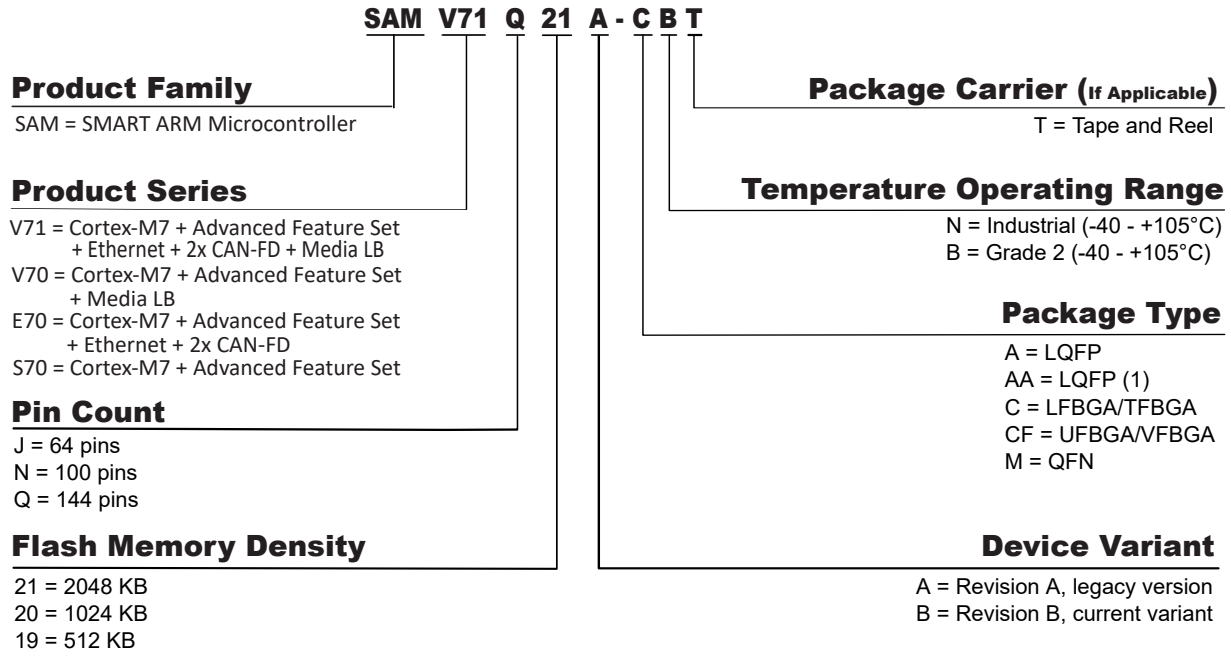
Note: HS = High-Speed; FS = Full-Speed.

Table 1-4. SAM S70 Family Features (Without CAN-FD, Ethernet AVB and Media LB)

Device	Flash Memory (KB)	Multi-port SRAM Memory (KB)	Pins	Packages	Digital Peripherals																		Analog		
					USB (see Note)	USART/UART	QSPI	USART/SPI	TWIHS	HSMCI port/bits	Image Sensor Interface (ISI)	SPI0	SPI1	External Bus Interface (EBI)	SDRAM Interface	DMA Channels	SSC	ETM	Timer Counter Channels	Timer Counter Channels I/O	I2SC	I/O Pins	12-bit ADC Channels	Analog Comparators	DAC Channels
SAMS70Q19	512	256	144	LQFP, LFBGA, UFBGA	HS	3/5	Y	3	3	1/4	12 -bit	Y	Y	Y	Y	24	Y	Y	12	36	2	114	24	Y	2
SAMS70Q20	1024	384																							
SAMS70Q21	2048																								
SAMS70N19	512	256	100	LQFP, TFBGA, VFBGA	HS	3/5	Y	3	3	1/4	12 -bit	Y	N	N	N	24	Y	Y	12	9	1	75	10	Y	2
SAMS70N20	1024	384																							
SAMS70N21	2048																								
SAMS70J19	512	256	64	LQFP, QFN	FS	0/5	SPI only	0	2	N	8-bit	N	N	N	N	24	Y	Y	12	3	0	44	5	Y	1
SAMS70J20	1024	384																							
SAMS70J21	2048																								

Note: HS = High-Speed; FS = Full-Speed.

2. Ordering Information



Note:

1. LQFP package type for Grade 2 variants.

3. Block Diagram

Refer to the table 1. Configuration Summary for detailed configurations of memory size, package and features of the SAM E70/S70/V70/V71 devices.

Figure 3-1. SAM S70 144-pin Block Diagram

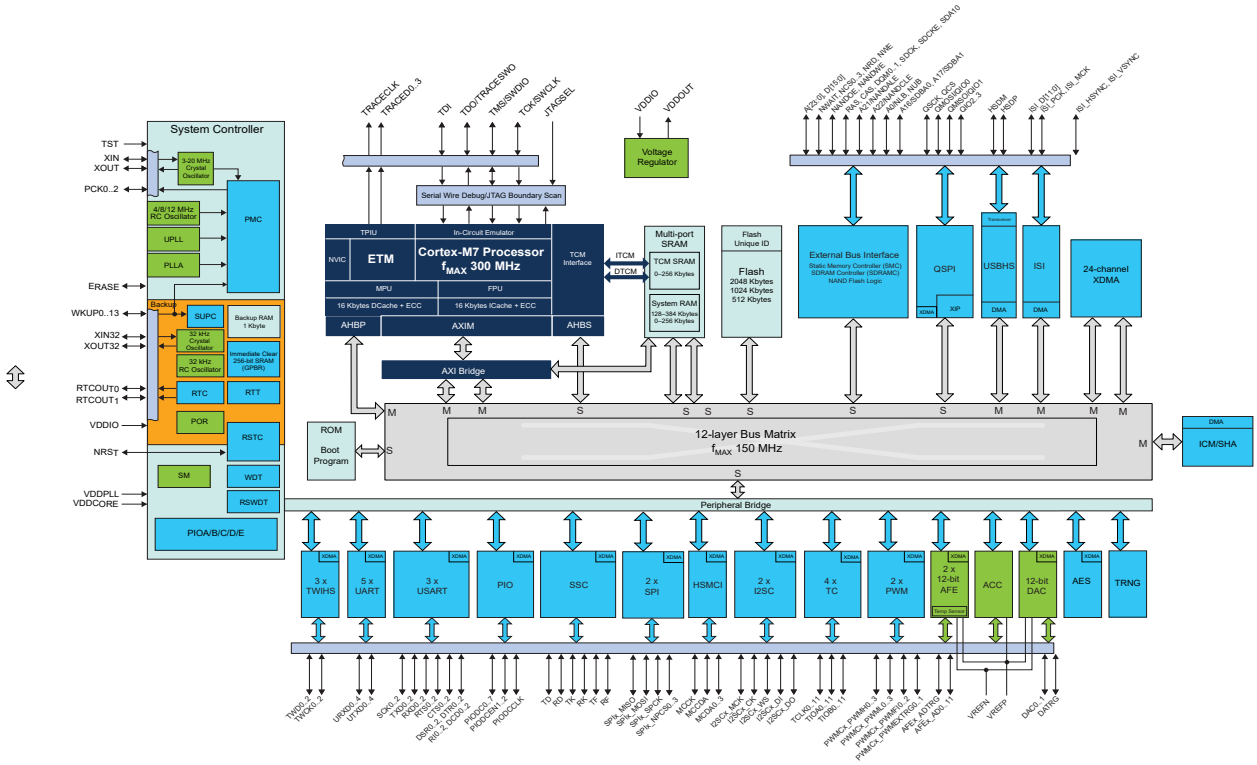


Figure 3-2. SAM E70 144-pin Block Diagram

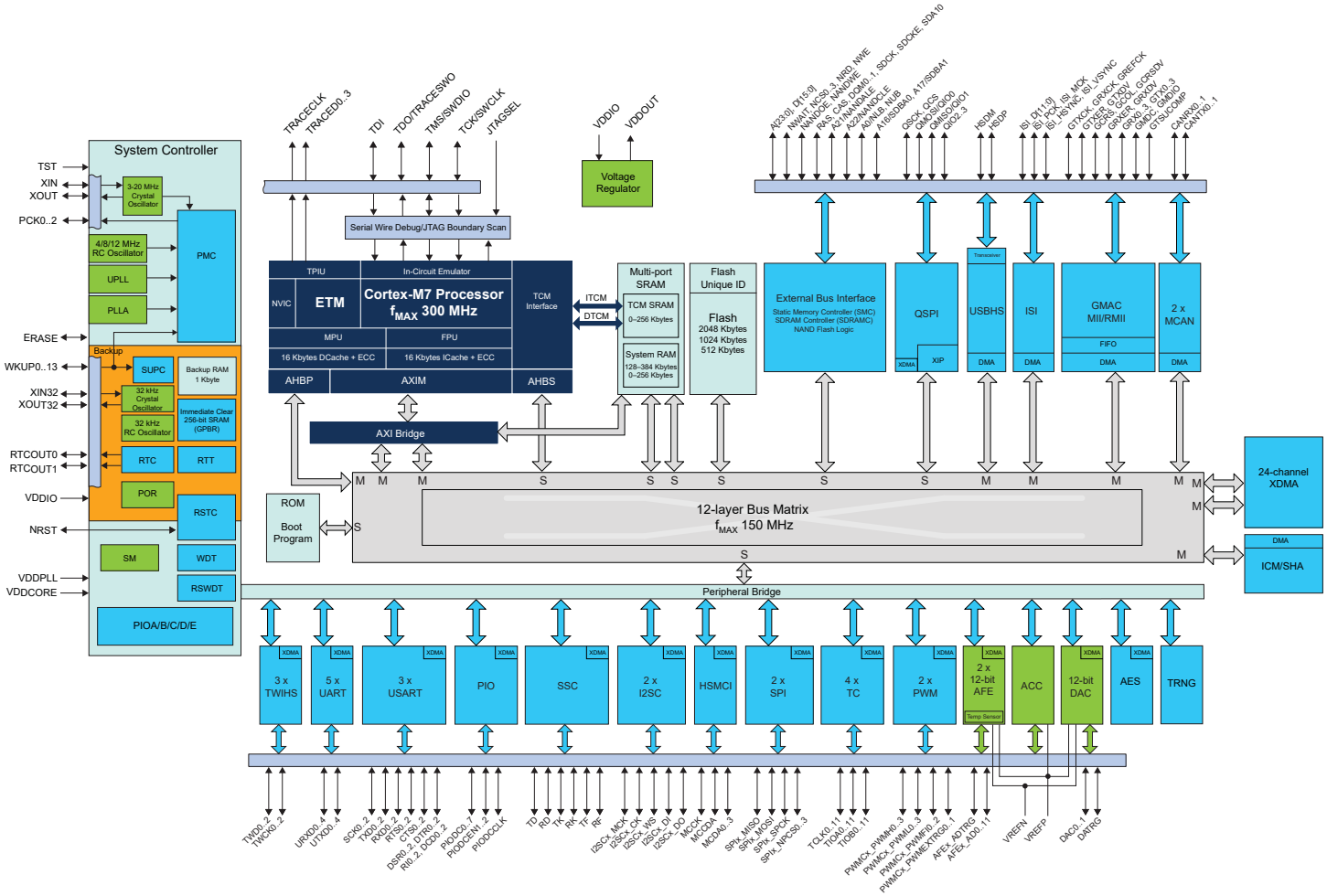


Figure 3-3. SAM V70 144-pin Block Diagram

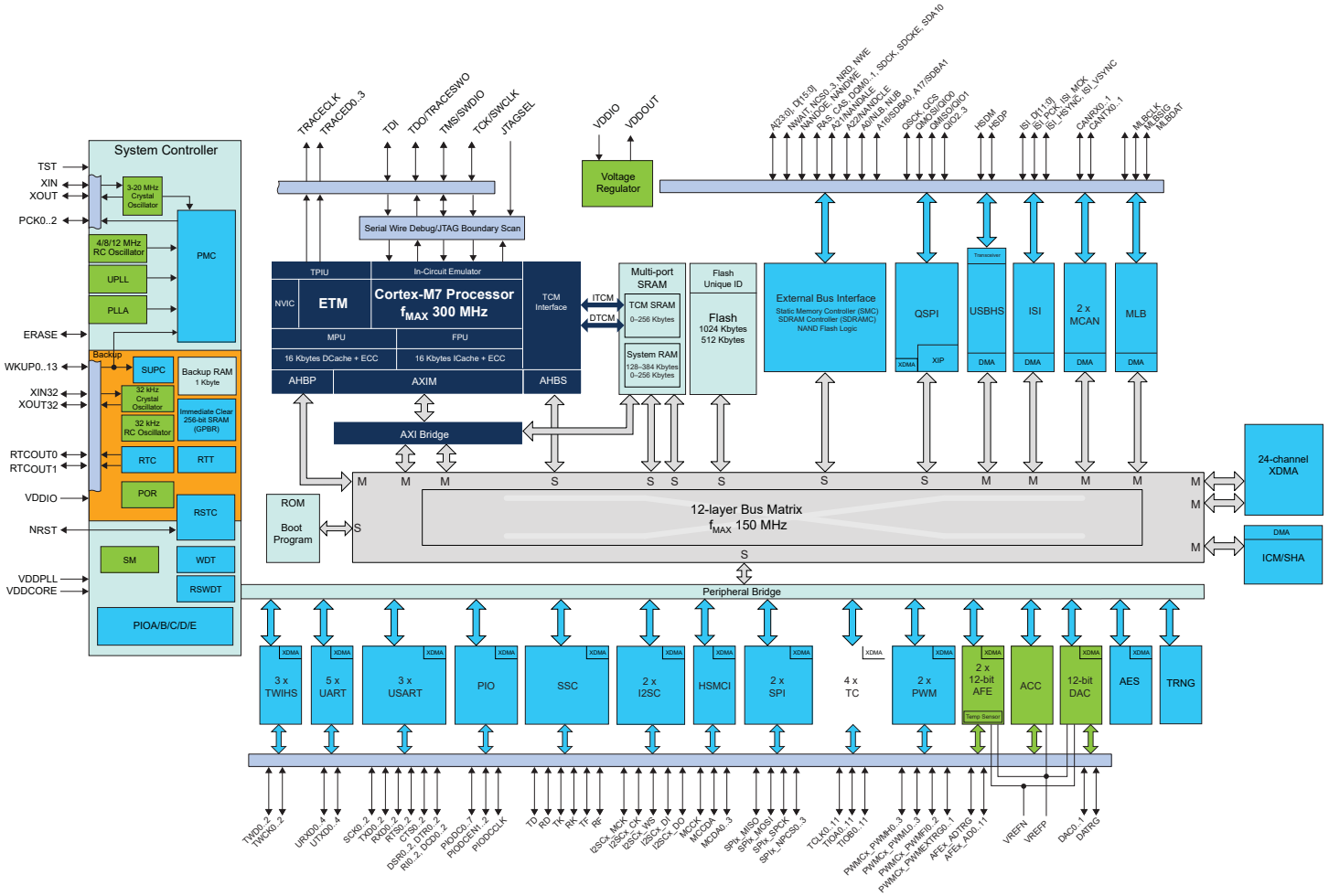
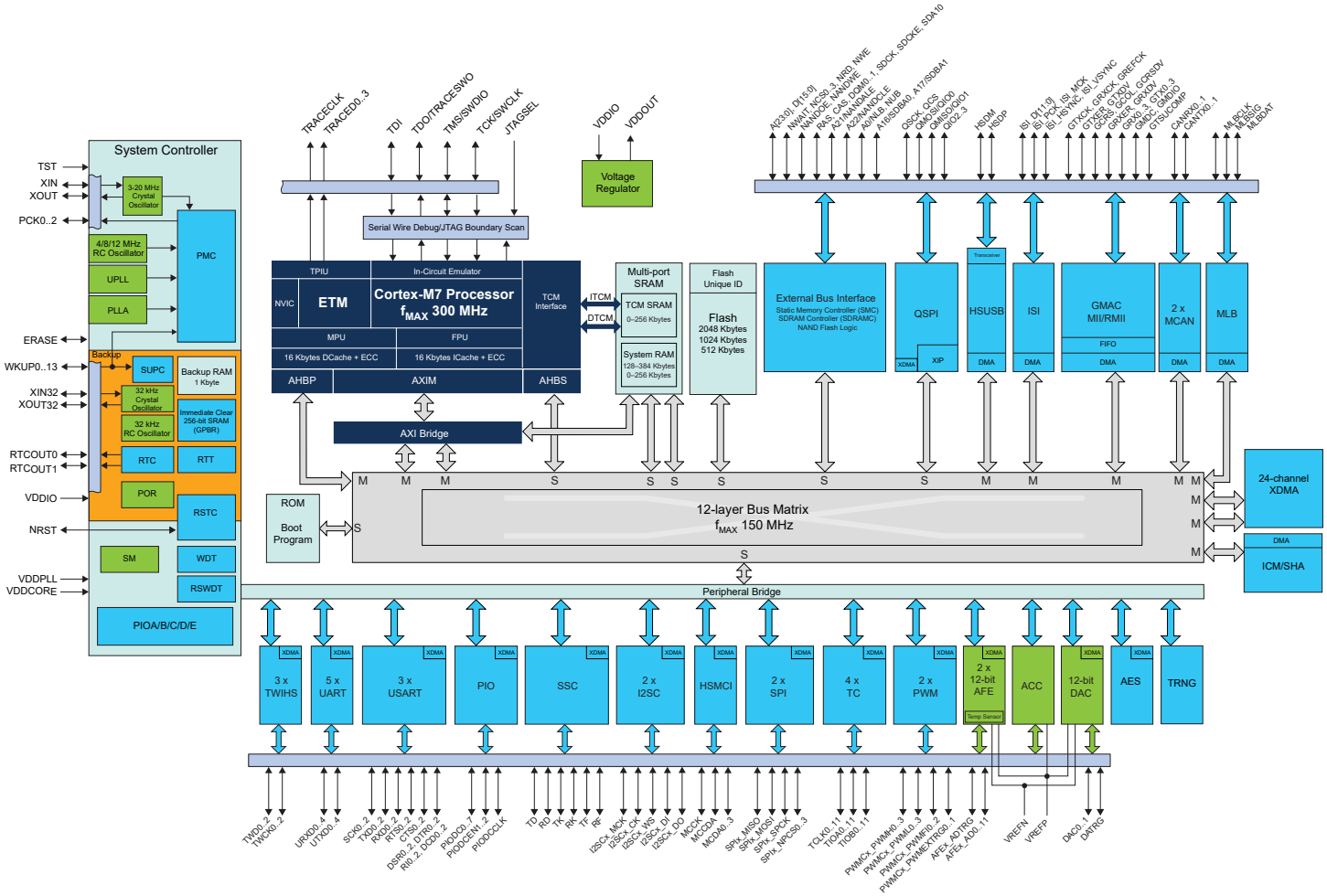


Figure 3-4. SAM V71 144-pin Block Diagram



4. Signal Description

The following table provides details on signal names classified by peripheral.

Table 4-1. Signal Description List

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Power Supplies					
VDDIO	Peripherals I/O Lines Power Supply	Power	–	–	–
VDDIN	Voltage Regulator Input, AFE, DAC and Analog Comparator Power Supply (see **Note**)	Power	–	–	–
VDDOUT	Voltage Regulator Output	Power	–	–	–
VDDPLL	PLLA Power Supply	Power	–	–	–
VDDPLLUSB	USB PLL and Oscillator Power Supply	Power	–	–	–
VDDCORE	Powers the core, the embedded memories and the peripherals	Power	–	–	–
GND, GNDPLL, GNDPLLUSB, GNDANA, GNDUTMI	Ground	Ground	–	–	–
VDDUTMII	USB Transceiver Power Supply	Power	–	–	–
VDDUTMIC	USB Core Power Supply	Power	–	–	–
GNDUTMI	USB Ground	Ground	–	–	–
Clocks, Oscillators and PLLs					
XIN	Main Oscillator Input	Input	–	VDDIO	–
XOUT	Main Oscillator Output	Output	–		–
XIN32	Slow Clock Oscillator Input	Input	–		–
XOUT32	Slow Clock Oscillator Output	Output	–		–

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
PCK0–PCK2	Programmable Clock Output	Output	–		–
Real Time Clock					
RTCOUT0	Programmable RTC Waveform Output	Output	–	VDDIO	–
RTCOUT1	Programmable RTC Waveform Output	Output	–		–
Serial Wire Debug/JTAG Boundary Scan					
SWCLK/TCK	Serial Wire Clock / Test Clock (Boundary scan mode only)	Input	–	VDDIO	–
TDI	Test Data In (Boundary scan mode only)	Input	–		–
TDO/TRACESWO	Test Data Out (Boundary scan mode only)	Output	–		–
SWDIO/TMS	Serial Wire Input/ Output / Test Mode Select (Boundary scan mode only)	I/O / Input	–		–
JTAGSEL	JTAG Selection	Input	High		–
Trace Debug Port					
TRACECLK	Trace Clock	Output	–	VDDIO	PCK3 is used for ETM
TRACED0–TRACED3	Trace Data	Output	–		–
Flash Memory					
ERASE	Flash and NVM Configuration Bits Erase Command	Input	High	VDDIO	–
Reset/Test					
NRST	Synchronous Microcontroller Reset	I/O	Low	VDDIO	–
TST	Test Select	Input	–		–
Universal Asynchronous Receiver Transceiver - UART(x=[0:4])					

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
URXDx	UART Receive Data	Input	–	–	PCK4 can be used to generate the baud rate
UTXDx	UART Transmit Data	Output	–	–	
PIO Controller - PIOA - PIOB - PIOC - PIOD - PIOE					
PA0–PA31	Parallel IO Controller A	I/O	–	VDDIO	–
PB0–PB9, PB12–PB13	Parallel IO Controller B	I/O	–		–
PC0– PC31	Parallel IO Controller C	I/O	–		–
PD0–PD31	Parallel IO Controller D	I/O	–	–	–
PE0–PE5	Parallel IO Controller E	I/O	–	–	–
PIO Controller - Parallel Capture Mode					
PIODC0–PIODC7	Parallel Capture Mode Data	Input	–	VDDIO	–
PIODCCLK	Parallel Capture Mode Clock	Input	–		–
PIODCEN1–PIODCEN2	Parallel Capture Mode Enable	Input	–		–
External Bus Interface					
D[15:0]	Data Bus	I/O	–	–	–
A[23:0]	Address Bus	Output	–	–	–
NWAIT	External Wait Signal	Input	Low	–	–
Static Memory Controller - SMC					
NCS0–NCS3	Chip Select Lines	Output	Low	–	–
NRD	Read Signal	Output	Low	–	–
NWE	Write Enable	Output	Low	–	–
NWR0–NWR1	Write Signal	Output	Low	–	–
NBS0–NBS1	Byte Mask Signal	Output	Low	–	Used also for SDRAMC
NAND Flash Logic					
NANDOE	NAND Flash Output Enable	Output	Low	–	–
NANDWE	NAND Flash Write Enable	Output	Low	–	–
SDR-SDRAM Controller Logic					

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
SDCK	SDRAM Clock	Output	–	–	–
SDCKE	SDRAM Clock Enable	Output	–	–	–
SDCS	SDRAM Controller Chip Select	Output	–	–	–
BA0–BA1	Bank Select	Output	–	–	–
SDWE	SDRAM Write Enable	Output	–	–	–
RAS–CAS	Row and Column Signal	Output	–	–	–
SDA10	SDRAM Address 10 Line	Output	–	–	–
High Speed Multimedia Card Interface - HSMCI					
MCCK	Multimedia Card Clock	I/O	–	–	–
MCCDA	Multimedia Card Slot A Command	I/O	–	–	–
MCDA0–MCDA3	Multimedia Card Slot A Data	I/O	–	–	–
Universal Synchronous Asynchronous Receiver Transmitter USART(x=[0:2])					
SCKx	USARTx Serial Clock	I/O	–	–	PCK4 can be used to generate the baud rate
TXDx	USARTx Transmit Data	I/O	–	–	
RXDx	USARTx Receive Data	Input	–	–	
RTSx	USARTx Request To Send	Output	–	–	
CTSx	USARTx Clear To Send	Input	–	–	
DTRx	USARTx Data Terminal Ready	Output	–	–	
DSRx	USARTx Data Set Ready	Input	–	–	
DCDx	USARTx Data Carrier Detect	Input	–	–	
RIx	USARTx Ring Indicator	Input	–	–	
LONCOL1	LON Collision Detection	Input	–	–	
Synchronous Serial Controller - SSC					