Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

ATtiny807/1607

AVR® Microcontroller with Core Independent Peripherals and picoPower® Technology

Introduction

The ATtiny807/1607 microcontrollers are using the high-performance, low-power AVR® RISC architecture, and are capable of running at up to 20 MHz, with up to 8/16 KB Flash, 512/1024 bytes of SRAM, and 128/256 bytes of EEPROM in a 24-pin package. The series uses the latest technologies with a flexible and low-power architecture including Event System and SleepWalking, accurate analog features and advanced peripherals.

Features

- CPU:
  - AVR® 8-bit CPU
  - Running at up to 20 MHz
  - Single cycle I/O access
  - Two-level interrupt controller
  - Two-cycle hardware multiplier
- Memories:
  - 8/16 KB In-system self-programmable Flash memory
  - 128/256B EEPROM
  - 512/1024B SRAM
- System:
  - Power-on Reset (POR)
  - Brown-out Detection (BOD)
  - Internal and external clock options with:
    - 16/20 MHz low-power internal RC oscillator
    - 32.768 kHz Ultra Low Power (ULP) internal RC oscillator with ±10% accuracy, ±2% calibration step size
    - External clock input
  - Single pin Unified Program Debug Interface (UPDI)
  - Three sleep modes:
    - Idle with all peripherals running and mode for immediate wake-up time
    - Standby Sleep mode:
      - Configurable operation of selected peripherals
      - SleepWalking peripherals
    - Power-Down Sleep mode with limited wake-up functionality

- Peripherals:
  - 3-channel Event System
  - One 16-bit Timer/Counter with Dedicated Period register and Three Compare Channels (TCA)
  - One 16-bit Timer/Counter type B with Input Capture (TCB)
  - One 16-bit Real Time Counter (RTC) running from internal RC oscillator
  - One USART with fractional baud rate generator, auto-baud, Start-Of-Frame (SOF) detection, and Local Interconnect Network (LIN) support
  - Master/slave Serial Peripheral Interface (SPI)
  - Master/slave TWI with dual address match
    - Standard mode (Sm, 100 kHz)
    - Fast mode (Fm, 400 kHz)
    - Fast mode Plus (Fm+, 1 MHz)
  - Configurable Custom Logic (CCL) with two Programmable Lookup Tables (LUT)
  - One Analog Comparator (AC) with 150 ns propagation delay
  - 10-bit 150 ksps Analog-to-Digital Converter (ADC)
  - Five selectable internal voltage references: 0.55V, 1.1V, 1.5V, 2.5V and 4.3V
  - Automated CRC memory scan
  - Programmable Watchdog Timer (WDT) with separate on-chip oscillator
  - External interrupt on all general purpose pins
- I/O and Packages:
  - 24-pin
    - 22 Programmable I/O lines
    - VQFN 4x4
- Temperature Ranges:
  - -40°C to 105°C operating range
  - -40°C to 125°C temperature graded device options available
- Speed Grades:
  - T_A max. 105°C
    - 0-5 MHz @ 1.8V – 5.5V
    - 0-10 MHz @ 2.7V – 5.5V
    - 0-20 MHz @ 4.5V – 5.5V

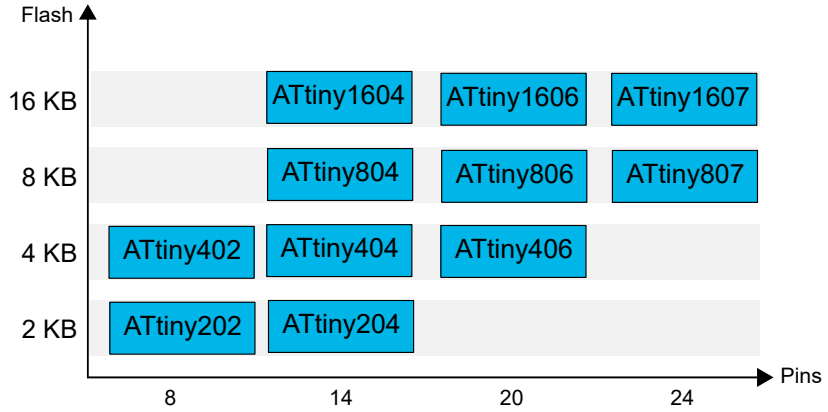
Table of Contents

1. tinyAVR® 0-Series Overview

The figure below shows the tinyAVR® 0-series, laying out pin count variants and memory sizes:

- Vertical migration is possible without code modification, as these devices are fully pin- and feature compatible.
- Horizontal migration to the left reduces the pin count and therefore the available features.

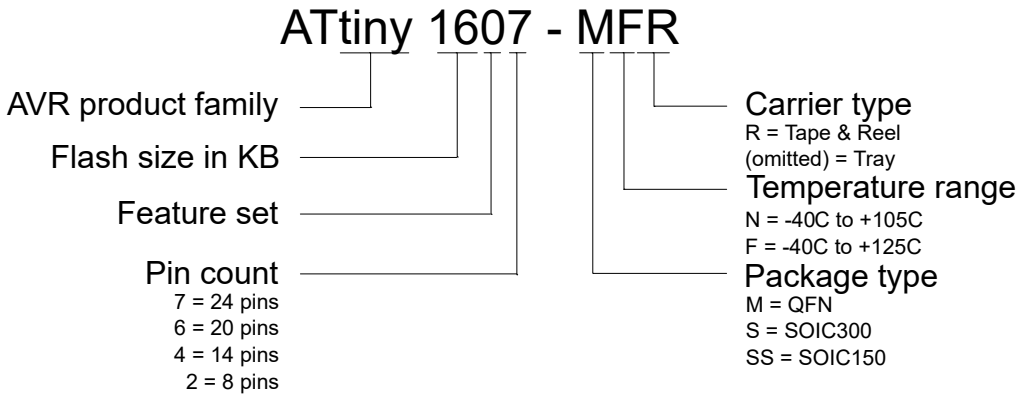
Figure 1-1. Device Family Overview



Devices with different Flash memory size typically also have different SRAM and EEPROM.

The name of a device of the ATtiny family contains information as depicted below (not all options are available):

Figure 1-2. Device Designations



1.1 Configuration Summary

1.1.1 Peripheral Summary

Table 1-1. Peripheral Summary

	ATtiny807	ATtiny1607
Pins	24	24
SRAM	512B	1024B
Flash	8 KB	16 KB
EEPROM	128B	256B
Max. frequency (MHz)	20	20
16-bit Timer/Counter type A (TCA)	1	1
16-bit Timer/Counter type B (TCB)	1	1
12-bit Timer/Counter type D (TCD)	NO	NO
Real Time Counter (RTC)	1	1
USART	1	1
SPI	1	1
TWI (I^2C)	1	1
ADC/Channels	1/12	1/12
DAC	No	No
AC pins	1/2p, 2n, 1 out Slow mode only	1/2p, 2n, 1 out Slow mode only
Peripheral Touch Controller (PTC)	No	No
Custom Logic	1	1

	ATtiny807	ATtiny1607
Window Watchdog	1	1
Event System channels	3	3
General purpose I/O	22	22
External interrupts	22	22
CRCSCAN	YES	YES

2. Ordering Information

2.1 ATtiny807

Table 2-1. ATtiny807 Ordering Codes

Ordering Code[1]	Flash	Package Type (GPC)	Leads	Power Supply	Operational Range	Carrier Type
ATtiny807-MNR	8 KB	VQFN 4x4 (ZHA)	24	1.8V - 5.5V	Industrial (-40°C +105°C)	Tape & Reel
ATtiny807-MFR	8 KB	VQFN 4x4 (ZHA)	24	1.8V - 5.5V	Industrial (-40°C +125°C)	Tape & Reel

Note:

1. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

2.2 ATtiny1607

Table 2-2. ATtiny1607 Ordering Codes

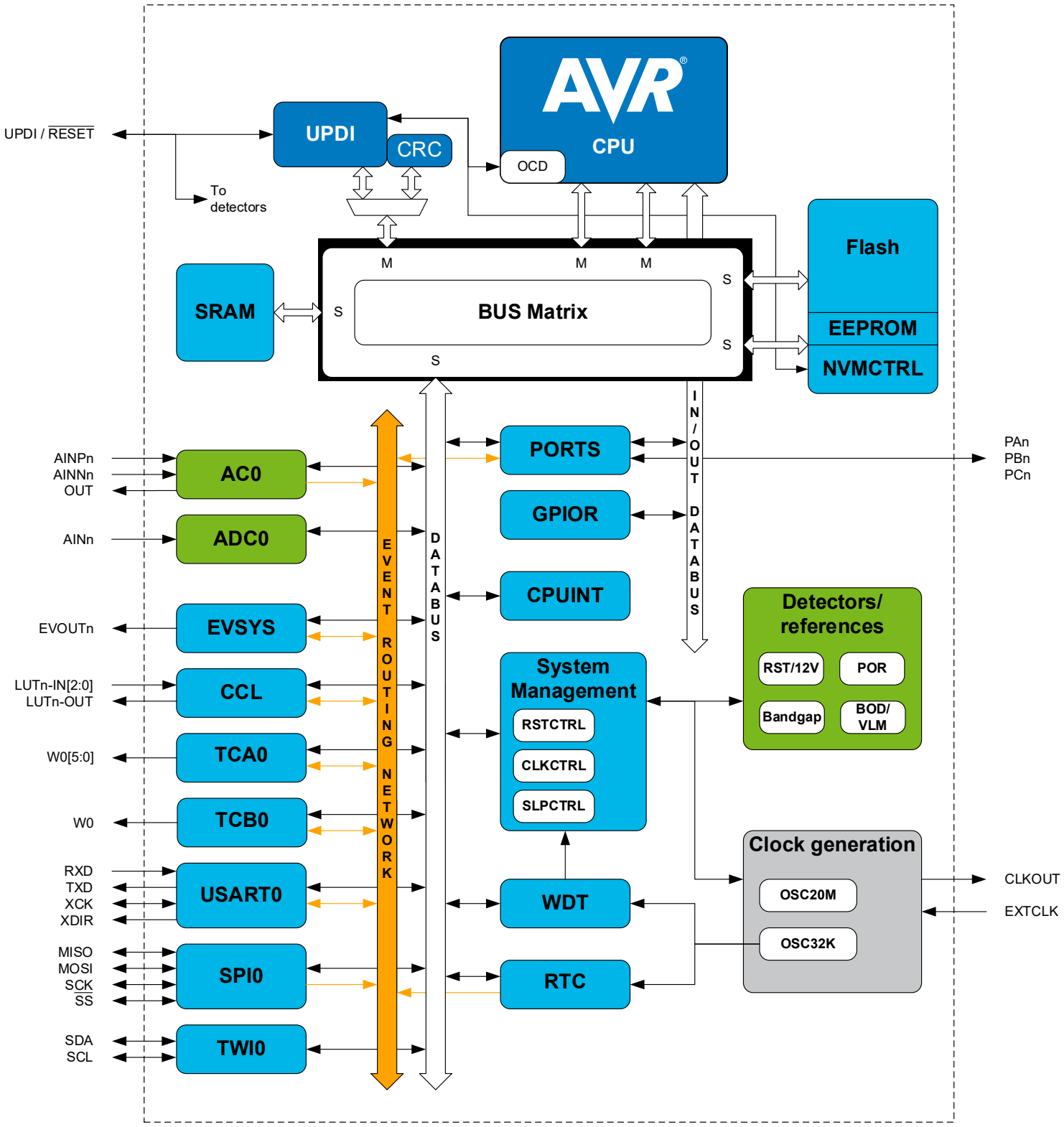
Ordering Code[1]	Flash	Package Type (GPC)	Leads	Power Supply	Operational Range	Carrier Type
ATtiny1607-MNR	16 KB	VQFN 4x4 (ZHA)	24	1.8V - 5.5V	Industrial (-40°C to +105°C)	Tape & Reel
ATtiny1607-MFR	16 KB	VQFN 4x4 (ZHA)	24	1.8V - 5.5V	Industrial (-40°C to +125°C)	Tape & Reel

Note:

1. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

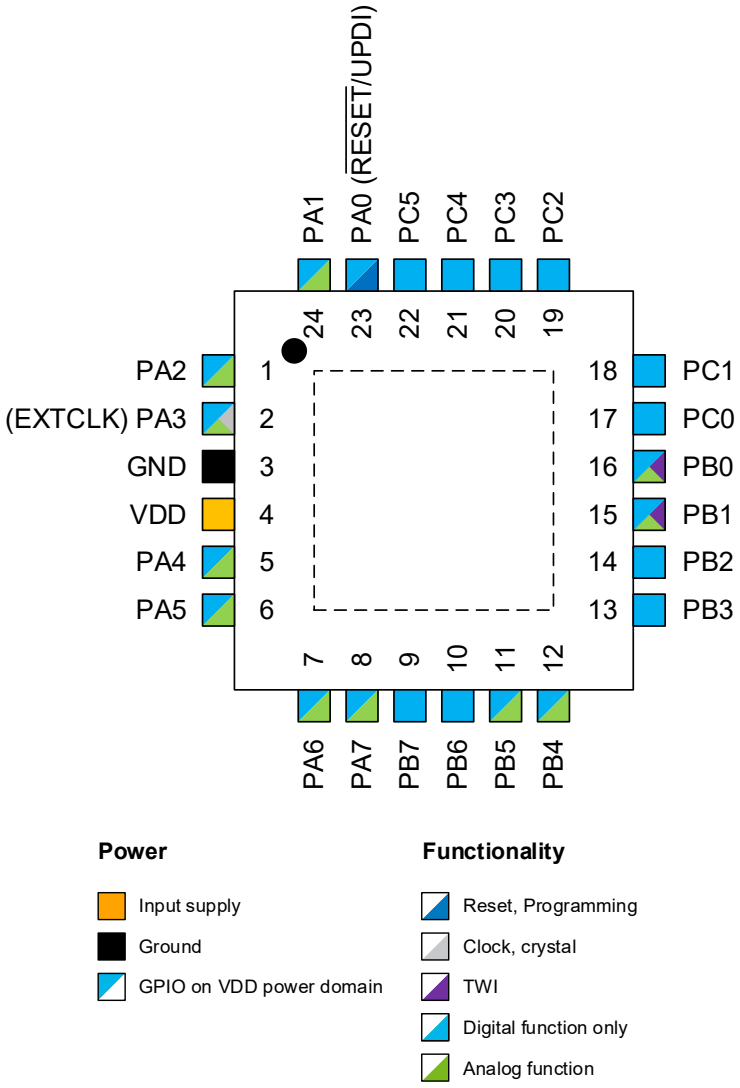
3. Block Diagram

Figure 3-1. Block Diagram



4. Pinout

4.1 24-pin QFN4x4



5. I/O Multiplexing and Considerations

5.1 Multiplexed Signals

Table 5-1. PORT Function Multiplexing

QFN 24-pin	Pin Name(1,2)	Special	EXTINTx	ADC0	AC0	USART0	SPI0	TWI0	TCA0	TCB0	Other	CCL	Scan
23	PA0	$\overline{\text{RESET}}$, UPDI	S	AIN0								LUT0-IN0	$\overline{\text{RESET}}$
24	PA1		S	AIN1		TXD	MOSI				BREAK	LUT0-IN1	
1	PA2		A	AIN2		RXD	MISO				EVOUT	LUT0-IN2	ENABLE
2	PA3	CLKI	S	AIN3		XCK	SCK		W03				CLOCK
3	GND												
4	VCC												
5	PA4		S	AIN4		XDIR	$\overline{\text{SS}}$		W04			LUT0-OUT	SO2
6	PA5		S	AIN5	OUT				W05	W00			SO3
7	PA6		A	AIN6	AINN0								SI0/SER
8	PA7		S	AIN7	AINP0							LUT1-OUT	SO0/SER
9	PB7		S										
10	PB6		A										
11	PB5		S	AIN8	AINP1				W02		CLKOUT		
12	PB4		S	AIN9	AINN1				W01			LUT0-OUT	
13	PB3		S			RXD			W00				SO1/SER
14	PB2		A			TXD			W02		EVOUT		SI1/SER
15	PB1	I2C	S	AIN10		XCK		SDA	W01				SI2
16	PB0	I2C	S	AIN11		XDIR		SCL	W00				SI3
17	PC0		S				SCK			W00			
18	PC1		S				MISO					LUT1-OUT	
19	PC2		A				MOSI				EVOUT		
20	PC3		S				$\overline{\text{SS}}$		W03			LUT1-IN0	
21	PC4		S						W04			LUT1-IN1	
22	PC5		S						W05			LUT1-IN2	

Note:

1. Pins names are of type P*xn*, with *x* being the PORT instance (A, B) and *n* the pin number. Notation for signals is PORT*x*_PIN*n*. All pins can be used as event input.
2. All pins can be used for external interrupt, where pins P*x*2 and P*x*6 of each port have full asynchronous detection.

Tip: Signals on alternative pin locations are in `typewriter` font.

5.2 Reset Pin Selection

The reset pin needs to operate as both GPIO, Reset, programming and enable of programming interface (12V)

RSTPINCFG[1:0]	Functionality	Description
00	GPIO	Reset pin used for GPIO Output functionality no sooner than 10 ms External Reset functionality is not available
01	RESET	Reset pin operating as external Reset with pull-up enabled
10	PDI	Reset pin used for programming interface External Reset functionality is not available

Note:

1. Refer to fuses SYSCFG0 in chapter *Memories* for more information
2. Selected reset pin will have filter
3. Option 2'b10 will be setting after production. Before fuses are read option 2'b00 is assumed
4. A pin cannot be set as output before at least 10ms after Reset is released internally

6. Memories

6.1 Overview

The main memories are SRAM data memory, EEPROM data memory, and Flash program memory. In addition, the peripheral registers are located in the I/O memory space.

Table 6-1. Physical Properties of EEPROM

Property	ATtiny1607	ATtiny807
Size	256B	128B
Page size	32B	32B
Number of pages	8	4
Start address	0x1400	0x1400
AUX rows	3	3

Table 6-2. Physical Properties of SRAM

Property	ATtiny1607	ATtiny807
Size	1 KB	512B
Start address	0x3C00	0x3E00

Table 6-3. Physical Properties of Flash Memory

Property	ATtiny1607	ATtiny807
Size	16 KB	8 KB
Page size	64B	64B
Number of pages	256	128
Start address	0x8000	0x8000
AUX rows	1	1

The SRAM is mirrored within the address space 0x2000 - 0x3FFF

Self programming between sections in memory is only possible in the following combinations:

- Boot
  - to application code
  - to application data
- Application code
  - to application data

It is not possible for the different sections to write to themselves. Application data cannot write to Flash or EEPROM.

CPU execution will be halted while doing self programming

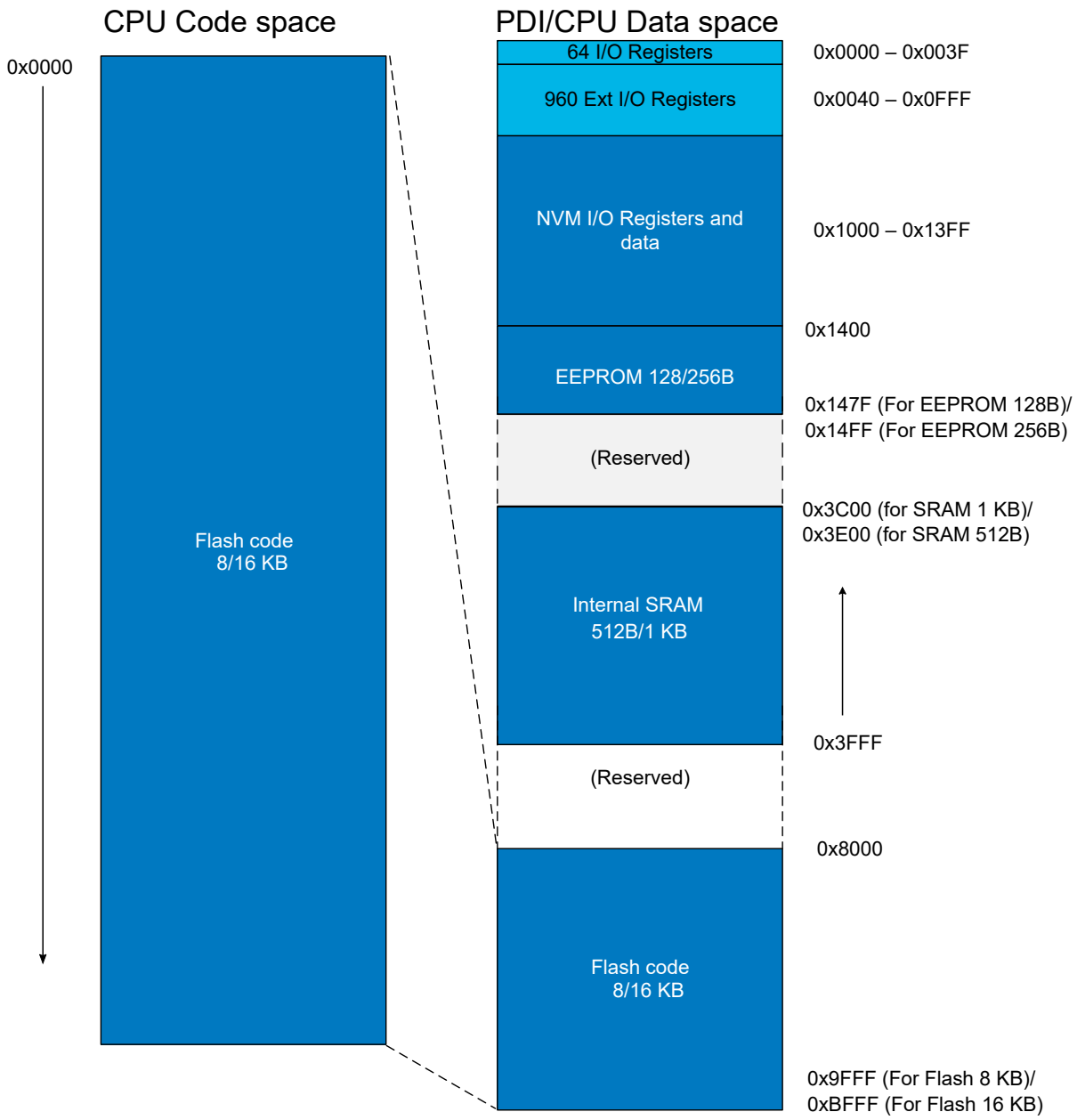
EEPROM can be written from Boot and application code

Related Links

6.8 I/O Memory

6.2 Memory Map

Figure 6-1. Memory Map: Flash 8/16KB, Internal SRAM 512B/1KB, EEPROM 128/256B



6.3 In-System Reprogrammable Flash Program Memory

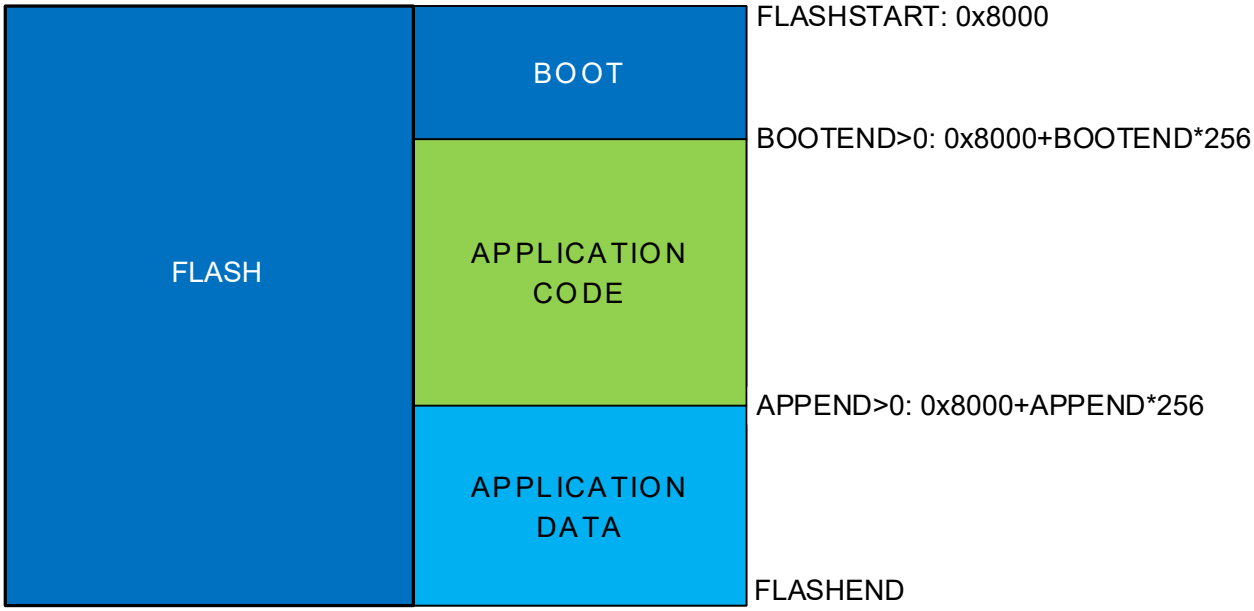
The ATtiny807/1607 contains 16/8 KB on-chip in-system reprogrammable Flash memory for program storage. Since all AVR instructions are 16 or 32 bits wide, the Flash is organized as 4K x 16. For write protection, the Flash program memory space can be divided into three sections (see the illustration below): Bootloader section, application code section, and application data section, with restricted access rights among them.

The Program Counter (PC) is 12/13-bits wide to address the whole program memory. The procedure for writing Flash memory is described in detail in the documentation of the Nonvolatile Memory Controller (NVMCTRL) peripheral.

The entire Flash memory is mapped in the memory space and is accessible with normal LD/ST instructions as well as the LPM instruction. For LD/ST instructions, the Flash is mapped from address 0x8000. For the LPM instruction, the Flash start address is 0x0000.

The ATtiny807/1607 also has a CRC peripheral that is a master on the bus.

Figure 6-2. Flash and the Three Sections



Related Links

9. NVMCTRL - Nonvolatile Memory Controller

6.4 SRAM Data Memory

The 512B/1 KB SRAM is used for data storage and stack.

Related Links

8. AVR CPU

8.5.4 Stack and Stack Pointer

6.5 EEPROM Data Memory

The ATtiny807/1607 has 128/256 bytes of EEPROM data memory, see Memory Map section. The EEPROM memory supports single byte read and write. The EEPROM is controlled by the Nonvolatile Memory Controller (NVMCTRL).

Related Links

9. NVMCTRL - Nonvolatile Memory Controller

6.2 Memory Map

6.6 User Row

In addition to the EEPROM, the ATtiny807/1607 has one extra page of EEPROM memory that can be used for firmware settings, the User Row (USERROW). This memory supports single byte read and write as the normal EEPROM. The CPU can write and read this memory as normal EEPROM and the UPDI can write and read it as a normal EEPROM memory if the part is unlocked. The User Row can be written by the UPDI when the part is locked. USERROW is not affected by a chip erase.

Related Links

6.2 Memory Map

9. NVMCTRL - Nonvolatile Memory Controller

30. UPDI - Unified Program and Debug Interface

6.7 Signature Bytes

All ATtiny microcontrollers have a 3-byte signature code that identifies the device. This code can be read in both Serial and Parallel mode. The three bytes reside in a separate address space. For the device, the signature bytes are given in the following table.

Note: When the device is locked, only the System Information Block (SIB) can be obtained.

Table 6-4. Device ID

Device Name	Signature Bytes Address		
	0x00	0x01	0x02
ATtiny807	0x1E	0x93	0x23
ATtiny1607	0x1E	0x94	0x23

Related Links

30.3.6 System Information Block

6.8 I/O Memory

All ATtiny807/1607 I/Os and peripherals are located in the I/O memory space. The I/O address range from 0x00 to 0x3F can be accessed in a single cycle using `IN` and `OUT` instructions. The extended I/O memory space from 0x0040 - 0x0FFF can be accessed by the `LD`/`LDS`/`LDD` and `ST`/`STS`/`STD` instructions, transferring data between the 32 general purpose working registers and the I/O memory space.

I/O registers within the address range 0x00 - 0x1F are directly bit accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions. Refer to the Instruction Set section for more details.

For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.

Some of the interrupt flags are cleared by writing a '1' to them. On ATtiny807/1607 devices, the CBI and SBI instructions will only operate on the specified bit and can be used on registers containing such interrupt flags. The CBI and SBI instructions work with registers 0x00 - 0x1F only.

General Purpose I/O Registers

The ATtiny807/1607 devices provide four general purpose I/O registers. These registers can be used for storing any information, and they are particularly useful for storing global variables and interrupt flags. general purpose I/O registers, which reside in the address range 0x1C - 0x1F, are directly bit accessible using the SBI, CBI, SBIS, and SBIC instructions.

Related Links

6.2 Memory Map
7.1 Peripheral Module Address Map
35. Instruction Set Summary

6.8.1 Register Summary - GPIOR

Offset	Name	Bit Pos.								
0x00	GPIOR0	7:0	GPIOR[7:0]							
0x01	GPIOR1	7:0	GPIOR[7:0]							
0x02	GPIOR2	7:0	GPIOR[7:0]							
0x03	GPIOR3	7:0	GPIOR[7:0]							

6.8.2 Register Description - GPIOR

6.8.2.1 General Purpose I/O Register n

Name: GPIOR
Offset: 0x00 + n*0x01 [n=0..3]
Reset: 0x00
Property: -

These are general purpose registers that can be used to store data, such as global variables and flags, in the bit accessible I/O memory space.

Bit	7	6	5	4	3	2	1	0
	GPIOR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – GPIOR[7:0] GPIO Register byte

6.9 Memory Section Access from CPU and UPDI on Locked Device

The device can be locked so that the memories cannot be read using the UPDI. The locking protects both the Flash (all BOOT, APPCODE, and APPDATA sections), SRAM, and the EEPROM including the FUSE data. This prevents successful reading of application data or code using the debugger interface. Regular memory access from within the application still is enabled.

The device is locked by writing any non-valid value to the LOCKBIT bit field in FUSE.LOCKBIT.

Table 6-5. Memory Access in Unlocked Mode (FUSE.LOCKBIT Valid)(1)

Memory Section	CPU Access		UPDI Access	
	Read	Write	Read	Write
SRAM	Yes	Yes	Yes	Yes
Registers	Yes	Yes	Yes	Yes
Flash	Yes	Yes	Yes	Yes
EEPROM	Yes	Yes	Yes	Yes
USERROW	Yes	Yes	Yes	Yes
SIGROW	Yes	No	Yes	No
Other Fuses	Yes	No	Yes	Yes

Table 6-6. Memory Access in Locked Mode (FUSE.LOCKBIT Invalid)(1)

Memory Section	CPU Access		UPDI Access	
	Read	Write	Read	Write
SRAM	Yes	Yes	No	No
Registers	Yes	Yes	No	No
Flash	Yes	Yes	No	No

Memory Section	CPU Access		UPDI Access	
	Read	Write	Read	Write
EEPROM	Yes	No	No	No
USERROW	Yes	Yes	No	Yes(2)
SIGROW	Yes	No	No	No
Other Fuses	Yes	No	No	No

Note:

1. Read operations marked No in the tables may appear to be successful, but the data is corrupt. Hence, any attempt of code validation through the UPDI will fail on these memory sections.
2. In Locked mode, the USERROW can be written blindly using the fuse Write command, but the current USERROW values cannot be read out.

Important: The only way to unlock a device is a CHIPERASE, which will erase all device memories to factory default so that no application data is retained.

6.10 Configuration and User Fuses (FUSE)

Fuses are part of the nonvolatile memory and hold factory calibration data and device configuration. The fuses are available from device power-up. The fuses can be read by the CPU or the UPDI, but can only be programmed or cleared by the UPDI. The configuration and calibration values stored in the fuses are written to their respective target registers at the end of the start-up sequence.

The content of the Signature Row fuses (SIGROW) is pre-programmed and cannot be altered. SIGROW holds information such as device ID, serial number, and calibration values.

The fuses for peripheral configuration (FUSE) are pre-programmed but can be altered by the user. Altered values in the configuration fuse will be effective only after a Reset.
Note: When writing the fuses write all reserved bits to '1'.

This device provides a User Row fuse area (USERROW) that can hold application data. The USERROW can be programmed on a locked device by the UPDI. This can be used for final configuration without having programming or debugging capabilities enabled.

Related Links

6.10.2 Signature Row Description
6.10.4 Fuse Description

6.10.1 Signature Row Summary (SIGROW)

Offset	Name	Bit Pos.									
0x00	DEVICEID0	7:0	DEVICEID[7:0]								
0x01	DEVICEID1	7:0	DEVICEID[7:0]								
0x02	DEVICEID2	7:0	DEVICEID[7:0]								
0x03	SERNUM0	7:0	SERNUM[7:0]								
0x04	SERNUM1	7:0	SERNUM[7:0]								
0x05	SERNUM2	7:0	SERNUM[7:0]								
0x06	SERNUM3	7:0	SERNUM[7:0]								
0x07	SERNUM4	7:0	SERNUM[7:0]								
0x08	SERNUM5	7:0	SERNUM[7:0]								
0x09	SERNUM6	7:0	SERNUM[7:0]								
0x0A	SERNUM7	7:0	SERNUM[7:0]								
0x0B	SERNUM8	7:0	SERNUM[7:0]								
0x0C	SERNUM9	7:0	SERNUM[7:0]								
0x0D ... 0x1F	Reserved										
0x20	TEMPSENSE0	7:0	TEMPSENSE[7:0]								
0x21	TEMPSENSE1	7:0	TEMPSENSE[7:0]								
0x22	OSC16ERR3V	7:0	OSC16ERR3V[7:0]								
0x23	OSC16ERR5V	7:0	OSC16ERR5V[7:0]								
0x24	OSC20ERR3V	7:0	OSC20ERR3V[7:0]								
0x25	OSC20ERR5V	7:0	OSC20ERR5V[7:0]								

6.10.2 Signature Row Description