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8-bit AVR Microcontrollers

ATtiny1614 / ATtiny1616 / ATtiny1617

Introduction

The ATtiny1614/1616/1617 is a member of the tinyAVR 1-series of microcontrollers, using the 8-bit AVR® processor with hardware multiplier, running at up to 20MHz and with 16KB Flash, 2KB of SRAM and 256B of EEPROM in a 14-, 20- and 24-pin package. The tinyAVR 1-series uses the latest technologies with a flexible and low power architecture including Event System and SleepWalking, accurate analog features and advanced peripherals. Capacitive touch interfaces with proximity sensing and driven shield are supported with the integrated QTouch® peripheral touch controller.

Features

- CPU
  - AVR® 8-bit CPU
  - Running at up to 20MHz
  - Single cycle I/O access
  - Two-level interrupt controller
  - Two-cycle hardware multiplier
- Memories
  - 16KB In-system self-programmable Flash memory
  - 256B EEPROM
  - 2KB SRAM
- System
  - Power-on Reset (POR)
  - Brown-out Detection (BOD)
  - Internal and external clock options:
    - 16/20MHz low power RC oscillator
    - 32.768kHz Ultra Low Power (ULP) internal RC oscillator with ±10% accuracy, ±2% calibration step size
    - 32.768kHz external crystal oscillator
    - External clock input
  - Single pin programming and debugging interface (UPDI)
  - Three sleep modes:
    - Idle with all peripherals running for immediate wake up
    - Standby
      - Configurable operation of selected peripherals
      - SleepWalking peripherals
    - Power Down with limited wake-up functionality

- Peripherals
  - One 16-bit Timer/Counter type A with dedicated period register, 3 compare channels (TCA)
  - Two 16-bit Timer/Counter type B with input capture (TCB)
  - One 12-bit Timer/Counter type D optimized for control applications (TCD)
  - 16-bit Real Time Counter (RTC) running from external crystal or internal RC oscillator
  - One USART with fractional baud rate generator, autobaud, and start-of-frame detection
  - Master/slave Serial Peripheral Interface (SPI)
  - Master/slave I^2C with dual address match
    - Standard mode (Sm, 100kHz)
    - Fast mode (Fm, 400kHz)
    - Fast mode plus (Fm+, 1MHz)
  - Configurable Custom Logic (CCL) with two programmable Lookup Tables (LUT)
  - Three Analog Comparators (AC) with low propagation delay
  - Two 10-bit 115ksps Analog to Digital Converters (ADC)
  - Three 8-bit Digital to Analog Converters (DAC) with one external channel
  - Five selectable internal voltage references: 0.55V, 1.1V, 1.5V, 2.5V and 4.3V
  - Automated CRC memory scan
  - Window Watchdog Timer (WDT) with separate on-chip oscillator
  - Peripheral Touch Controller (PTC)
    - Capacitive touch buttons, sliders and wheels
    - Wake-up on touch
    - Driven shield for improved moisture and noise handling performance
    - 14 self-capacitance and 9 mutual-capacitance channels
  - External interrupt on all general purpose pins
- I/O and Packages:
  - 12 to 22 programmable I/O lines
  - 14-pin SOIC150
  - 20-pin QFN 3x3 and SOIC300
  - 24-pin QFN 4x4
- Temperature Ranges:
  - -40°C to 105°C
  - -40°C to 125°C Temperature Device Options available
- Speed Grades:
  - 0-5MHz @ 1.8V – 5.5V
  - 0-10MHz @ 2.7V – 5.5V
  - 0-20MHz @ 4.5V – 5.5V

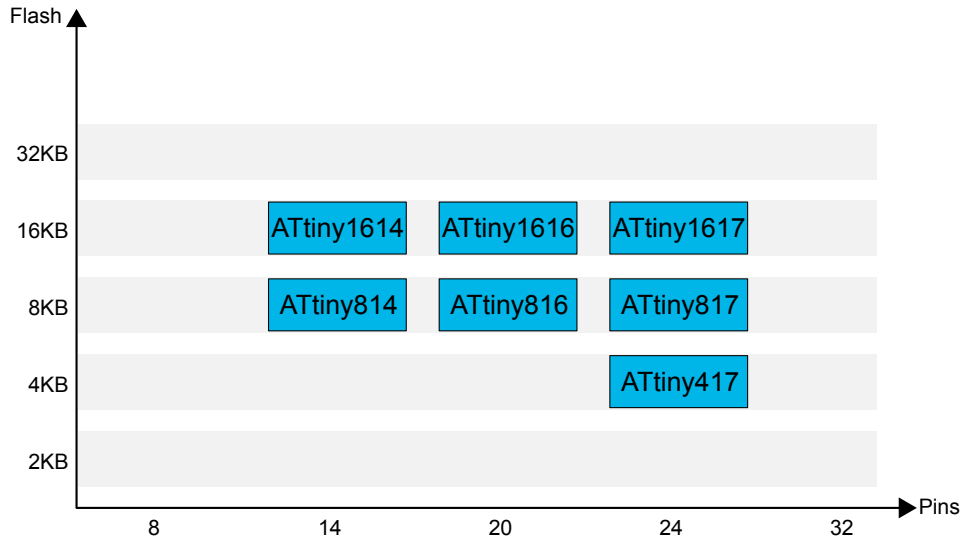
Table of Contents

1. tinyAVR 1-Series Overview

Figure 1-1 shows the tinyAVR™ 1-series, laying out pin count variants and memory sizes:

- Vertical migration can be done upwards without code modification, since these devices are pin compatible and provide the same or even more features. Downward migration may require code modification due to fewer available instances of some peripherals.
- Horizontal migration to the left reduces the pin count and therefore also the available features.

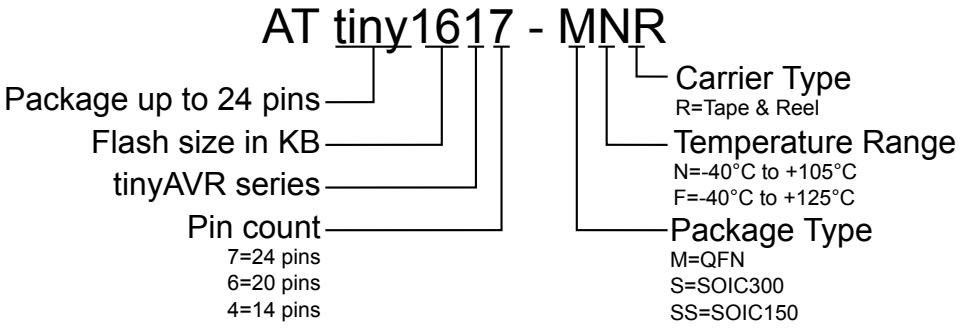
Figure 1-1. tinyAVR 1-Series Overview



Devices with different Flash memory size typically also have different SRAM and EEPROM.

The name of a device of the series contains information as depicted below:

Figure 1-2. Device Designations



1.1 Configuration Summary

1.1.1 Peripheral Summary

Table 1-1. Peripheral Summary

	ATtiny1614	ATtiny1616	ATtiny1617
Pins	14	20	24
SRAM	2KB	2KB	2KB
Flash	16KB	16KB	16KB
EEPROM	256B	256B	256B
Max. frequency (MHz)	20	20	20
16-bit Timer/Counter type A (TCA)	1	1	1
16-bit Timer/Counter type B (TCB)	2	2	2
I	1	1	1
Real Time Counter (RTC)	1	1	1
USART	1	1	1
SPI	1	1	1
TWI (I^2C)	1	1	1
ADC	2	2	2
ADC channels	10+4	12+8	12+12
DAC	3	3	3
AC	3	3	3
Peripheral Touch Controller (PTC)(1)	1	1	1
PTC number of self-capacitance channels(1)	6XY, 1DS	12XY, 2DS	14XY, 2DS
PTC number of mutual-capacitance channels(1)	9	9	9
Custom Logic/Configurable Lookup Tables	1	1	1
Window Watchdog	1	1	1
Event System channels	6	6	6
General purpose I/O	12	18	22
External interrupts	12	18	22
CRCSCAN	1	1	1

Note:

1. The PTC takes control over the ADC0 while the PTC is used.

2. Ordering Information

2.1 ATtiny161x

Table 2-1. ATtiny1617 Ordering Codes

Ordering Code[1]	Flash	Package Type (GPC)	Leads	Power Supply	Operational Range	Carrier Type
ATtiny1617-MNR	16KB	QFN (ZHA)	24	1.8V - 5.5V	Industrial (-40°C to +105°C)	Tape & Reel
ATtiny1617-MFR	16KB	QFN (ZHA)	24	1.8V - 5.5V	Industrial (-40°C to +125°C)	Tape & Reel

Table 2-2. ATtiny1616 Ordering Codes

Ordering Code[1]	Flash	Package Type (GPC)	Leads	Power Supply	Operational Range	Carrier Type
ATtiny1616-MNR	16KB	QFN (ZCL)	20	1.8V - 5.5V	Industrial (-40°C to +105°C)	Tape & Reel
ATtiny1616-MFR	16KB	QFN (ZCL)	20	1.8V - 5.5V	Industrial (-40°C to +125°C)	Tape & Reel
ATtiny1616-SNR	16KB	SOIC300 (SRJ)	20	1.8V - 5.5V	Industrial (-40°C to +105°C)	Tape & Reel
ATtiny1616-SFR	16KB	SOIC300 (SRJ)	20	1.8V - 5.5V	Industrial (-40°C to +125°C)	Tape & Reel

Table 2-3. ATtiny1614 Ordering Codes

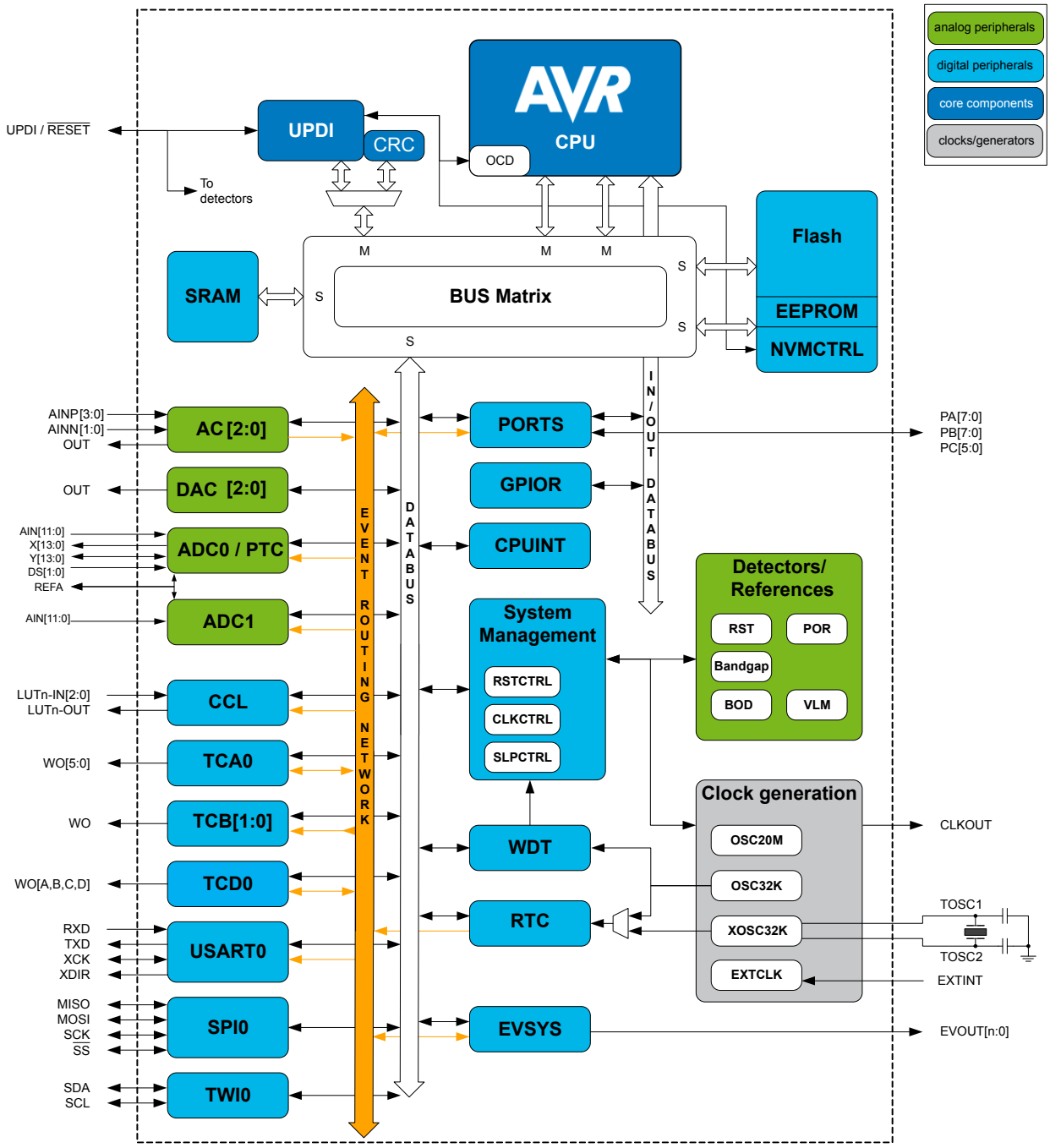
Ordering Code[1]	Flash	Package Type (GPC)	Leads	Power Supply	Operational Range	Carrier Type
ATtiny1614-SSNR	16KB	SOIC150 (SVQ)	14	1.8V - 5.5V	Industrial (-40°C to +105°C)	Tape & Reel
ATtiny1614-SSFR	16KB	SOIC150 (SVQ)	14	1.8V - 5.5V	Industrial (-40°C to +125°C)	Tape & Reel

Note:

1. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

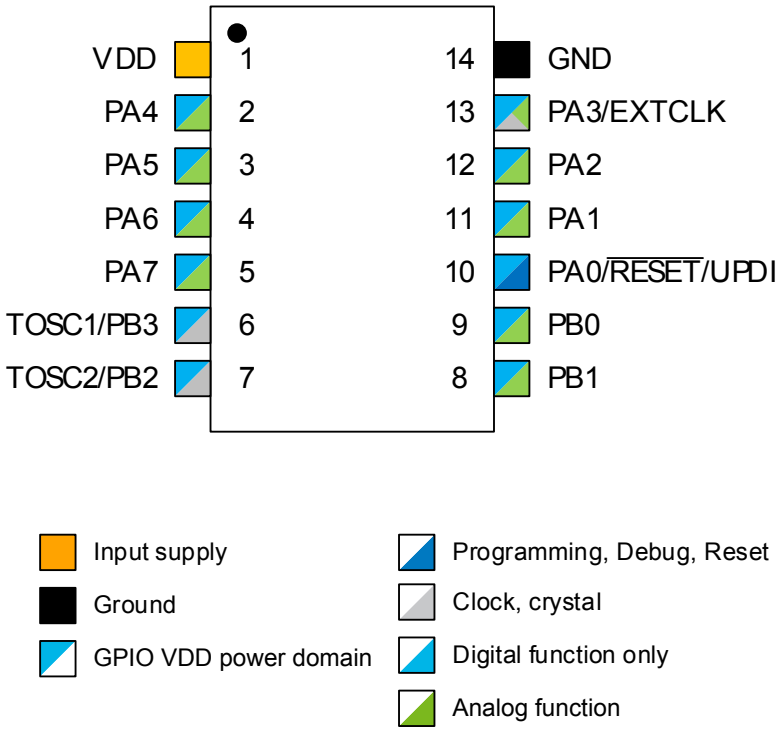
3. Block Diagram

Figure 3-1. ATtiny1614/1616/1617 Block Diagram

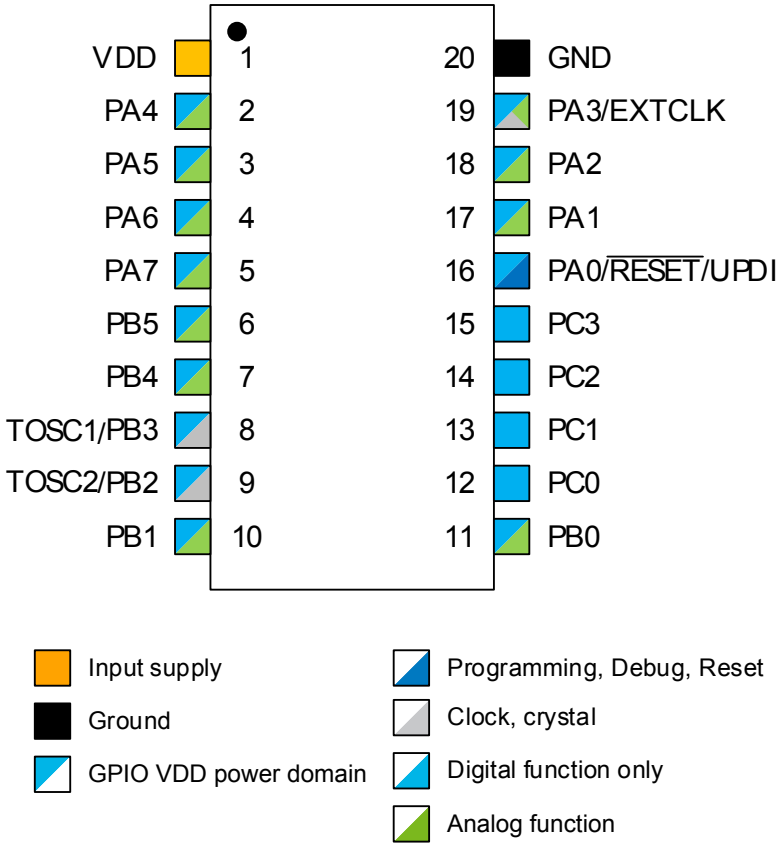


4. Pinout

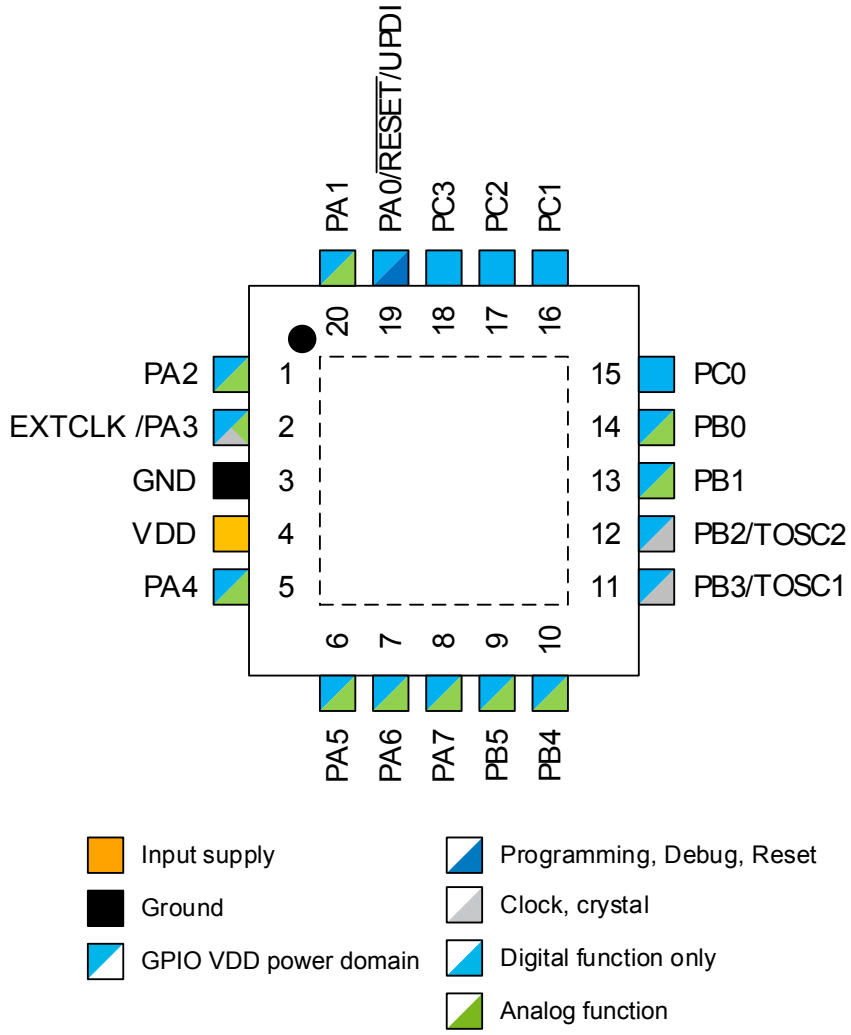
4.1 14-pin SOIC



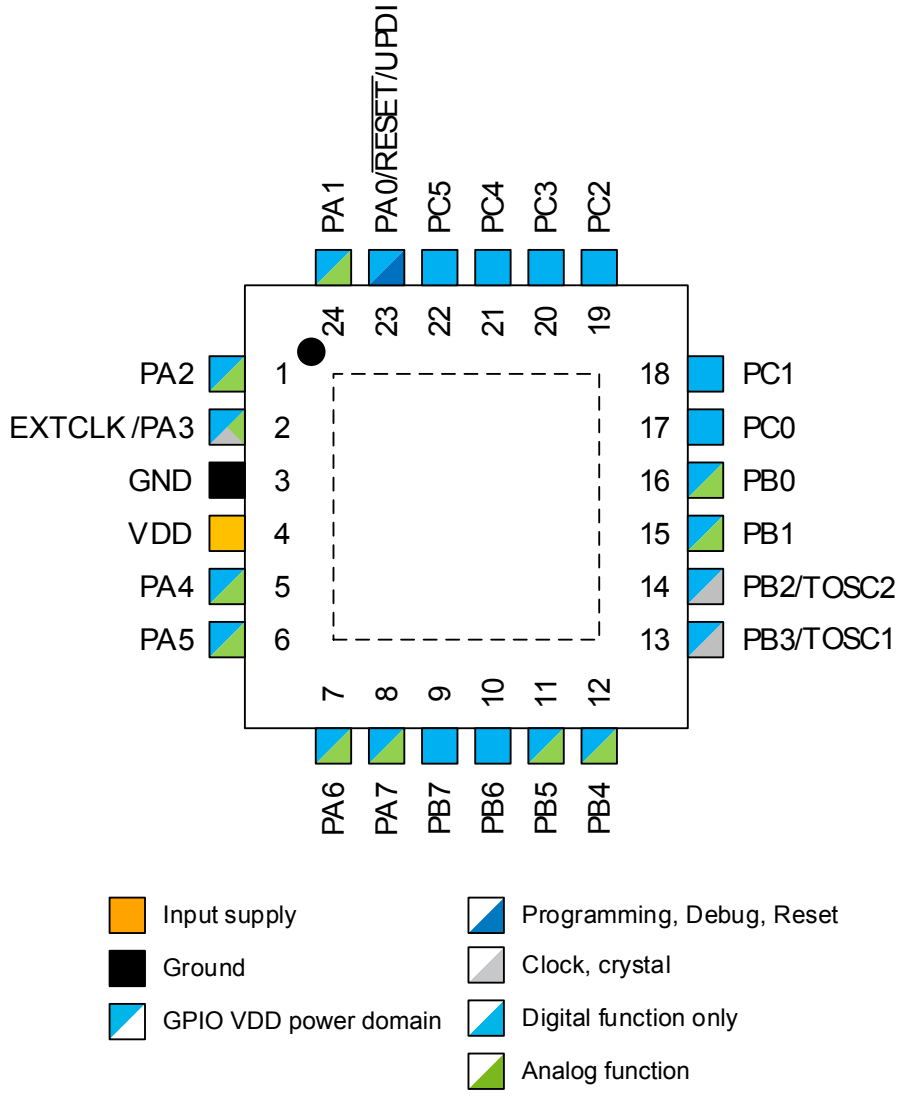
4.2 20-pin SOIC



4.3 20-pin QFN


PA1
PA0/RESET/UPDI
PC3
PC2
PC1
20
19
18
17
16
PA2
1
EXTCLK /PA3
2
GND
3
VDD
4
PA4
5
15
PC0
14
PB0
13
PB1
12
PB2/TOSC2
11
PB3/TOSC1
6
7
8
9
10
PA5
PA6
PA7
PB5
PB4
Input supply
Ground
GPIO VDD power domain
Programming, Debug, Reset
Clock, crystal
Digital function only
Analog function

4.4 24-pin QFN


PA1
PA0/RESET/UPDI
PC5
PC4
PC3
PC2
24
23
22
21
20
19
PA2
1
EXTCLK /PA3
2
GND
3
VDD
4
PA4
5
PA5
6
18
PC1
17
PC0
16
PB0
15
PB1
14
PB2/TOSC2
13
PB3/TOSC1
7
8
9
10
11
12
PA6
PA7
PB7
PB6
PB5
PB4
Input supply
Ground
GPIO VDD power domain
Programming, Debug, Reset
Clock, crystal
Digital function only
Analog function

5. I/O Multiplexing and Considerations

5.1 Multiplexed Signals

Table 5-1. PORT Function Multiplexing

QFN 24-pin	QFN 20-pin	SOIC 20-pin	SOIC 14-pin	Pin Name (1,2)	Other/ Special	ADC0	ADC1	PTC (3)	AC0	AC1	AC2	DAC0	USART0	SPI0	TWI0	TCA0	TCBn	TCD0	CCL
23	19	16	10	PA0	$\overline{\text{RESET}}$ $\overline{\text{T}}$ UPDI	AIN0													LUT0-IN0
24	20	17	11	PA1	BREAK	AIN1							TXD	MOSI	SDA				LUT0-IN1
1	1	18	12	PA2	EVOUT0	AIN2							RxD	MISO	SCL				LUT0-IN2
2	2	19	13	PA3	EXTCLK	AIN3							XCK	SCK		WO3	TCB1 WO		
3	3	20	14	GND															
4	4	1	1	VDD															
5	5	2	2	PA4		AIN4	AIN0	X0/Y0					XDIR	$\overline{\text{SS}}$		WO4		WOA	LUT0-OUT
6	6	3	3	PA5	VREFA	AIN5	AIN1	X1/Y1	OUT	AINN0						WO5	TCB0 WO	WOB	
7	7	4	4	PA6		AIN6	AIN2	X2/Y2	AINN0	AINP1	AINP0	OUT							
8	8	5	5	PA7		AIN7	AIN3	X3/Y3	AINP0	AINP0	AINN0								LUT1-OUT
9				PB7			AIN4			AINN1	AINP3								
10				PB6			AIN5		AINP3		AINN1								
11	9	6		PB5	CLKOUT	AIN8		X12/Y12	AINP1		AINP2					WO2			
12	10	7		PB4		AIN9		X13/Y13/	AINN1	AINP3						WO1			LUT0-OUT
13	11	8	6	PB3	TOSC1					OUT			RxD			WO0			
14	12	9	7	PB2	TOSC2, EVOUT1						OUT		TxD			WO2			
15	13	10	8	PB1		AIN10		X4/Y4	AINP2				XCK		SDA	WO1			
16	14	11	9	PB0		AIN11		X5/Y5		AINP2	AINP1		XDIR		SCL	WO0			
17	15	12		PC0			AIN6	X6/Y6						SCK			TCB0 WO	WOC	
18	16	13		PC1			AIN7	X7/Y7						MISO				WOD	LUT1-OUT
19	17	14		PC2	EVOUT2		AIN8	X9/Y8						MOSI					
20	18	15		PC3			AIN9	X9/Y9						$\overline{\text{SS}}$		WO3			LUT1-IN0
21				PC4	BREAK		AIN10	X10/Y10								WO4	TCB1 WO		LUT1-IN1
22				PC5			AIN11	X11/Y11								WO5			LUT1-IN2

Note:

1. Pins names are of type P*xn*, with *x* being the PORT instance (A,B) and *n* the pin number. Notation for signals is PORT*x*_PIN*n*. All pins can be used as event input.
2. All pins can be used for external interrupt, where pins P*x*2 and P*x*6 of each port have full asynchronous detection.
3. Every PTC line can be configured as X-line or Y-line.

Tip: Signals on alternative pin locations are in `typewriter` font.

6. Memories

6.1 Overview

The main memories are SRAM data memory, EEPROM data memory, and Flash program memory. In addition, the peripheral registers are located in the I/O memory space.

Table 6-1. Physical Properties of EEPROM

Property	ATtiny1617/1616/1614
Size	256B
Page size	32B
Number of pages	8
Start address	0x1400

Table 6-2. Physical Properties of SRAM

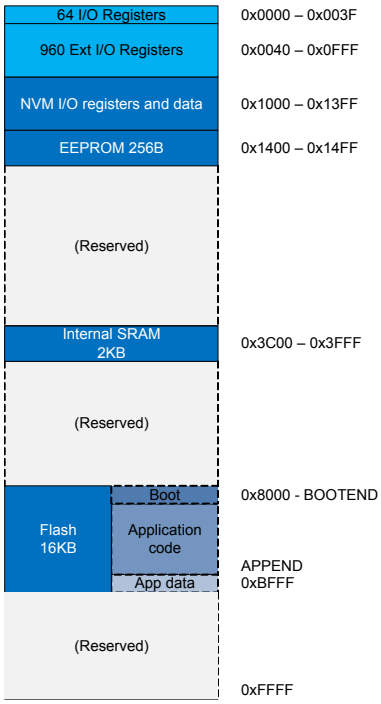
Property	ATtiny1617/1616/1614
Size	2KB
Start address	0x3800

Table 6-3. Physical Properties of Flash Memory

Property	ATtiny1617/1616/1614
Size	16KB
Page size	64B
Number of pages	256
Start address	0x8000

6.2 Memory Map

Figure 6-1. Memory Map ATtiny1617/ATtiny1616/ATtiny1614



6.3 In-System Reprogrammable Flash Program Memory

The ATtiny1614/1616/1617 contains 16KB On-Chip In-System Reprogrammable Flash memory for program storage. Since all AVR instructions are 16 or 32 bits wide, the Flash is organized as 4K x 16. For write protection, the Flash Program memory space can be divided into three sections: Boot Loader section, Application code section and Application data section, with restricted access rights among them.

The program counter is 13 bits wide to address the whole program memory. The procedure for writing Flash memory is described in detail in the documentation of the Non-Volatile Memory Controller (NVMCTRL) peripheral.

The entire Flash memory is mapped in the memory space and is accessible with normal LD/ST instructions as well as the LPM instruction. For LD/ST instructions, the Flash is mapped from address 0x8000. For the LPM instruction, the Flash start address is 0x0000.

The ATtiny1614/1616/1617 also has a CRC module that is a master on the bus. If the CRC is configured to run in the background it will read the Flash memory and can affect the program timing.

Related Links

Configuration Summary

NVMCTRL - Non Volatile Memory Controller

6.4 SRAM Data Memory

The 2KB SRAM is used for data storage and stack.

Related Links

AVR CPU

Stack and Stack Pointer

6.5 EEPROM Data Memory

The ATtiny1614/1616/1617 has 256 bytes of EEPROM data memory, see Memory Map. The EEPROM memory supports single byte read and write. The EEPROM is controlled by the Non-Volatile Memory Controller (NVMCTRL).

Related Links

NVMCTRL - Non Volatile Memory Controller

BOD - Brownout Detector

6.6 User Row

In addition to the EEPROM, the ATtiny1614/1616/1617 has one extra page of EEPROM memory that can be used for firmware settings, the User Row (USERROW). This memory supports single byte read and write as the normal EEPROM. The CPU can write and read this memory as normal EEPROM and the UPDI can write and read it as a normal EEPROM memory if the part is unlocked. The User Row can also be written by the UPDI when the part is locked. USERROW is not affected by a chip erase.

Related Links

NVMCTRL - Non Volatile Memory Controller

UPDI - Unified Program and Debug Interface

6.7 I/O Memory

All ATtiny1614/1616/1617 I/Os and peripherals are located in the I/O space. The I/O address range from 0x00 to 0x3F can be accessed in a single cycle using IN and OUT instructions. The Extended I/O space from 0x0040 - 0x0FFF can be accessed by the LD/LDS/LDD and ST/STS/STD instructions, transferring data between the 32 general purpose working registers and the I/O space.

I/O Registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions. Refer to the Instruction Set section for more details.

For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.

Some of the interrupt flags are cleared by writing a '1' to them. On ATtiny1614/1616/1617 devices, the CBI and SBI instructions will only operate on the specified bit, and can therefore be used on registers containing such interrupt flags. The CBI and SBI instructions work with registers 0x00 - 0x1F only.

General Purpose I/O Registers

The ATtiny1614/1616/1617 devices provide four General Purpose I/O Registers. These registers can be used for storing any information, and they are particularly useful for storing global variables and interrupt flags. General Purpose I/O Registers, which recide in the address range 0x1C - 0x1F, are directly bit-accessible using the SBI, CBI, SBIS, and SBIC instructions.

6.8 FUSES - Configuration and User Fuses

Fuses are part of the non-volatile memory and holds factory calibration data and device configuration. The fuses are available from device power-up. The fuses can be read by the CPU or the UPDI, but can

only be programmed or cleared by the UPDI. The configuration and calibration values stored in the fuses are written to their respective target registers at the end of the start-up sequence.

The content of the Signature Row fuses (SIGROW) is pre-programmed, and cannot be altered. SIGROW holds information such as device ID, serial number, and calibration values.

The fuses for peripheral configuration (FUSE) are pre-programmed, but can be altered by the user. Altered values in the configuration fuses will be effective only after a Reset.

This device also provides a User Row fuse area (USERROW) that can hold application data. The USERROW can be programmed on a locked device by the UPDI. This can be used for final configuration without having programming or debugging capabilities enabled.

6.8.1 Signature Row Summary - SIGROW

Offset	Name	Bit Pos.								
0x00	DEVICEID0	7:0	DEVICEID[7:0]							
0x01	DEVICEID1	7:0	DEVICEID[7:0]							
0x02	DEVICEID2	7:0	DEVICEID[7:0]							
0x03	SERNUM0	7:0	SERNUM[7:0]							
0x04	SERNUM1	7:0	SERNUM[7:0]							
0x05	SERNUM2	7:0	SERNUM[7:0]							
0x06	SERNUM3	7:0	SERNUM[7:0]							
0x07	SERNUM4	7:0	SERNUM[7:0]							
0x08	SERNUM5	7:0	SERNUM[7:0]							
0x09	SERNUM6	7:0	SERNUM[7:0]							
0x0A	SERNUM7	7:0	SERNUM[7:0]							
0x0B	SERNUM8	7:0	SERNUM[7:0]							
0x0C	SERNUM9	7:0	SERNUM[7:0]							
0x0D ... 0x1F	Reserved									
0x20	TEMPSENSE0	7:0	TEMPSENSE[7:0]							
0x21	TEMPSENSE1	7:0	TEMPSENSE[7:0]							
0x22	OSC16ERR3V	7:0	OSC16ERR3V[7:0]							
0x23	OSC16ERR5V	7:0	OSC16ERR5V[7:0]							
0x24	OSC20ERR3V	7:0	OSC20ERR3V[7:0]							
0x25	OSC20ERR5V	7:0	OSC20ERR5V[7:0]							

6.8.2 Signature Row Description

6.8.2.1 Device ID n

Each device has a Device ID, identifying the device and its properties, such as memory sizes, pin count, and die revision. This can be used to identify a device and hence, the available features by software. The Device ID consists of three bytes: SIGROW.DEVICEID[2:0].

Name: DEVICEIDn
Offset: 0x00 + n*0x01 [n=0..2]
Reset: [Device ID]
Property: -

Bit	7	6	5	4	3	2	1	0
	DEVICEID[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bits 7:0 – DEVICEID[7:0]: Byte n of the Device ID

6.8.2.2 Serial Number Byte n

Each device has an individual serial number, representing a unique ID. This can be used to identify a specific device in the field. The serial number consists of ten bytes: SIGROW.SERNUM[9:0].

Name: SERNUMn
Offset: 0x03 + n*0x01 [n=0..9]
Reset: [device serial number]
Property: -

Bit	7	6	5	4	3	2	1	0
	SERNUM[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bits 7:0 – SERNUM[7:0]: Serial Number Byte n

6.8.2.3 Temperature Sensor Calibration n

These registers contain correction factors for temperature measurements by the ADC. SIGROW.TEMPSENSE0 is a correction factor for the gain/slope (unsigned), SIGROW.TEMPSENSE1 is a correction factor for the offset (signed).

Name: TEMPSENSEn
Offset: 0x20 + n*0x01 [n=0..1]
Reset: [Temperature sensor calibration value]
Property: -

Bit	7	6	5	4	3	2	1	0
	TEMPSENSE[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – TEMPSENSE[7:0]: Temperature Sensor Calibration Byte n

6.8.2.4 OSC16 error at 3V

Name: OSC16ERR3V
Offset: 0x22
Reset: [Oscillator frequency error value]
Property: -

Bit	7	6	5	4	3	2	1	0
	OSC16ERR3V[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – OSC16ERR3V[7:0]: OSC16 error at 3V
This registers contain the signed oscillator frequency error value when running at internal 16MHz at 3V, as measured during production.

6.8.2.5 OSC16 error at 5V

Name: OSC16ERR5V
Offset: 0x23