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ATtiny202/402

AVR® Microcontroller with Core Independent Peripherals and picoPower® Technology

Introduction

The ATtiny202/402 microcontrollers are using the high-performance, low-power AVR® RISC architecture, and are capable of running at up to 20 MHz, with up to 2/4 KB Flash, 128/256 bytes of SRAM, and 64/128 bytes of EEPROM in a 8-pin package. The series uses the latest technologies with a flexible and low-power architecture including Event System and SleepWalking, accurate analog features, and advanced peripherals.

Features

- CPU:
  - AVR® 8-bit CPU
  - Running at up to 20 MHz
  - Single cycle I/O access
  - Two-level interrupt controller
  - Two-cycle hardware multiplier
- Memories:
  - 2/4 KB In-system self-programmable Flash memory
  - 64/128B EEPROM
  - 128/256B SRAM
  - Write/Erase Cycles: 10,000 Flash/100,000 EEPROM
  - Data Retention: 20 Years at 85°C
- System:
  - Power-on Reset (POR)
  - Brown-out Detection (BOD)
  - Clock Options:
    - 16/20 MHz Low-Power Internal RC Oscillator with:
      - ±3% Accuracy over full temperature and voltage range
      - ±2% Drift over limited temperature and 1.8 ... 3.6V voltage range
    - 32.768 kHz Ultra Low-Power (ULP) Internal RC Oscillator with ±10% Accuracy, ±2% Calibration Step Size
    - External Clock Input
  - Single Pin Unified Program Debug Interface (UPDI)
  - Three Sleep Modes:
    - Idle with all peripherals running and mode for immediate wake-up time

    - Standby
        - Configurable operation of selected peripherals
        - SleepWalking peripherals
    - Power-down with wake-up functionality
- Peripherals:
    - 3-channel Event System
    - One 16-bit Timer/Counter Type A with Dedicated Period Register, Three Compare Channels (TCA)
    - One 16-bit Timer/Counter Type B with Input Capture (TCB)
    - One 16-bit Real-Time Counter (RTC) running from Internal RC Oscillator
    - One USART with fractional Baud Rate Generator, Auto-baud, and Start-of-frame Detection
    - Master/Slave Serial Peripheral Interface (SPI)
    - Master/Slave TWI with Dual Address Match
        - Standard mode (Sm, 100 kHz)
        - Fast mode (Fm, 400 kHz)
        - Fast mode Plus (Fm+, 1 MHz)
    - Configurable Custom Logic (CCL) with Two Programmable Look-up Tables (LUT)
    - Analog Comparator (AC)
    - 10-bit 115 ksps Analog-to-Digital Converter (ADC)
    - Five selectable internal voltage references: 0.55V, 1.1V, 1.5V, 2.5V, and 4.3V
    - Automated CRC memory scan
    - Watchdog Timer (WDT) with Window mode, with separate on-chip oscillator
    - External interrupt on all general purpose pins
- I/O and Packages:
    - 6 Programmable I/O lines
    - 8-pin SOIC150
- Temperature Ranges:
    - -40°C to 105°C
    - -40°C to 125°C Temperature graded device options available
- Speed Grades:
    - 0-5 MHz @ 1.8V – 5.5V
    - 0-10 MHz @ 2.7V – 5.5V
    - 0-20 MHz @ 4.5V – 5.5V

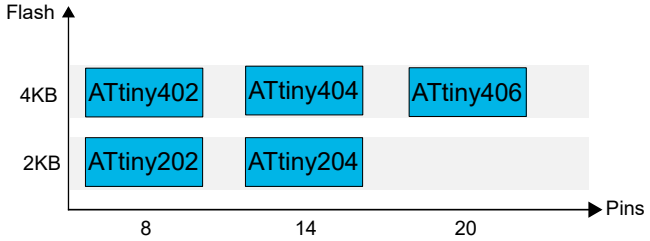
Table of Contents

1. tinyAVR® 0-Series Overview

The figure below shows the tinyAVR 0-series, laying out pin count variants and memory sizes:

- Vertical migration can be done upwards without code modification since these devices are pin compatible and provide the same or additional features. Downward migration may require code modification due to fewer available instances of some peripherals.
- Horizontal migration to the left reduces the pin count and therefore, the available features.

Figure 1-1. Device Family Overview

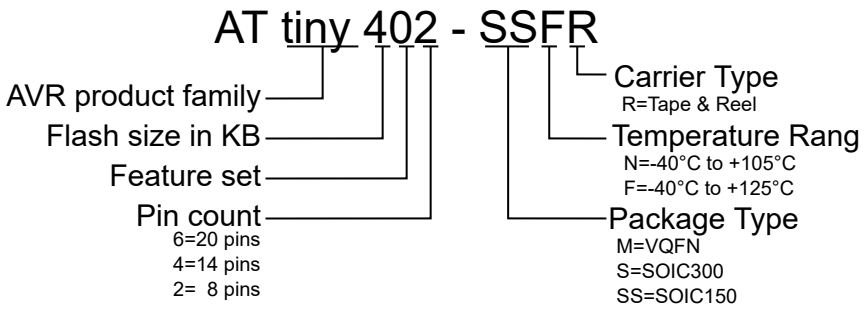


The fully compatible variants of the ATtiny devices, that is the vertical migration option shown in the figure above, come with both smaller and larger Flash memories.

Devices with different Flash memory size typically also have different SRAM and EEPROM.

The name of a device of the ATtiny family contains information as depicted below (not all options are available):

Figure 1-2. Device Designations



1.1 Configuration Summary

1.1.1 Peripheral Summary

Table 1-1. Peripheral Summary

	ATtiny202	ATtiny402
Pins	8	8
SRAM	128B	256B
Flash	2 KB	4 KB

	ATtiny202	ATtiny402
EEPROM	64B	128B
Max. frequency (MHz)	20	20
16-bit Timer/Counter type A (TCA)	1	1
16-bit Timer/Counter type B (TCB)	1	1
12-bit Timer/Counter type D (TCD)	No	No
Real-Time Counter (RTC)	1	1
USART	1	1
SPI	1	1
TWI (I^2C)	1	1
ADC	1	1
ADC channels	6	6
DAC	No	No
AC	1	1
AC inputs	1p/1n	1p/1n
Peripheral Touch Controller (PTC)	No	No
Custom Logic	1	1
Window Watchdog	1	1
Event System channels	3	3
General purpose I/O	6	6
External interrupts	6	6
CRCSCAN	1	1

2. Ordering Information

2.1 ATtiny202

Table 2-1. ATtiny202 Ordering Codes

Ordering Code[1]	Flash	Package Type (GPC)	Leads	Power Supply	Operational Range	Carrier Type
ATtiny202-SSNR	2 KB	SOIC150 (SWB)	8	1.8V - 5.5V	Industrial (-40°C +105°C)	Tape & Reel
ATtiny202-SSFR	2 KB	SOIC150 (SWB)	8	1.8V - 5.5V	Industrial (-40°C +125°C)	Tape & Reel

1. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

2.2 ATtiny402

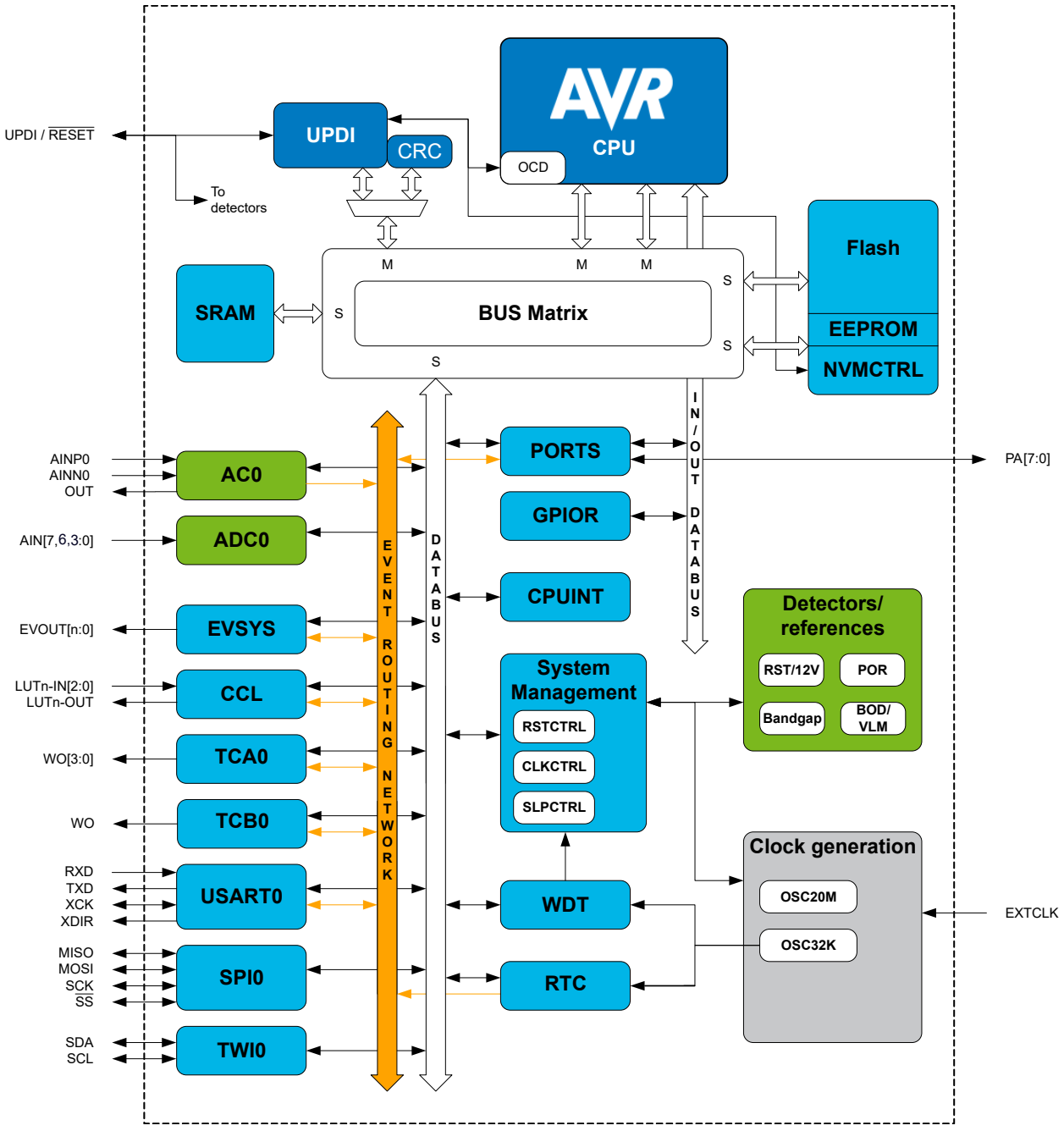
Table 2-2. ATtiny402 Ordering Codes

Ordering Code[1]	Flash	Package Type (GPC)	Leads	Power Supply	Operational Range	Carrier Type
ATtiny402-SSNR	4 KB	SOIC150 (SWB)	8	1.8V - 5.5V	Industrial (-40°C +105°C)	Tape & Reel
ATtiny402-SSFR	4 KB	SOIC150 (SWB)	8	1.8V - 5.5V	Industrial (-40°C +125°C)	Tape & Reel

1. Pb-free packaging complies with the European Directive for Restriction of Hazardous Substances (RoHS directive). They are also Halide free and fully Green.

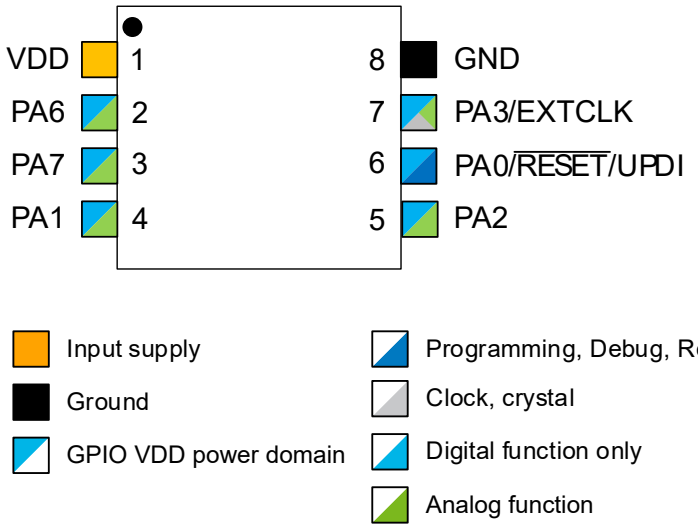
3. Block Diagram

Figure 3-1. Block Diagram



4. Pinout

4.1 8-Pin SOIC



5. I/O Multiplexing and Considerations

5.1 Multiplexed Signals

Table 5-1. PORT Function Multiplexing

SOIC 8-pin	Pin Name (1,2)	Other/Special	ADC0	AC0	USART0	SPI0	TWI0	TCA0	TCB0	CCL
6	PA0	$\overline{\text{RESET}}$/UPDI	AIN0		XDIR	$\overline{\text{SS}}$				LUT0-IN0
5	PA1		AIN1		TXD	MOSI	SDA	WO1		LUT0-IN1
4	PA2	EVOUT0	AIN2		RxD	MISO	SCL	WO2		LUT0-IN2
7	PA3	EXTCLK	AIN3	OUT	XCK	SCK		WO0/WO3		
8	GND									
1	VDD									
2	PA6		AIN6	AINN0	TXD	MOSI			WO	LUT0-OUT
3	PA7		AIN7	AINP0	RXD	MISO		WO0		LUT1-OUT

Note:

1. Pin names are of type P*xn*, with *x* being the PORT instance (A, B) and *n* the pin number. Notation for signals is PORT*x*_PIN*n*. All pins can be used as event input.
2. All pins can be used for external interrupt, where pins P*x*2 and P*x*6 of each port have full asynchronous detection.

Tip: Signals on alternative pin locations are in `typewriter` font.
See PORTMUX chapter for selecting the altarnative pin locations.

6. Memories

6.1 Overview

The main memories are SRAM data memory, EEPROM data memory, and Flash program memory. In addition, the peripheral registers are located in the I/O memory space.

Table 6-1. Physical Properties of Flash Memory

Property	ATtiny202	ATtiny402
Size	2 KB	4 KB
Page size	64B	64B
Number of pages	32	64
Start address	0x8000	0x8000

Table 6-2. Physical Properties of SRAM

Property	ATtiny202	ATtiny402
Size	128B	256B
Start address	0x3F80	0x3F00

Table 6-3. Physical Properties of EEPROM

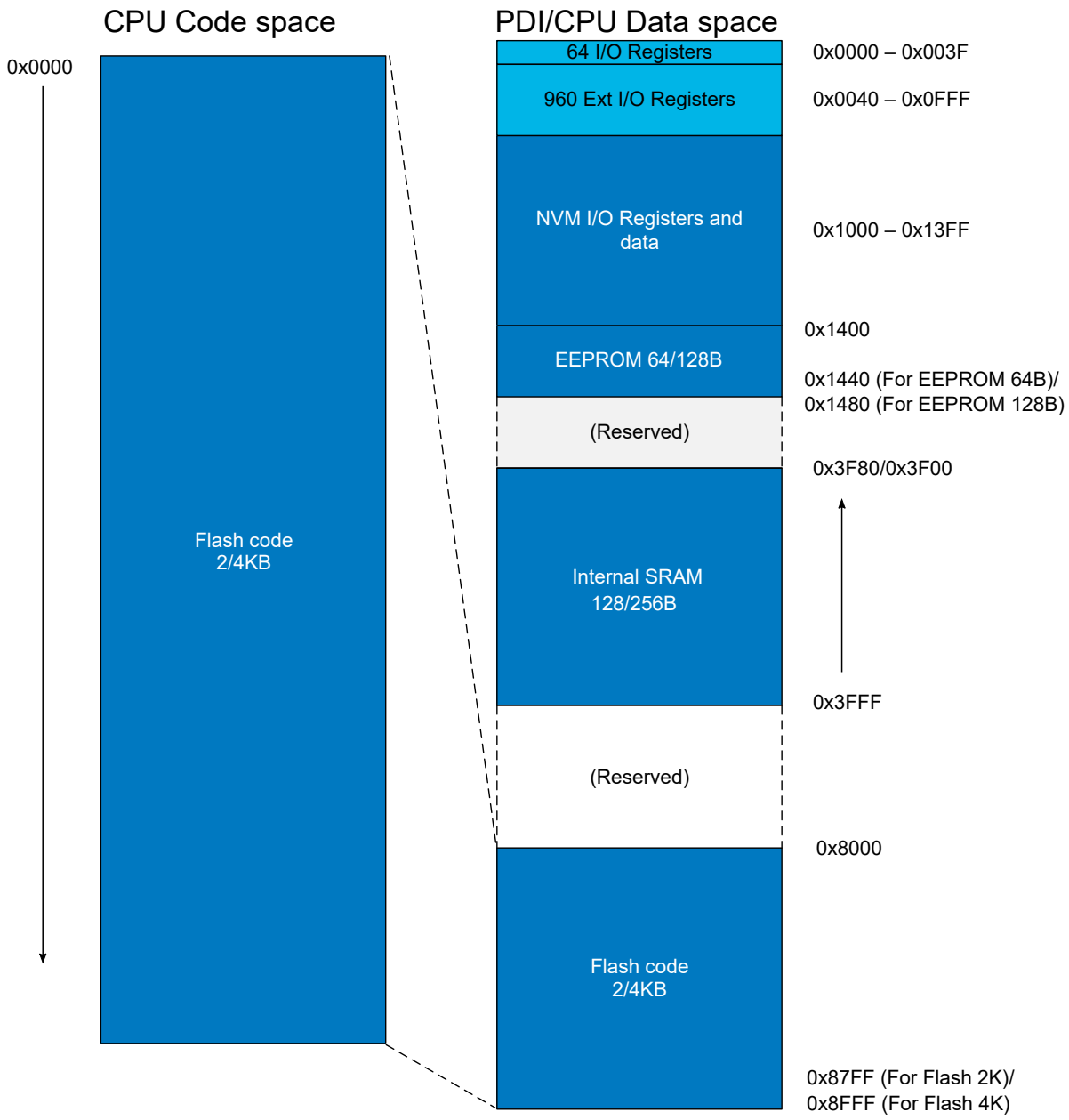
Property	ATtiny202	ATtiny402
Size	64B	128B
Page size	32B	32B
Number of pages	2	4
Start address	0x1400	0x1400

Related Links

I/O Memory

6.2 Memory Map

Figure 6-1. Memory Map: Flash 2/4 KB, Internal SRAM 128/256B, EEPROM 64/128B



6.3 In-System Reprogrammable Flash Program Memory

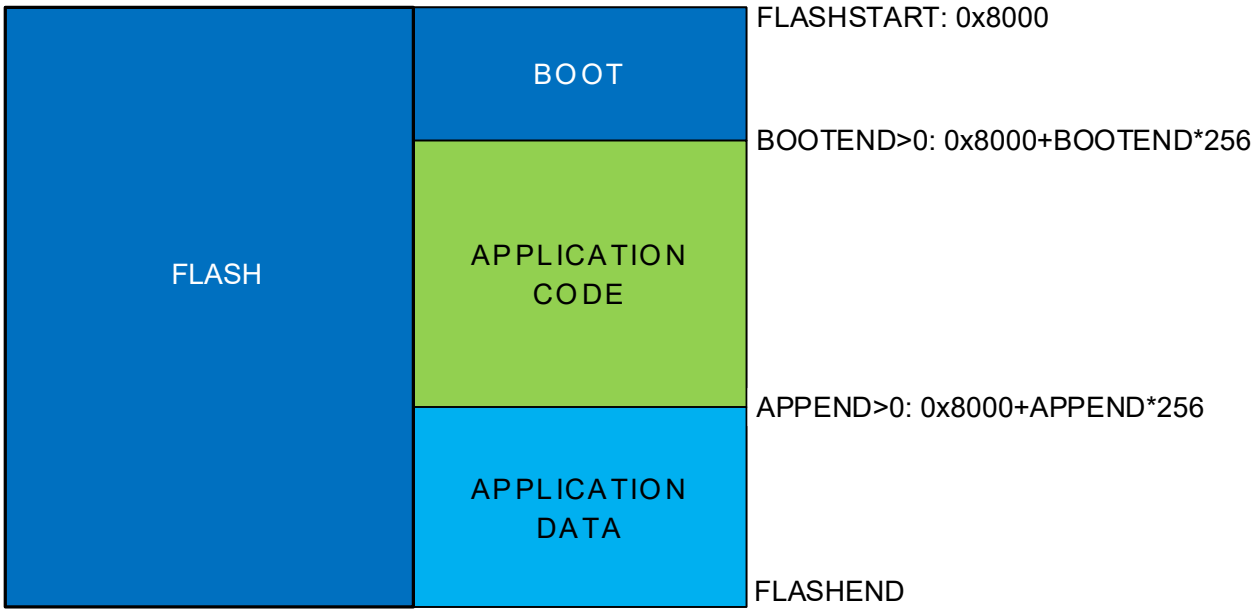
The ATtiny202/402 contains 4/2 KB on-chip in-system reprogrammable Flash memory for program storage. Since all AVR instructions are 16 or 32 bits wide, the Flash is organized as 4K x 16. For write protection, the Flash program memory space can be divided into three sections (see the illustration below): Bootloader section, application code section, and application data section, with restricted access rights among them.

The Program Counter (PC) is 11-bits wide to address the whole program memory. The procedure for writing Flash memory is described in detail in the documentation of the Nonvolatile Memory Controller (NVMCTRL) peripheral.

The entire Flash memory is mapped in the memory space and is accessible with normal LD/ST instructions as well as the LPM instruction. For LD/ST instructions, the Flash is mapped from address 0x8000. For the LPM instruction, the Flash start address is 0x0000.

The ATtiny202/402 also has a CRC peripheral that is a master on the bus.

Figure 6-2. Flash and the Three Sections



Related Links

Configuration Summary

Nonvolatile Memory Controller (NVMCTRL)

6.4 SRAM Data Memory

The 128B/256B SRAM is used for data storage and stack.

Related Links

AVR CPU

Stack and Stack Pointer

6.5 EEPROM Data Memory

The ATtiny202/402 has 64/128 bytes of EEPROM data memory, see Memory Map section. The EEPROM memory supports single byte read and write. The EEPROM is controlled by the Nonvolatile Memory Controller (NVMCTRL).

Related Links

Memory Map

Nonvolatile Memory Controller (NVMCTRL)

6.6 User Row

In addition to the EEPROM, the ATtiny202/402 has one extra page of EEPROM memory that can be used for firmware settings, the User Row (USERROW). This memory supports single byte read and write as the normal EEPROM. The CPU can write and read this memory as normal EEPROM and the UPDI can write and read it as a normal EEPROM memory if the part is unlocked. The User Row can be written by the UPDI when the part is locked. USERROW is not affected by a chip erase.

Related Links

Memory Map
Nonvolatile Memory Controller (NVMCTRL)
Unified Program and Debug Interface (UPDI)

6.7 Signature Bytes

All ATtiny microcontrollers have a 3-byte signature code that identifies the device. This code can be read in both Serial and Parallel mode. The three bytes reside in a separate address space. For the device, the signature bytes are given in the following table.

Note: When the device is locked, only the System Information Block (SIB) can be obtained.

Table 6-4. Device ID

Device Name	Signature Bytes Address		
	0x00	0x01	0x02
ATtiny202	0x1E	0x91	0x23
ATtiny402	0x1E	0x92	0x27

Related Links

System Information Block

6.8 Memory Section Access from CPU and UPDI on Locked Device

The device can be locked so that the memories cannot be read using the UPDI. The locking protects both the Flash (all BOOT, APPCODE, and APPDATA sections), SRAM, and the EEPROM including the FUSE data. This prevents successful reading of application data or code using the debugger interface. Regular memory access from within the application still is enabled.

The device is locked by writing any non-valid value to the LOCKBIT bit field in FUSE.LOCKBIT.

Table 6-5. Memory Access in Unlocked Mode (FUSE.LOCKBIT Valid)(1)

Memory Section	CPU Access		UPDI Access	
	Read	Write	Read	Write
SRAM	Yes	Yes	Yes	Yes
Registers	Yes	Yes	Yes	Yes
Flash	Yes	Yes	Yes	Yes

Memory Section	CPU Access		UPDI Access	
	Read	Write	Read	Write
EEPROM	Yes	Yes	Yes	Yes
USERROW	Yes	Yes	Yes	Yes
SIGROW	Yes	No	Yes	No
Other Fuses	Yes	No	Yes	Yes

Table 6-6. Memory Access in Locked Mode (FUSE.LOCKBIT Invalid)(1)

Memory Section	CPU Access		UPDI Access	
	Read	Write	Read	Write
SRAM	Yes	Yes	No	No
Registers	Yes	Yes	No	No
Flash	Yes	Yes	No	No
EEPROM	Yes	No	No	No
USERROW	Yes	Yes	No	Yes(2)
SIGROW	Yes	No	No	No
Other Fuses	Yes	No	No	No

Note:

1. Read operations marked No in the tables may appear to be successful, but the data is corrupt. Hence, any attempt of code validation through the UPDI will fail on these memory sections.
2. In Locked mode, the USERROW can be written blindly using the fuse Write command, but the current USERROW values cannot be read out.

Important: The only way to unlock a device is a CHIPERASE, which will erase all device memories to factory default so that no application data is retained.

Related Links

Fuse Summary - FUSE
LOCKBIT
Unified Program and Debug Interface (UPDI)
Enabling of KEY Protected Interfaces

6.9 I/O Memory

All ATtiny202/402 I/Os and peripherals are located in the I/O memory space. The I/O address range from 0x00 to 0x3F can be accessed in a single cycle using `IN` and `OUT` instructions. The extended I/O memory space from 0x0040 - 0x0FFF can be accessed by the `LD`/`LDS`/`LDD` and `ST`/`STS`/`STD` instructions, transferring data between the 32 general purpose working registers and the I/O memory space.

I/O registers within the address range 0x00 - 0x1F are directly bit accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions. Refer to the Instruction Set section for more details.

For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.

Some of the interrupt flags are cleared by writing a '1' to them. On ATtiny202/402 devices, the CBI and SBI instructions will only operate on the specified bit, and can be used on registers containing such interrupt flags. The CBI and SBI instructions work with registers 0x00 - 0x1F only.

General Purpose I/O Registers

The ATtiny202/402 devices provide four general purpose I/O registers. These registers can be used for storing any information, and they are particularly useful for storing global variables and interrupt flags. general purpose I/O registers, which reside in the address range 0x1C - 0x1F, are directly bit accessible using the SBI, CBI, SBIS, and SBIC instructions.

Related Links

Memory Map
Peripheral Module Address Map
Instruction Set Summary

6.9.1 Register Summary - GPIOR

Offset	Name	Bit Pos.								
0x00	GPIOR0	7:0	GPIOR[7:0]							
0x01	GPIOR1	7:0	GPIOR[7:0]							
0x02	GPIOR2	7:0	GPIOR[7:0]							
0x03	GPIOR3	7:0	GPIOR[7:0]							

6.9.2 Register Description - GPIOR

6.9.2.1 General Purpose I/O Register n

Name: GPIOR
Offset: 0x00 + n*0x01 [n=0..3]
Reset: 0x00
Property: -

These are general purpose registers that can be used to store data, such as global variables and flags, in the bit accessible I/O memory space.

Bit	7	6	5	4	3	2	1	0
	GPIOR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – GPIOR[7:0] GPIO Register byte

6.10 Configuration and User Fuses (FUSE)

Fuses are part of the nonvolatile memory and hold factory calibration data and device configuration. The fuses are available from device power-up. The fuses can be read by the CPU or the UPDI, but can only be programmed or cleared by the UPDI. The configuration and calibration values stored in the fuses are written to their respective target registers at the end of the start-up sequence.

The content of the Signature Row fuses (SIGROW) is pre-programmed and cannot be altered. SIGROW holds information such as device ID, serial number, and calibration values.

The fuses for peripheral configuration (FUSE) are pre-programmed but can be altered by the user. Altered values in the configuration fuse will be effective only after a Reset.
Note: When writing the fuses write all reserved bits to '1'.

This device provides a User Row fuse area (USERROW) that can hold application data. The USERROW can be programmed on a locked device by the UPDI. This can be used for final configuration without having programming or debugging capabilities enabled.

Related Links
Signature Row Description
Fuse Description

6.10.1 Signature Row Summary - SIGROW

Offset	Name	Bit Pos.									
0x00	DEVICEID0	7:0	DEVICEID[7:0]								
0x01	DEVICEID1	7:0	DEVICEID[7:0]								
0x02	DEVICEID2	7:0	DEVICEID[7:0]								
0x03	SERNUM0	7:0	SERNUM[7:0]								
0x04	SERNUM1	7:0	SERNUM[7:0]								
0x05	SERNUM2	7:0	SERNUM[7:0]								
0x06	SERNUM3	7:0	SERNUM[7:0]								
0x07	SERNUM4	7:0	SERNUM[7:0]								
0x08	SERNUM5	7:0	SERNUM[7:0]								
0x09	SERNUM6	7:0	SERNUM[7:0]								
0x0A	SERNUM7	7:0	SERNUM[7:0]								
0x0B	SERNUM8	7:0	SERNUM[7:0]								
0x0C	SERNUM9	7:0	SERNUM[7:0]								
0x0D ... 0x1F	Reserved										
0x20	TEMPSENSE0	7:0	TEMPSENSE[7:0]								
0x21	TEMPSENSE1	7:0	TEMPSENSE[7:0]								
0x22	OSC16ERR3V	7:0	OSC16ERR3V[7:0]								
0x23	OSC16ERR5V	7:0	OSC16ERR5V[7:0]								
0x24	OSC20ERR3V	7:0	OSC20ERR3V[7:0]								
0x25	OSC20ERR5V	7:0	OSC20ERR5V[7:0]								

6.10.2 Signature Row Description

6.10.2.1 Device ID n

Name: DEVICEIDn
Offset: 0x00 + n*0x01 [n=0..2]
Reset: [Device ID]
Property: -

Each device has a device ID identifying the device and its properties; such as memory sizes, pin count, and die revision. This can be used to identify a device and hence, the available features by software. The Device ID consists of three bytes: SIGROW.DEVICEID[2:0].

Bit	7	6	5	4	3	2	1	0
	DEVICEID[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bits 7:0 – DEVICEID[7:0] Byte n of the Device ID

6.10.2.2 Serial Number Byte n

Name: SERNUMn
Offset: 0x03 + n*0x01 [n=0..9]
Reset: [device serial number]
Property: -

Each device has an individual serial number, representing a unique ID. This can be used to identify a specific device in the field. The serial number consists of ten bytes: SIGROW.SERNUM[9:0].

Bit	7	6	5	4	3	2	1	0
	SERNUM[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bits 7:0 – SERNUM[7:0] Serial Number Byte n