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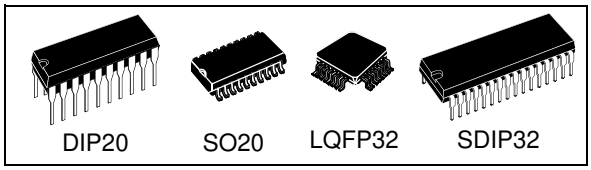
ST7FOXF1, ST7FOXK1, ST7FOXK2

8-bit MCU with single voltage Flash memory, SPI, I²C, ADC, timers

Features

- Memories
  - 4 to 8 Kbytes single voltage extended Flash (XFlash) Program memory with Read-Out Protection
    In-Circuit Programming and In-Application programming (ICP and IAP)
    Endurance: 1K write/erase cycles guaranteed
    Data retention: 20 years at 55 °C
  - 384 bytes RAM
- Clock, Reset and Supply Management
  - Low voltage supervisor (LVD) for safe power-on/off
  - Clock sources: Internal trimmable 8 MHz RC oscillator, auto wakeup internal low power - low frequency oscillator, crystal/ceramic resonator or external clock
  - External reset source and watchdog reset
  - Five power saving modes: Halt, Active-Halt, Auto Wakeup from Halt, Wait and Slow
- I/O Ports
  - Up to 24 multifunctional bidirectional I/Os
  - Up to 8 high sink outputs



- 6 timers
  - Configurable watchdog timer
  - Dual 8-bit Lite timers with prescaler, 1 real time base and 1 input capture
  - Dual 12-bit Auto-reload timers with 4 PWM outputs, input capture, output compare, dead-time generation and enhanced one pulse mode functions
  - One 16-bit timer
- Communication interfaces:
  - I²C multimaster interface
  - SPI synchronous serial interface
- A/D converter: up to 10 input channels
- Interrupt management
  - 13 interrupt vectors plus TRAP and RESET
- Instruction set
  - 8-bit data manipulation
  - 63 basic instructions with illegal opcode detection
  - 17 main addressing modes
  - 8 x 8 unsigned multiply instructions
- Development tools
  - Full HW/SW development package
  - DM (Debug Module)

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1 Description

The ST7FOX is a member of the ST7 microcontroller family. All ST7 devices are based on a common industry-standard 8-bit core, featuring an enhanced instruction set.

The device is positioned at the entry level of the 8-bit microcontroller range providing an attractive cost while at the same time embedding the most advanced features.

The ST7FOX features Flash memory with byte-by-byte In-Circuit Programming (ICP) and In-Application Programming (IAP) capability.

Under software control, the ST7FOX device can be placed in Wait, Slow, or Halt mode, reducing power consumption when the application is in idle or standby state.

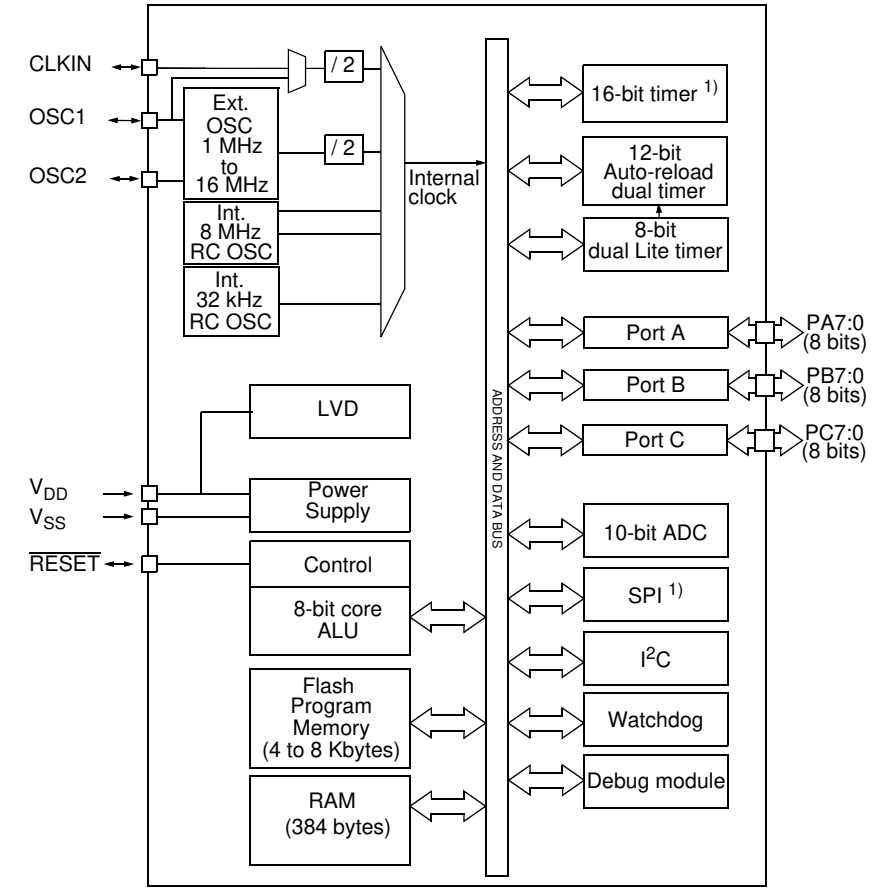
The enhanced instruction set and addressing modes of the ST7 offer both power and flexibility to software developers, enabling the design of highly efficient and compact application code. In addition to standard 8-bit data management, all ST7 microcontrollers feature true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes.

The ST7FOX features an on-chip Debug Module (DM) to support In-Circuit Debugging (ICD). For a description of the DM registers, refer to the ST7 ICC Protocol Reference Manual.

Table 1. Device summary

Features	ST7FOXF1 / ST7FOXK1	ST7FOXK2
Program memory - bytes	4K	8K
RAM (stack) - bytes	384 (128)	
Timers	Dual 8-bit timer, dual 12-bit AT (4 PWM)	Dual 8-bit timer, dual 12-bit AT (4 PWM), 1 x 16-bit timer
ADC	1 x 10-bit	
Peripherals	I²C	I²C and SPI
Packages	DIP20, SO20, LQFP32, SDIP32	LQFP32, SDIP32

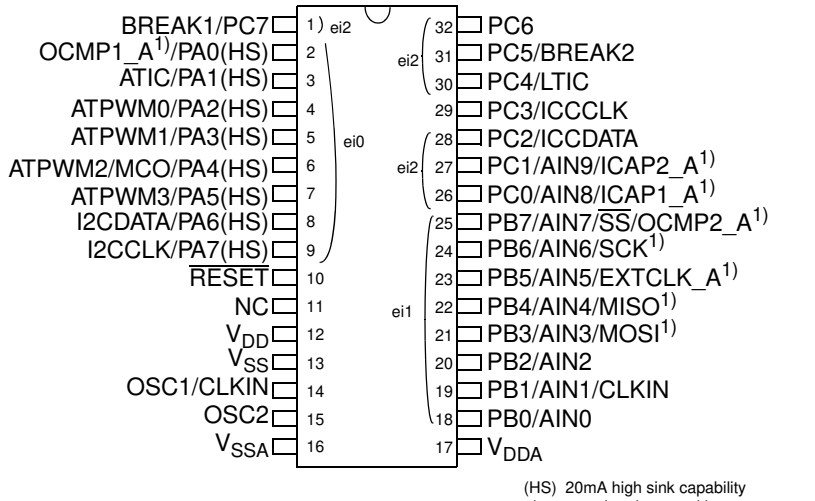
Figure 1. General block diagram



Note 1 : available on 8K version only

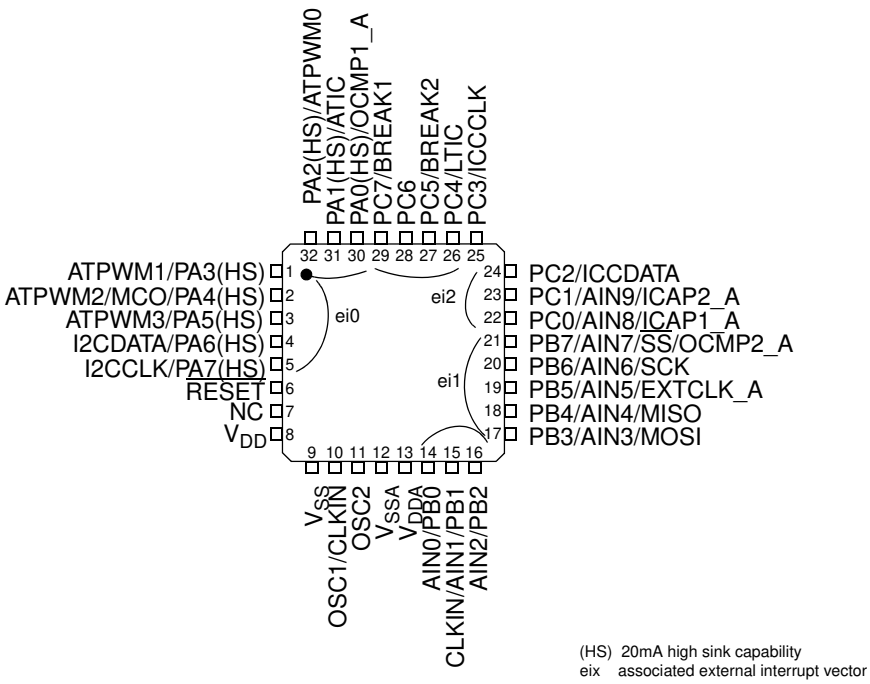
2 Pin description

Figure 2. 32-pin SDIP package pinout



Note 1: Available on 8K version only

Figure 3. 32-pin LQFP 7x7 package pinout



Legend / Abbreviations for *Table 2*:

Type: I = input, O = output, S = supply

In/Output level: C_T = CMOS $0.3V_{DD}/0.7V_{DD}$ with input trigger

Output level: HS = 20 mA high sink (on N-buffer only)

Port and control configuration:

- Input: float = floating, wpu = weak pull-up, int = interrupt, ana = analog
- Output: OD = open drain, PP = push-pull

The RESET configuration of each pin is shown in bold which is valid as long as the device is in reset state.

Table 2. Device pin description (32-pin packages)

Pin number		Pin name	Type	Level		Port/control						Main function (after reset)	Alternate function
						Input				Output			
LQFP32	SDIP32			Input	Output	float	wpu	int	ana	OD[1]	PP		
1	5	PA3(HS)/ATPWM1	I/O	C_T	HS	**x**	ei0			x	x	**Port A3 (HS)**	ATPWM1
2	6	PA4(HS)/ ATPWM2/MCO	I/O	C_T	HS	**x**				x	x	**Port A4 (HS)**	ATPWM2/ MCO
3	7	PA5 (HS)ATPWM3	I/O	C_T	HS	**x**				x	x	**Port A5 (HS)**	ATPWM3
4	8	PA6(HS)/ I2CDATA/SCK[2]	I/O	C_T	HS	**x**		ei0		T		**Port A6 (HS)**	I2CDATA/SPI serial clock
5	9	PA7(HS)/I2CCLK/$\overline{SS}$ [2]	I/O	C_T	HS	**x**				T		**Port A7 (HS)**	I2CCLK/SPI slave select (active low)
6	10	RESET					**x**			x		Reset	
8	12	V_{DD}[3]	S									Digital Supply Voltage	
9	13	V_{SS}[3]	S									Digital Ground Voltage	
10	14	OSC1/CLKIN	I									Resonator oscillator inverter input or External clock input	
11	15	OSC2	O									Resonator oscillator output	
12	16	V_{SSA}[3]	S									Analog Ground Voltage	
13	17	V_{DDA}[3]	S									Analog Supply Voltage	

Table 2. Device pin description (32-pin packages) (continued)

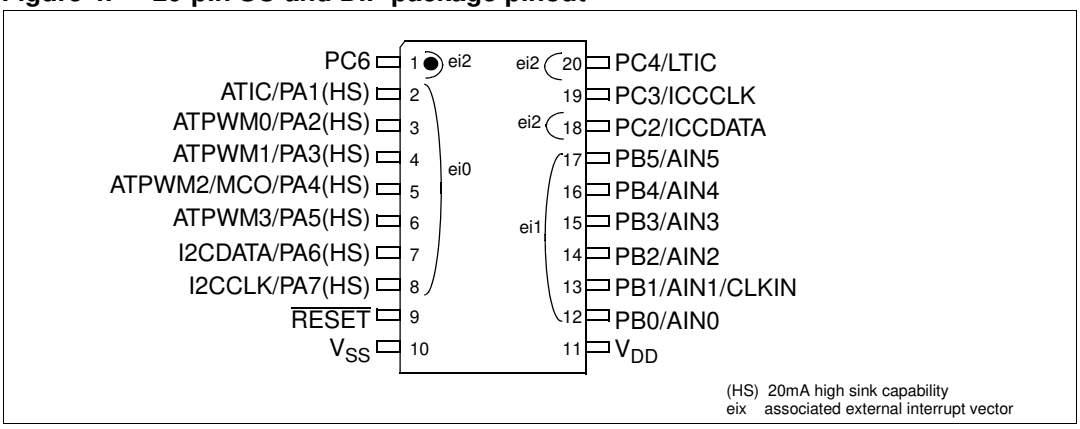
Pin number		Pin name	Type	Level		Port/control						Main function (after reset)	Alternate function
						Input				Output			
LQFP32	SDIP32			Input	Output	float	wpu	int	ana	OD[1]	PP		
14	18	PB0/AIN0	I/O	C_T		**x**	ei1		x	x	x	**Port B0**	AIN0
15	19	PB1/AIN1/CLKIN	I/O	C_T		**x**			x	x	x	**Port B1**	AIN1/External clock source
16	20	PB2/AIN2	I/O	C_T		**x**			x	x	x	**Port B2**	AIN2
17	21	PB3/AIN3/MOSI[2]	I/O	C_T		**x**			x	x	x	**Port B3**	AIN3/SPI Master out /Slave in data
18	22	PB4/AIN4/MISO[2]	I/O	C_T		**x**			x	x	x	**Port B4**	AIN4/SPI Master in/Slave out data
19	23	PB5/AIN5/ EXTCLK_A[2]	I/O	C_T		**x**			x	x	x	**Port B5**	AIN5/Timer A input clock
20	24	PB6/AIN6/SCK[2]	I/O	C_T		**x**			x	x	x	**Port B6**	AIN6/SPI serial clock
21	25	PB7/AIN7/$\overline{SS}$[2]/ OCMP2_A[2]	I/O	C_T		**x**			x	x	x	**Port B7**	AIN7/SPI slave select (active low)/ Timer A Output Compare 2
22	26	PC0/AIN8/ ICAP1_A[2]	I/O	C_T		**x**	ei2		x	x	x	**Port C0**	AIN8/Timer A Input Capture 1
23	27	PC1/AIN9/ ICAP2_A[2]	I/O	C_T		**x**			x	x	x	**Port C1**	AIN9/Timer A Input Capture 2
24	28	PC2/ICCDATA	I/O	C_T		**x**				x	x	**Port C2**	ICCDATA
25	29	PC3/ICCCLK	I/O	C_T		x	**x**			x	x	**Port C3**	ICCCLK
26	30	PC4/LTIC	I/O	C_T		**x**	ei2			x	x	**Port C4**	LTIC
27	31	PC5/BREAK2[4]	I/O	C_T		**x**				x	x	**Port C5**	BREAK2
28	32	PC6	I/O	C_T		**x**				x	x	**Port C6**	
29	1	PC7/BREAK1	I/O	C_T		**x**				x	x	**Port C7**	BREAK1

Table 2. Device pin description (32-pin packages) (continued)

Pin number		Pin name	Type	Level		Port/control						Main function (after reset)	Alternate function
						Input				Output			
LQFP32	SDIP32			Input	Output	float	wpu	int	ana	OD[1]	PP		
30	2	PA0 (HS)[5]/OCMP1_A[2]	I/O	C_T	HS [5]	**x**	ei0			x	x	**Port A0** (HS)[5]/ Timer A Output Compare 1	
31	3	PA1 (HS)/ATIC	I/O	C_T	HS	**x**				x	x	**Port A1 (HS)**	ATIC
32	4	PA2 (HS)/ATPWM0	I/O	C_T	HS	**x**				x	x	**Port A2 (HS)**	ATPWM0

1. In the open-drain output column, T defines a true open-drain I/O (P-Buffer and protection diode to V_{DD} are not implemented).
2. Available on ST7FOXK2 only.
3. It is mandatory to connect all available V_{DD} and V_{DDA} pins to the supply voltage and all V_{SS} and V_{SSA} pins to ground.
4. BREAK2 available on ST7FOXK2 only
5. Available on ST7FOXK1 only.

Figure 4. 20-pin SO and DIP package pinout



Legend / Abbreviations for *Table 3*: Type: I = input, O = output, S = supply

In/Output level:C_T= CMOS $0.3V_{DD}/0.7V_{DD}$ with input trigger

Output level: HS = 20mA high sink (on N-buffer only)

Port and control configuration:

- Input: float = floating, wpu = weak pull-up, int = interrupt, ana = analog
- Output: OD = open drain, PP = push-pull

Note: The RESET configuration of each pin is shown in bold which is valid as long as the device is in reset state.

Table 3. Device pin description (20-pin package)

Pin Number	Pin Name	Type	Level		Port / Control						Main function (after reset)	Alternate function
					Input				Output (1)			
			Input	Output	float	wpu	int	ana	OD	PP		
1	PC6	I/O	C_T		x	ei2			x	x	Port C6	
2	PA1 (HS)/ATIC	I/O	C_T	HS	x				x	x	Port A1 (HS)	ATIC
3	PA2 (HS)/ATPWM0	I/O	C_T	HS	x				x	x	Port A2 (HS)	ATPWM0
4	PA3 (HS)/ATPWM1	I/O	C_T	HS	x				x	x	Port A3 (HS)	ATPWM1
5	PA4 (HS)ATPWM2/MCO	I/O	C_T	HS	x	ei0			x	x	Port A4 (HS)	ATPWM2/MCO
6	PA5 (HS)ATPWM3	I/O	C_T	HS	x				x	x	Port A5 (HS)	ATPWM3
7	PA6 (HS)/I2CDATA	I/O	C_T	HS	x				T		Port A6 (HS)	I2CDATA
8	PA7 (HS)/ I2CCLK	I/O	C_T	HS	x				T		Port A7 (HS)	I2CCLK
9	RESET					x			x		Reset	
10	V_{SS} (3)	S									Digital Ground Voltage	
11	V_{DD} (2)	S									Digital Supply Voltage	
12	PB0/AIN0	I/O	C_T		x			x	x	x	Port B0	AIN0
13	PB1/AIN1/CLKIN	I/O	C_T		x			x	x	x	Port B1	AIN1/External clock source
14	PB2/AIN2	I/O	C_T		x	ei1		x	x	x	Port B2	AIN2
15	PB3/AIN3	I/O	C_T		x			x	x	x	Port B3	AIN3
16	PB4/AIN4	I/O	C_T		x			x	x	x	Port B4	AIN4
17	PB5/AIN5	I/O	C_T		x			x	x	x	Port B5	AIN5
18	PC2/ICCDATA	I/O	C_T		x	ei2			x	x	Port C2	ICCDATA
19	PC3/ICCCLK	I/O	C_T		x				x	x	Port C3	ICCCLK
20	PC4/LTIC	I/O	C_T		x	ei2			x	x	Port C4	LTIC

1. In the open-drain output column, T defines a true open-drain I/O (P-Buffer and protection diode to V_{DD} not implemented).
2. It is mandatory to connect all available V_{DD} and V_{DDA} pins to the supply voltage and all V_{SS} and V_{SSA} pins to ground.

3 Register and memory mapping

As shown in *Figure 5*, the MCU is capable of addressing 64 Kbytes of memories and I/O registers.

The available memory locations consist of 128 bytes of register locations, 384 bytes of RAM and 4 to 8 Kbytes of Flash program memory. The RAM space includes up to 128 bytes for the stack from 180h to 1FFh.

The highest address bytes contain the user reset and interrupt vectors.

The Flash memory contains two sectors (see *Figure 5*) mapped in the upper part of the ST7 addressing space so the reset and interrupt vectors are located in Sector 0 (FFE0h-FFFFh).

The size of Flash Sector 0 and other device options are configurable by option bytes (refer to *Section 13.1 on page 211*).

Caution: Memory locations marked as “Reserved” must never be accessed. Accessing a reserved area can have unpredictable effects on the device.

Figure 5. ST7FOXF1/ST7FOXK1/ST7FOXK2 memory map

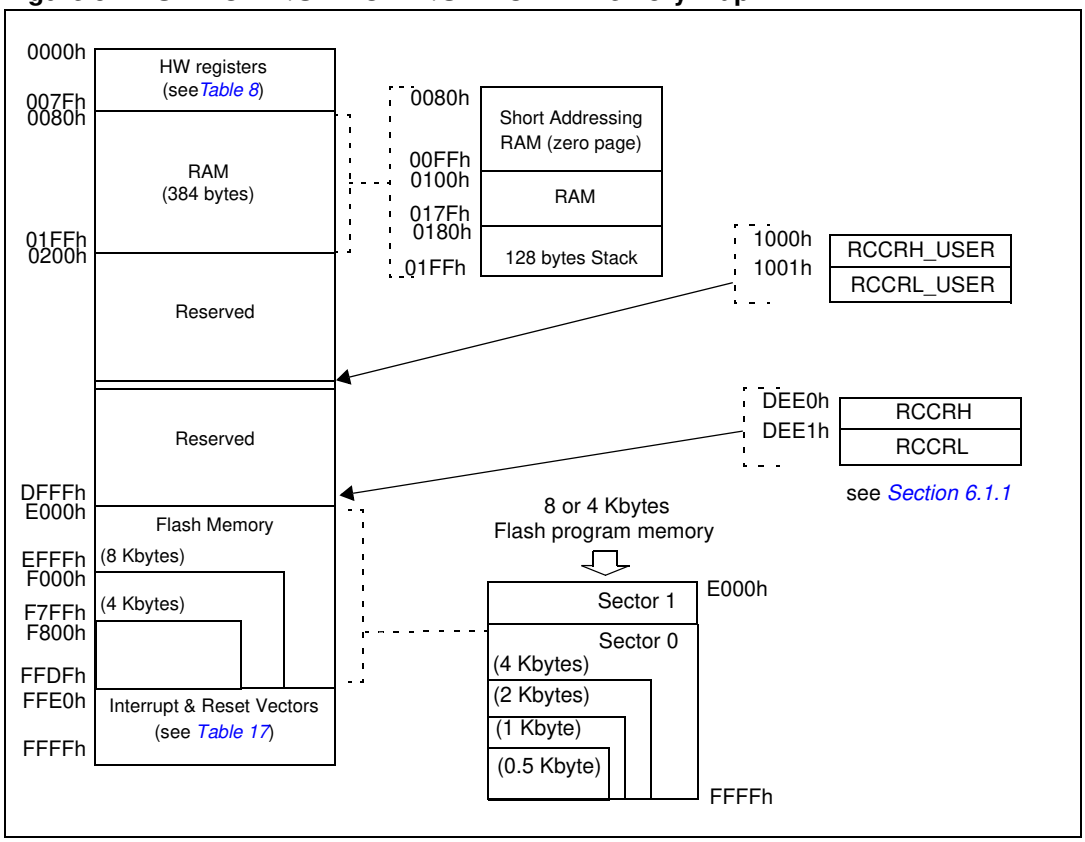


Table 4. Hardware register map(1)

Address	Block	Register label	Register name	Reset status	Remarks
0000h	Port A	PADR	Port A Data register	00h	R/W
0001h		PADDR	Port A Data Direction register	00h	R/W
0002h		PAOR	Port A Option register	00h	R/W
0003h	Port B	PBDR	Port B Data register	00h	R/W
0004h		PBDDR	Port B Data Direction register	00h	R/W
0005h		PBOR	Port B Option register	00h	R/W
0006h	Port C	PCDR	Port C Data register	00h	R/W
0007h		PCDDR	Port C Data Direction register	00h	R/W
0008h		PCOR	Port C Option register	08h	R/W
0009h to 000Bh	Reserved area (3 bytes)				
000Ch	LITE TIMER	LTCSR2	Lite Timer Control/Status register 2	0Fh	R/W
000Dh		LTARR	Lite Timer Auto-reload register	00h	R/W
000Eh		LTCNTR	Lite Timer Counter register	00h	Read Only
000Fh		LTCSR1	Lite Timer Control/Status register 1	0x00 0000b	R/W
0010h		LTICR	Lite Timer Input Capture register	xxh	Read Only
0011h	AUTO-RELOAD TIMER	ATCSR	Timer Control/Status register	0x00 0000b	R/W
0012h		CNTR1H	Counter register 1 High	00h	Read Only
0013h		CNTR1L	Counter register 1 Low	00h	Read Only
0014h		ATR1H	Auto-Reload register 1 High	00h	R/W
0015h		ATR1L	Auto-Reload register 1 Low	00h	R/W
0016h		PWMCR	PWM Output Control register	00h	R/W
0017h		PWM0CSR	PWM 0 Control/Status register	00h	R/W
0018h		PWM1CSR	PWM 1 Control/Status register	00h	R/W
0019h		PWM2CSR	PWM 2 Control/Status register	00h	R/W
001Ah		PWM3CSR	PWM 3 Control/Status register	00h	R/W
001Bh		DCR0H	PWM 0 Duty Cycle register High	00h	R/W
001Ch		DCR0L	PWM 0 Duty Cycle register Low	00h	R/W
001Dh		DCR1H	PWM 1 Duty Cycle register High	00h	R/W
001Eh		DCR1L	PWM 1 Duty Cycle register Low	00h	R/W
001Fh		DCR2H	PWM 2 Duty Cycle register High	00h	R/W
0020h		DCR2L	PWM 2 Duty Cycle register Low	00h	R/W
0021h		DCR3H	PWM 3 Duty Cycle register High	00h	R/W
0022h		DCR3L	PWM 3 Duty Cycle register Low	00h	R/W
0023h		ATICRH	Input Capture register High	00h	Read Only
0024h		ATICRL	Input Capture register Low	00h	Read Only
0025h		ATCSR2	Timer Control/Status register 2	03h	R/W
0026h		BREAKCR1	Break Control register	00h	R/W
0027h		ATR2H	Auto-Reload register 2 High	00h	R/W
0028h		ATR2L	Auto-Reload register 2 Low	00h	R/W
0029h		DTGR	Dead Time Generation register	00h	R/W
002Ah		BREAKEN	Break Enable register	03h	R/W
002Bh	Reserved area (1 byte)				
002Ch	AUTO-RELOAD TIMER	BREAKCR2 (4)	Break Control register 2 (4)	00h	R/W

Table 4. Hardware register map(1) (continued)

Address	Block	Register label	Register name	Reset status	Remarks
002Dh	ITC	ISPR0	Interrupt Software Priority register 0	FFh	R/W
002Eh		ISPR1	Interrupt Software Priority register 1	FFh	R/W
002Fh		ISPR2	Interrupt Software Priority register 2	FFh	R/W
0030h		ISPR3	Interrupt Software Priority register 3	FFh	R/W
0031h		EICR	External Interrupt Control register	00h	R/W
0032h	Reserved area (1 byte)				
0033h	WDG	WDGCR	Watchdog Control register	7Fh	R/W
0034h	FLASH	FCSR	Flash Control/Status register	00h	R/W
0035h	RC Calibration	RCC_CSR	RC calibration Control/Status register	00h	R/W
0036h	ADC	ADCCSR	A/D Control Status register	00h	R/W
0037h		ADCDRH	A/D Data register High	xxh	Read Only
0038h		ADCDRL	A/D Data Low / test register	0xh	R/W
0039h	Reserved area (1 byte)				
003Ah	MCC	MCCSR	Main Clock Control/Status register	00h	R/W
003Bh	Clock and Reset	RCCRH	RC oscillator Control register High	FFh	R/W
003Ch		RCCRL	RC oscillator Control register Low	011x 0x00b	R/W
003Dh		PSCR	Prescaler register	00h or 03h(2)	R/W
003Eh to 0047h	Reserved area (10 bytes)				
0048h	AWU	AWUCSR	AWU Control/Status register	FFh	R/W
0049h		AWUPR	AWU Preload register	00h	R/W
004Ah	DM(3)	DMCR	DM Control register	00h	R/W
004Bh		DMSR	DM Status register	00h	R/W
004Ch		DMBK1H	DM Breakpoint register 1 High	00h	R/W
004Dh		DMBK1L	DM Breakpoint register 1 Low	00h	R/W
004Eh		DMBK2H	DM Breakpoint register 2 High	00h	R/W
004Fh		DMBK2L	DM Breakpoint register 2 Low	00h	R/W
0050h		DMCR2	DM Control register 2	00h	R/W
0051h	Clock Controller	CKCNTCSR	Clock Controller Status register	09h	R/W
0052h to 0054h	Reserved area (3 bytes)				

Table 4. Hardware register map(1) (continued)

Address	Block	Register label	Register name	Reset status	Remarks
0055h	16-bit Timer(4)	TACR2	Timer A Control register 2	00h	R/W
0056h		TACR1	Timer A Control register 1	00h	R/W
0057h		TACSR	Timer A Control/status register	00h	Read Only
0058h		TAICHR1	Timer A Input capture 1 high register	xxh	Read Only
0059h		TAICLR1	Timer A Input capture 1 low register	xxh	Read Only
005Ah		TAOCHR1	Timer A Output compare 1 high register	80h	R/W
005Bh		TAOCLR1	Timer A Output compare 1 low register	00h	R/W
005Ch		TACHR	Timer A Output counter high register	FFh	Read Only
005Dh		TACLR	Timer A Output counter low register	FCh	Read Only
005Eh		TAACHR	Timer A Alternate counter high register	FFh	Read Only
005Fh		TAACLR	Timer A Alternate counter low register	FCh	Read Only
0060h		TAICHR2	Timer A Input capture 2 high register	xxh	Read Only
0061h		TAICLR2	Timer A Input capture 2 low register	xxh	Read Only
0062h		TAOCHR2	Timer A Output compare 2 high register	80h	R/W
0063h		TAOCLR2	Timer A Output compare 2 low register	00h	R/W
0064h	I2C	I2CCR	I^2C Control register	00h	R/W
0065h		I2CSR1	I^2C Status register 1	00h	Read only
0066h		I2CSR2	I^2C Status register 2	00h	Read only
0067h		I2CCCR	I^2C Clock Control register	00h	R/W
0068h		I2COAR1	I^2C Own Address register 1	00h	R/W
0069h		I2COAR2	I^2C Own Address register 2	40h	R/W
006Ah		I2CDR	I^2C Data register	00h	R/W
0070h	SPI(4)	SPIDR	SPI Data register	0xh	R/W
0071h		SPICR	SPI Control register	00h	R/W
0072h		SPISR	SPI Status register	xxh	R/W

1. Legend: x=undefined, R/W=read/write.
2. Reset status is 03h for ST7FOXK2 and 00h for ST7FOXF1 and ST7FOXK1
3. For a description of the Debug Module registers, see ICC protocol reference manual.
4. Available on ST7FOXK2 only

4 Flash programmable memory

4.1 Introduction

The ST7 single voltage extended Flash (XFlash) is a non-volatile memory that can be electrically erased and programmed either on a byte-by-byte basis or up to 32 bytes in parallel.

The XFlash devices can be programmed off-board (plugged in a programming tool) or on-board using In-Circuit Programming or In-Application Programming.

The array matrix organization allows each sector to be erased and reprogrammed without affecting other sectors.

4.2 Main features

- ICP (In-Circuit Programming)
- IAP (In-Application Programming)
- ICT (In-Circuit Testing) for downloading and executing user application test patterns in RAM
- Sector 0 size configurable by option byte
- Read-out and write protection

4.3 Programming modes

The ST7 can be programmed in three different ways:

- Insertion in a programming tool. In this mode, Flash sectors 0 and 1, option byte row can be programmed or erased.
- In-Circuit Programming. In this mode, Flash sectors 0 and 1, option byte row can be programmed or erased without removing the device from the application board.
- In-Application Programming. In this mode, sector 1 can be programmed or erased without removing the device from the application board and while the application is running.

4.3.1 In-Circuit Programming (ICP)

ICP uses a protocol called ICC (In-Circuit Communication) which allows an ST7 plugged on a printed circuit board (PCB) to communicate with an external programming device connected via cable. ICP is performed in three steps:

Switch the ST7 to ICC mode (In-Circuit Communications). This is done by driving a specific signal sequence on the ICCCLK/DATA pins while the $\overline{\text{RESET}}$ pin is pulled low. When the ST7 enters ICC mode, it fetches a specific Reset vector which points to the ST7 System Memory containing the ICC protocol routine. This routine enables the ST7 to receive bytes from the ICC interface.

- Download ICP Driver code in RAM from the ICCDATA pin
- Execute ICP Driver code in RAM to program the Flash memory

Depending on the ICP Driver code downloaded in RAM, Flash memory programming can be fully customized (number of bytes to program, program locations, or selection of the serial communication interface for downloading).

4.3.2 In Application Programming (IAP)

This mode uses an IAP Driver program previously programmed in Sector 0 by the user (in ICP mode).

This mode is fully controlled by user software. This allows it to be adapted to the user application, (user-defined strategy for entering programming mode, choice of communications protocol used to fetch the data to be stored etc.)
IAP mode can be used to program any memory areas except Sector 0, which is Write/Erase protected to allow recovery in case errors occur during the programming operation.

4.4 ICC interface

ICP needs a minimum of 4 and up to 6 pins to be connected to the programming tool. These pins are:

- $\overline{\text{RESET}}$: device reset
- V_{SS}: device power supply ground
- ICCCLK: ICC output serial clock pin
- ICCDATA: ICC input serial data pin
- OSC1: main clock input for external source
- V_{DD}: application board power supply (optional, see Note 3)

Note: 1 If the ICCCLK or ICCDATA pins are only used as outputs in the application, no signal isolation is necessary. As soon as the Programming Tool is plugged to the board, even if an ICC session is not in progress, the ICCCLK and ICCDATA pins are not available for the application. If they are used as inputs by the application, isolation such as a serial resistor has to be implemented in case another device forces the signal. Refer to the Programming Tool documentation for recommended resistor values.

2 During the ICP session, the programming tool must control the $\overline{\text{RESET}}$ pin. This can lead to conflicts between the programming tool and the application reset circuit if it drives more than 5mA at high level (push pull output or pull-up resistor<1 kΩ). A schottky diode can be used to isolate the application RESET circuit in this case. When using a classical RC network with R>1 kΩ or a reset management IC with open drain output and pull-up resistor>1 kΩ, no additional components are needed. In all cases the user must ensure that no external reset is generated by the application during the ICC session.

3 The use of pin 7 of the ICC connector depends on the Programming Tool architecture. This pin must be connected when using most ST Programming Tools (it is used to monitor the application power supply). Please refer to the Programming Tool manual.

4 In "enabled option byte" mode (38-pulse ICC mode), the internal RC oscillator is forced as a clock source, regardless of the selection in the option byte. In "disabled option byte" mode (35-pulse ICC mode), pin 9 has to be connected to the PB1/CLKIN pin of the ST7 when the clock is not available in the application or if the selected clock option is not programmed in the option byte.

Caution: During normal operation the ICCCLK pin must be internally or externally pulled- up (external pull-up of 10 kΩ mandatory in noisy environment) to avoid entering ICC mode unexpectedly