



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





# ATtiny204/404

---

## AVR® Microcontroller with Core Independent Peripherals and picoPower® Technology

---

### Introduction

---

The ATtiny204/404 microcontrollers are using the high-performance, low-power AVR® RISC architecture, and are capable of running at up to 20 MHz, with up to 2/4 KB Flash, 128/256 bytes of SRAM, and 64/128 bytes of EEPROM in a 14-pin package. The series uses the latest technologies with a flexible and low-power architecture including Event System and SleepWalking, accurate analog features, and advanced peripherals.

### Features

---

- CPU:
  - AVR® 8-bit CPU
  - Running at up to 20 MHz
  - Single cycle I/O access
  - Two-level interrupt controller
  - Two-cycle hardware multiplier
- Memories:
  - 2/4 KB In-system self-programmable Flash memory
  - 64/128B EEPROM
  - 128/256B SRAM
  - Write/Erase Cycles: 10,000 Flash/100,000 EEPROM
  - Data Retention: 20 Years at 85°C
- System:
  - Power-on Reset (POR)
  - Brown-out Detection (BOD)
  - Clock Options:
    - 16/20 MHz Low-Power Internal RC Oscillator with:
      - ±3% Accuracy over full temperature and voltage range
      - ±2% Drift over limited temperature and 1.8 ... 3.6V voltage range
    - 32.768 kHz Ultra Low-Power (ULP) Internal RC Oscillator with ±10% Accuracy, ±2% Calibration Step Size
    - External Clock Input
  - Single Pin Unified Program Debug Interface (UPDI)
  - Three Sleep Modes:
    - Idle with all peripherals running and mode for immediate wake-up time

- Standby
  - Configurable operation of selected peripherals
  - SleepWalking peripherals
- Power-down with wake-up functionality
- Peripherals:
  - 3-channel Event System
  - One 16-bit Timer/Counter Type A with Dedicated Period Register, Three Compare Channels (TCA)
  - One 16-bit Timer/Counter Type B with Input Capture (TCB)
  - One 16-bit Real-Time Counter (RTC) running from Internal RC Oscillator
  - One USART with fractional Baud Rate Generator, Auto-baud, and Start-of-frame Detection
  - Master/Slave Serial Peripheral Interface (SPI)
  - Master/Slave TWI with Dual Address Match
    - Standard mode (Sm, 100 kHz)
    - Fast mode (Fm, 400 kHz)
    - Fast mode Plus (Fm+, 1 MHz)
  - Configurable Custom Logic (CCL) with Two Programmable Look-up Tables (LUT)
  - Analog Comparator (AC)
  - 10-bit 115 ksps Analog-to-Digital Converter (ADC)
  - Five selectable internal voltage references: 0.55V, 1.1V, 1.5V, 2.5V, and 4.3V
  - Automated CRC memory scan
  - Watchdog Timer (WDT) with Window mode, with separate on-chip oscillator
  - External interrupt on all general purpose pins
- I/O and Packages:
  - 12 Programmable I/O lines
  - 14-pin SOIC150
- Temperature Ranges:
  - -40°C to 105°C
  - -40°C to 125°C Temperature graded device options available
- Speed Grades:
  - 0-5 MHz @ 1.8V – 5.5V
  - 0-10 MHz @ 2.7V – 5.5V
  - 0-20 MHz @ 4.5V – 5.5V

## Table of Contents

---

Introduction.....	1
Features.....	1
1. tinyAVR <sup>®</sup> 0-Series Overview.....	9
1.1. Configuration Summary.....	9
2. Ordering Information.....	11
2.1. ATtiny204.....	11
2.2. ATtiny404.....	11
3. Block Diagram.....	12
4. Pinout.....	13
4.1. 14-Pin SOIC.....	13
5. I/O Multiplexing and Considerations.....	14
5.1. Multiplexed Signals.....	14
6. Memories.....	15
6.1. Overview.....	15
6.2. Memory Map.....	15
6.3. In-System Reprogrammable Flash Program Memory.....	15
6.4. SRAM Data Memory.....	16
6.5. EEPROM Data Memory.....	16
6.6. User Row.....	17
6.7. Signature Bytes.....	17
6.8. Memory Section Access from CPU and UPDI on Locked Device.....	17
6.9. I/O Memory.....	18
6.10. Configuration and User Fuses (FUSE).....	21
7. Peripherals and Architecture.....	39
7.1. Peripheral Module Address Map.....	39
7.2. Interrupt Vector Mapping.....	40
7.3. System Configuration (SYSCFG).....	41
8. AVR CPU.....	44
8.1. Features.....	44
8.2. Overview.....	44
8.3. Architecture.....	44
8.4. Arithmetic Logic Unit (ALU).....	46
8.5. Functional Description.....	47
8.6. Register Summary - CPU.....	52
8.7. Register Description.....	52

9. Nonvolatile Memory Controller (NVMCTRL).....	57
9.1. Features.....	57
9.2. Overview.....	57
9.3. Functional Description.....	58
9.4. Register Summary - NVMCTRL.....	65
9.5. Register Description.....	65
10. Clock Controller (CLKCTRL).....	73
10.1. Features.....	73
10.2. Overview.....	73
10.3. Functional Description.....	75
10.4. Register Summary - CLKCTRL.....	80
10.5. Register Description.....	80
11. Sleep Controller (SLPCTRL).....	89
11.1. Features.....	89
11.2. Overview.....	89
11.3. Functional Description.....	90
11.4. Register Summary - SLPCTRL.....	93
11.5. Register Description.....	93
12. Reset Controller (RSTCTRL).....	95
12.1. Features.....	95
12.2. Overview.....	95
12.3. Functional Description.....	96
12.4. Register Summary - RSTCTRL.....	99
12.5. Register Description.....	99
13. CPU Interrupt Controller (CPUINT).....	102
13.1. Features.....	102
13.2. Overview.....	102
13.3. Functional Description.....	104
13.4. Register Summary - CPUINT.....	111
13.5. Register Description.....	111
14. Event System (EVSYS).....	116
14.1. Features.....	116
14.2. Overview.....	116
14.3. Functional Description.....	119
14.4. Register Summary - EVSYS.....	121
14.5. Register Description.....	121
15. Port Multiplexer (PORTMUX).....	130
15.1. Overview.....	130
15.2. Register Summary - PORTMUX.....	131
15.3. Register Description.....	131
16. I/O Pin Configuration (PORT).....	135

16.1. Features.....	135
16.2. Overview.....	135
16.3. Functional Description.....	137
16.4. Register Summary - PORT.....	141
16.5. Register Description - Ports.....	141
16.6. Register Summary - VPORT.....	153
16.7. Register Description - Virtual Ports.....	153
<b>17. Brown-Out Detector (BOD).....</b>	<b>158</b>
17.1. Features.....	158
17.2. Overview.....	158
17.3. Functional Description.....	160
17.4. Register Summary - BOD.....	162
17.5. Register Description.....	162
<b>18. Voltage Reference (VREF).....</b>	<b>169</b>
18.1. Features.....	169
18.2. Overview.....	169
18.3. Functional Description.....	169
18.4. Register Summary - VREF.....	171
18.5. Register Description.....	171
<b>19. Watchdog Timer (WDT).....</b>	<b>174</b>
19.1. Features.....	174
19.2. Overview.....	174
19.3. Functional Description.....	176
19.4. Register Summary - WDT.....	180
19.5. Register Description.....	180
<b>20. 16-bit Timer/Counter Type A (TCA).....</b>	<b>184</b>
20.1. Features.....	184
20.2. Overview.....	184
20.3. Functional Description.....	188
20.4. Register Summary - TCA in Normal Mode (CTRLD.SPLITM=0).....	198
20.5. Register Description - Normal Mode.....	199
20.6. Register Summary - TCA in Split Mode (CTRLD.SPLITM=1).....	219
20.7. Register Description - Split Mode.....	219
<b>21. 16-bit Timer/Counter Type B (TCB).....</b>	<b>235</b>
21.1. Features.....	235
21.2. Overview.....	235
21.3. Functional Description.....	238
21.4. Register Summary - TCB.....	246
21.5. Register Description.....	246
<b>22. Real-Time Counter (RTC).....</b>	<b>258</b>
22.1. Features.....	258
22.2. Overview.....	258

22.3. RTC Functional Description.....	260
22.4. PIT Functional Description.....	261
22.5. Events.....	263
22.6. Interrupts.....	264
22.7. Sleep Mode Operation.....	264
22.8. Synchronization.....	265
22.9. Configuration Change Protection.....	265
22.10. Register Summary - RTC.....	266
22.11. Register Description.....	266
<b>23. Universal Synchronous and Asynchronous Receiver and Transmitter (USART)..</b>	<b>282</b>
23.1. Features.....	282
23.2. Overview.....	282
23.3. Functional Description.....	286
23.4. Register Summary - USART.....	301
23.5. Register Description.....	301
<b>24. Serial Peripheral Interface (SPI).....</b>	<b>320</b>
24.1. Features.....	320
24.2. Overview.....	320
24.3. Functional Description.....	323
24.4. Register Summary - SPI.....	331
24.5. Register Description.....	331
<b>25. Two-Wire Interface (TWI).....</b>	<b>340</b>
25.1. Features.....	340
25.2. Overview.....	340
25.3. Functional Description.....	342
25.4. Register Summary - TWI.....	356
25.5. Register Description.....	356
<b>26. Cyclic Redundancy Check Memory Scan (CRCSCAN).....</b>	<b>376</b>
26.1. Features.....	376
26.2. Overview.....	376
26.3. Functional Description.....	378
26.4. Register Summary - CRCSCAN.....	381
26.5. Register Description.....	381
<b>27. Configurable Custom Logic (CCL).....</b>	<b>385</b>
27.1. Features.....	385
27.2. Overview.....	385
27.3. Functional Description.....	387
27.4. Register Summary - CCL.....	396
27.5. Register Description.....	396
<b>28. Analog Comparator (AC).....</b>	<b>403</b>
28.1. Features.....	403
28.2. Overview.....	403

28.3. Functional Description.....	405
28.4. Register Summary - AC.....	407
28.5. Register Description.....	407
<b>29. Analog-to-Digital Converter (ADC).....</b>	<b>412</b>
29.1. Features.....	412
29.2. Overview.....	412
29.3. Functional Description.....	416
29.4. Register Summary - ADCn.....	424
29.5. Register Description.....	424
<b>30. Unified Program and Debug Interface (UPDI).....</b>	<b>442</b>
30.1. Features.....	442
30.2. Overview.....	442
30.3. Functional Description.....	445
30.4. Register Summary - UPDI.....	465
30.5. Register Description.....	465
<b>31. Electrical Characteristics.....</b>	<b>476</b>
31.1. Disclaimer.....	476
31.2. Absolute Maximum Ratings .....	476
31.3. General Operating Ratings .....	477
31.4. Power Consumption for ATtiny204/ATtiny404.....	478
31.5. Wake-Up Time.....	479
31.6. Power Consumption of Peripherals.....	480
31.7. BOD and POR Characteristics.....	481
31.8. External Reset Characteristics.....	481
31.9. Oscillators and Clocks.....	482
31.10. I/O Pin Characteristics.....	483
31.11. USART.....	484
31.12. SPI.....	485
31.13. TWI.....	486
31.14. VREF.....	488
31.15. ADC.....	490
31.16. AC.....	492
31.17. UPDI Timing.....	493
31.18. Programming Time.....	493
<b>32. Typical Characteristics.....</b>	<b>494</b>
32.1. Power Consumption.....	494
32.2. GPIO.....	501
32.3. VREF Characteristics.....	509
32.4. BOD Characteristics.....	511
32.5. ADC Characteristics.....	514
32.6. AC Characteristics.....	519
32.7. OSC20M Characteristics.....	522
32.8. OSCULP32K Characteristics.....	524



---

---

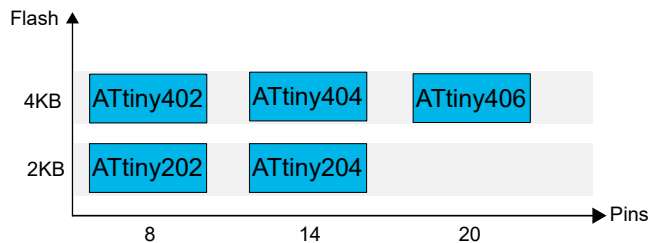
33. Errata.....	525
33.1. Errata - ATtiny204/ATtiny404 .....	525
34. Package Drawings.....	527
34.1. 14-Pin SOIC150.....	527
35. Thermal Considerations.....	528
35.1. Thermal Resistance Data.....	528
35.2. Junction Temperature.....	528
36. Instruction Set Summary.....	529
37. Conventions.....	534
37.1. Numerical Notation.....	534
37.2. Memory Size and Type.....	534
37.3. Frequency and Time.....	534
37.4. Registers and Bits.....	535
38. Acronyms and Abbreviations.....	536
39. Data Sheet Revision History.....	539
39.1. Revision History.....	539
The Microchip Web Site.....	540
Customer Change Notification Service.....	540
Customer Support.....	540
Microchip Devices Code Protection Feature.....	540
Legal Notice.....	541
Trademarks.....	541
Quality Management System Certified by DNV.....	542
Worldwide Sales and Service.....	543

## 1. tinyAVR® 0-Series Overview

The figure below shows the tinyAVR 0-series, laying out pin count variants and memory sizes:

- Vertical migration can be done upwards without code modification since these devices are pin compatible and provide the same or additional features. Downward migration may require code modification due to fewer available instances of some peripherals.
- Horizontal migration to the left reduces the pin count and therefore, the available features.

**Figure 1-1. Device Family Overview**

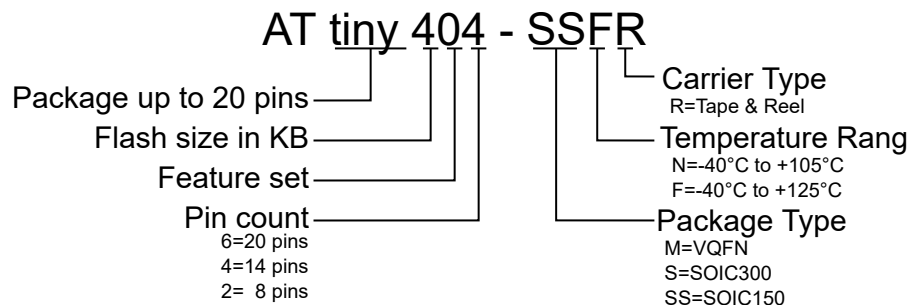


The fully compatible variants of the ATtiny devices, that is the vertical migration option shown in the figure above, come with both smaller and larger Flash memories.

Devices with different Flash memory size typically also have different SRAM and EEPROM.

The name of a device of the ATtiny family contains information as depicted below (not all options are available):

**Figure 1-2. Device Designations**



### 1.1 Configuration Summary

#### 1.1.1 Peripheral Summary

**Table 1-1. Peripheral Summary**

	ATtiny204	ATtiny404
Pins	14	14
SRAM	128B	256B
Flash	2 KB	4 KB

# ATtiny204/404

## tinyAVR® 0-Series Overview

	ATtiny204	ATtiny404
EEPROM	64B	128B
Max. frequency (MHz)	20	20
16-bit Timer/Counter type A (TCA)	1	1
16-bit Timer/Counter type B (TCB)	1	1
12-bit Timer/Counter type D (TCD)	No	No
Real-Time Counter (RTC)	1	1
USART	1	1
SPI	1	1
TWI (I <sup>2</sup> C)	1	1
ADC	1	1
ADC channels	10	10
DAC	No	No
AC	1	1
AC inputs	1p/1n	1p/1n
Peripheral Touch Controller (PTC)	No	No
Custom Logic	1	1
Window Watchdog	1	1
Event System channels	3	3
General purpose I/O	12	12
External interrupts	12	12
CRCSCAN	1	1

## 2. Ordering Information

### 2.1 ATtiny204

**Table 2-1. ATtiny204 Ordering Codes**

Ordering Code <sup>(1)</sup>	Flash	Package Type (GPC)	Leads	Power Supply	Operational Range	Carrier Type
ATtiny204-SSNR	2 KB	SOIC150 (SVQ)	14	1.8V - 5.5V	Industrial (-40°C +105°C)	Tape & Reel
ATtiny204-SSFR	2 KB	SOIC150 (SVQ)	14	1.8V - 5.5V	Industrial (-40°C +125°C)	Tape & Reel

1. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

### 2.2 ATtiny404

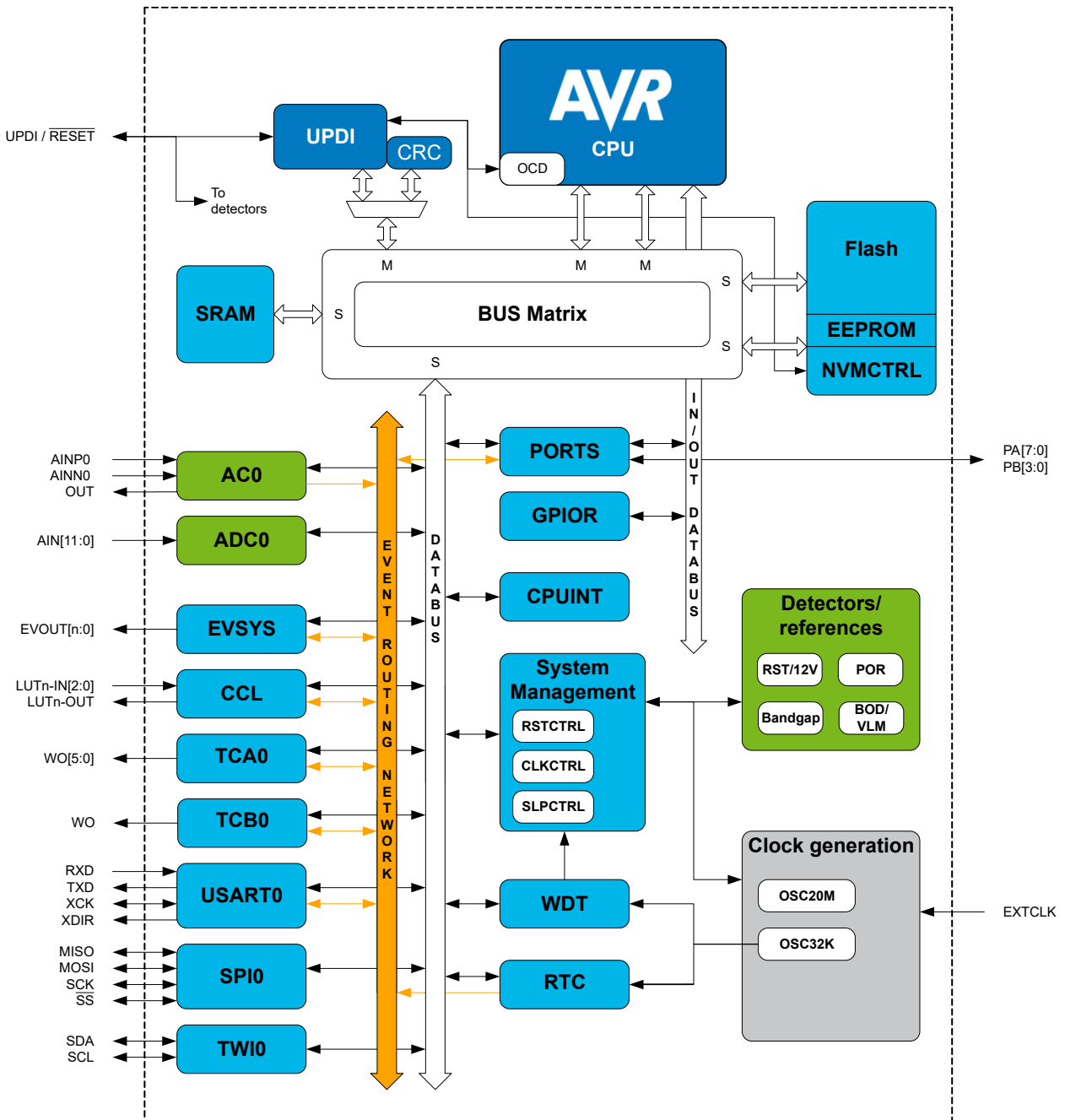
**Table 2-2. ATtiny404 Ordering Codes**

Ordering Code <sup>(1)</sup>	Flash	Package Type (GPC)	Leads	Power Supply	Operational Range	Carrier Type
ATtiny404-SSNR	4 KB	SOIC150 (SVQ)	14	1.8V - 5.5V	Industrial (-40°C +105°C)	Tape & Reel
ATtiny404-SSFR	4 KB	SOIC150 (SVQ)	14	1.8V - 5.5V	Industrial (-40°C +125°C)	Tape & Reel

1. Pb-free packaging complies with the European Directive for Restriction of Hazardous Substances (RoHS directive). They are also Halide free and fully Green.

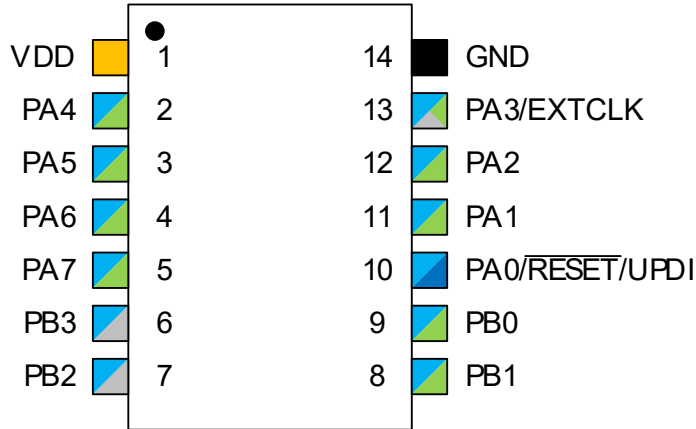
### 3. Block Diagram








Figure 3-1. Block Diagram



### 4. Pinout

#### 4.1 14-Pin SOIC



-  Input supply
-  Ground
-  GPIO VDD power domain
-  Programming, Debug, Reset
-  Clock
-  Digital function only
-  Analog function

## 5. I/O Multiplexing and Considerations

### 5.1 Multiplexed Signals

**Table 5-1. PORT Function Multiplexing**

SOC 14-pin	Pin Name (1,2)	Other/Special	ADC0	AC0	USART0	SPI0	TWI0	TCA0	TCB0	CCL
10	PA0	RESET/UPDI	AIN0							LUT0-IN0
11	PA1		AIN1		TXD	MOSI	SDA			LUT0-IN1
12	PA2	EVOUT0	AIN2		RxD	MISO	SCL			LUT0-IN2
13	PA3	EXTCLK	AIN3		XCK	SCK		WO3		
14	GND									
1	VDD									
2	PA4		AIN4		XDIR	SS		WO4		LUT0-OUT
3	PA5		AIN5	OUT				WO5	WO	
4	PA6		AIN6	AINN0		MOSI				
5	PA7		AIN7	AINP0		MISO				LUT1-OUT
6	PB3				RxD			WO0		
7	PB2	EVOUT1			TxD			WO2		
8	PB1		AIN10		XCK		SDA	WO1		
9	PB0		AIN11		XDIR		SCL	WO0		

**Note:**

1. Pin names are of type Pxn, with x being the PORT instance (A, B) and n the pin number. Notation for signals is PORTx\_PINn. All pins can be used as event input.
2. All pins can be used for external interrupt, where pins Px2 and Px6 of each port have full asynchronous detection.



**Tip:** Signals on alternative pin locations are in *typewriter font*. See PORTMUX chapter for selecting the alternative pin locations.

## 6. Memories

### 6.1 Overview

The main memories are SRAM data memory, EEPROM data memory, and Flash program memory. In addition, the peripheral registers are located in the I/O memory space.

**Table 6-1. Physical Properties of Flash Memory**

Property	ATtiny204	ATtiny404
Size	2 KB	4 KB
Page size	64B	64B
Number of pages	32	64
Start address	0x8000	0x8000

**Table 6-2. Physical Properties of SRAM**

Property	ATtiny204	ATtiny404
Size	128B	256B
Start address	0x3F80	0x3F00

**Table 6-3. Physical Properties of EEPROM**

Property	ATtiny204	ATtiny404
Size	64B	128B
Page size	32B	32B
Number of pages	2	4
Start address	0x1400	0x1400

#### Related Links

[I/O Memory](#)

### 6.2 Memory Map

### 6.3 In-System Reprogrammable Flash Program Memory

The ATtiny204/404 contains 4/2 KB on-chip in-system reprogrammable Flash memory for program storage. Since all AVR instructions are 16 or 32 bits wide, the Flash is organized as 4K x 16. For write protection, the Flash program memory space can be divided into three sections (see the illustration below): Bootloader section, application code section, and application data section, with restricted access rights among them.

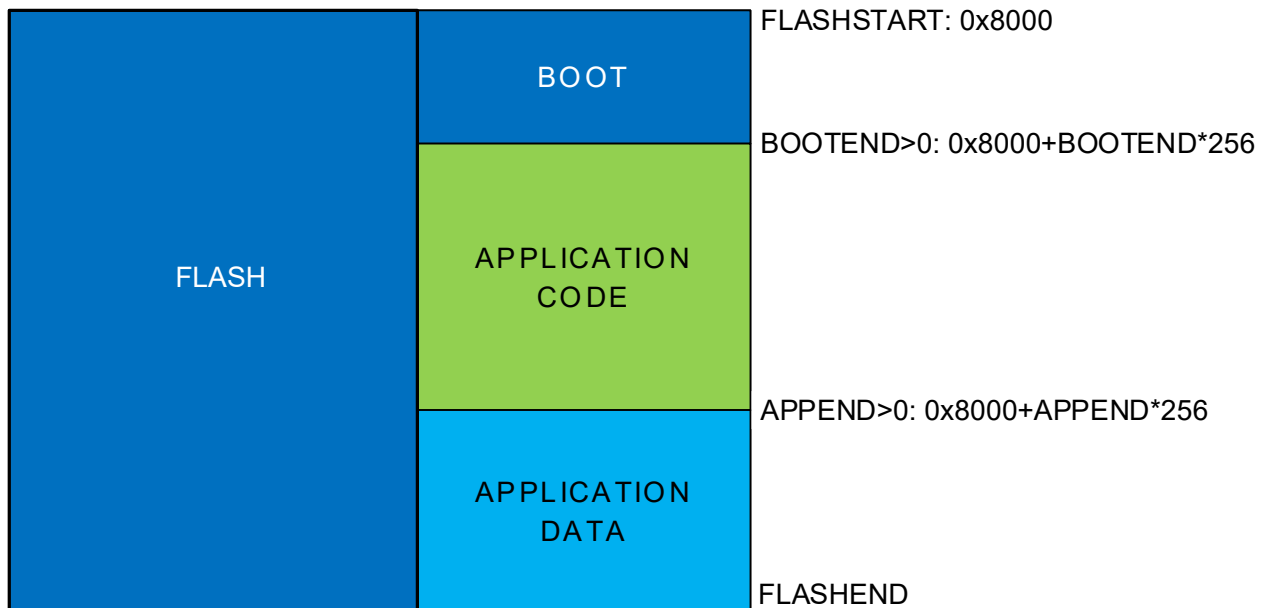


The Program Counter (PC) is 11-bits wide to address the whole program memory. The procedure for writing Flash memory is described in detail in the documentation of the Nonvolatile Memory Controller (NVMCTRL) peripheral.

The entire Flash memory is mapped in the memory space and is accessible with normal LD/ST instructions as well as the LPM instruction. For LD/ST instructions, the Flash is mapped from address 0x8000. For the LPM instruction, the Flash start address is 0x0000.

The ATtiny204/404 also has a CRC peripheral that is a master on the bus.

**Figure 6-1. Flash and the Three Sections**



**Related Links**

- [Configuration Summary](#)
- [Nonvolatile Memory Controller \(NVMCTRL\)](#)

### 6.4 SRAM Data Memory

The 128B/256B SRAM is used for data storage and stack.

**Related Links**

- [AVR CPU](#)
- [Stack and Stack Pointer](#)

### 6.5 EEPROM Data Memory

The ATtiny204/404 has 64/128 bytes of EEPROM data memory, see Memory Map section. The EEPROM memory supports single byte read and write. The EEPROM is controlled by the Nonvolatile Memory Controller (NVMCTRL).

**Related Links**

- [Memory Map](#)
- [Nonvolatile Memory Controller \(NVMCTRL\)](#)

### 6.6 User Row

In addition to the EEPROM, the ATtiny204/404 has one extra page of EEPROM memory that can be used for firmware settings, the User Row (USERROW). This memory supports single byte read and write as the normal EEPROM. The CPU can write and read this memory as normal EEPROM and the UPDI can write and read it as a normal EEPROM memory if the part is unlocked. The User Row can be written by the UPDI when the part is locked. USERROW is not affected by a chip erase.

#### Related Links

[Memory Map](#)

[Nonvolatile Memory Controller \(NVMCTRL\)](#)

[Unified Program and Debug Interface \(UPDI\)](#)

### 6.7 Signature Bytes

All ATtiny microcontrollers have a 3-byte signature code that identifies the device. The three bytes reside in a separate address space. For the device, the signature bytes are given in the following table.

**Note:** When the device is locked, only the System Information Block (SIB) can be obtained.

**Table 6-4. Device ID**

Device Name	Signature Bytes Address		
	0x00	0x01	0x02
ATtiny204	0x1E	0x91	0x22
ATtiny404	0x1E	0x92	0x26

#### Related Links

[System Information Block](#)

### 6.8 Memory Section Access from CPU and UPDI on Locked Device

The device can be locked so that the memories cannot be read using the UPDI. The locking protects both the Flash (all BOOT, APPCODE, and APPDATA sections), SRAM, and the EEPROM including the FUSE data. This prevents successful reading of application data or code using the debugger interface. Regular memory access from within the application still is enabled.

The device is locked by writing any non-valid value to the LOCKBIT bit field in FUSE.LOCKBIT.

**Table 6-5. Memory Access in Unlocked Mode (FUSE.LOCKBIT Valid)<sup>(1)</sup>**

Memory Section	CPU Access		UPDI Access	
	Read	Write	Read	Write
SRAM	Yes	Yes	Yes	Yes
Registers	Yes	Yes	Yes	Yes
Flash	Yes	Yes	Yes	Yes
EEPROM	Yes	Yes	Yes	Yes

Memory Section	CPU Access		UPDI Access	
	Read	Write	Read	Write
USERROW	Yes	Yes	Yes	Yes
SIGROW	Yes	No	Yes	No
Other Fuses	Yes	No	Yes	Yes

**Table 6-6. Memory Access in Locked Mode (FUSE.LOCKBIT Invalid)<sup>(1)</sup>**

Memory Section	CPU Access		UPDI Access	
	Read	Write	Read	Write
SRAM	Yes	Yes	No	No
Registers	Yes	Yes	No	No
Flash	Yes	Yes	No	No
EEPROM	Yes	No	No	No
USERROW	Yes	Yes	No	Yes <sup>(2)</sup>
SIGROW	Yes	No	No	No
Other Fuses	Yes	No	No	No

**Note:**

1. Read operations marked No in the tables may appear to be successful, but the data is corrupt. Hence, any attempt of code validation through the UPDI will fail on these memory sections.
2. In Locked mode, the USERROW can be written blindly using the fuse Write command, but the current USERROW values cannot be read out.



**Important:** The only way to unlock a device is a CHIPERASE, which will erase all device memories to factory default so that no application data is retained.

**Related Links**

[Fuse Summary - FUSE](#)

[LOCKBIT](#)

[Unified Program and Debug Interface \(UPDI\)](#)

[Enabling of KEY Protected Interfaces](#)

## 6.9 I/O Memory

All ATtiny204/404 I/Os and peripherals are located in the I/O memory space. The I/O address range from 0x00 to 0x3F can be accessed in a single cycle using IN and OUT instructions. The extended I/O memory space from 0x0040 - 0x0FFF can be accessed by the LD/LDS/LDD and ST/STS/STD instructions, transferring data between the 32 general purpose working registers and the I/O memory space.

I/O registers within the address range 0x00 - 0x1F are directly bit accessible using the `SBI` and `CBI` instructions. In these registers, the value of single bits can be checked by using the `SBIS` and `SBIC` instructions. Refer to the Instruction Set section for more details.

For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.

Some of the interrupt flags are cleared by writing a '1' to them. On ATtiny204/404 devices, the `CBI` and `SBI` instructions will only operate on the specified bit and can be used on registers containing such interrupt flags. The `CBI` and `SBI` instructions work with registers 0x00 - 0x1F only.

### General Purpose I/O Registers

The ATtiny204/404 devices provide four general purpose I/O registers. These registers can be used for storing any information, and they are particularly useful for storing global variables and interrupt flags. general purpose I/O registers, which reside in the address range 0x1C - 0x1F, are directly bit accessible using the `SBI`, `CBI`, `SBIS`, and `SBIC` instructions.

### Related Links

[Memory Map](#)

[Peripheral Module Address Map](#)

[Instruction Set Summary](#)

---

---

**6.9.1 Register Summary - GPIOR**

Offset	Name	Bit Pos.								
0x00	<a href="#">GPIOR0</a>	7:0								GPIOR[7:0]
0x01	<a href="#">GPIOR1</a>	7:0								GPIOR[7:0]
0x02	<a href="#">GPIOR2</a>	7:0								GPIOR[7:0]
0x03	<a href="#">GPIOR3</a>	7:0								GPIOR[7:0]

**6.9.2 Register Description - GPIOR**

### 6.9.2.1 General Purpose I/O Register n

**Name:** GPIOR  
**Offset:** 0x00 + n\*0x01 [n=0..3]  
**Reset:** 0x00  
**Property:** -

These are general purpose registers that can be used to store data, such as global variables and flags, in the bit accessible I/O memory space.

Bit	7	6	5	4	3	2	1	0
	GPIOR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bits 7:0 – GPIOR[7:0]** GPIO Register byte

## 6.10 Configuration and User Fuses (FUSE)

Fuses are part of the nonvolatile memory and hold factory calibration data and device configuration. The fuses are available from device power-up. The fuses can be read by the CPU or the UPDI, but can only be programmed or cleared by the UPDI. The configuration and calibration values stored in the fuses are written to their respective target registers at the end of the start-up sequence.

The content of the Signature Row fuses (SIGROW) is pre-programmed and cannot be altered. SIGROW holds information such as device ID, serial number, and calibration values.

The fuses for peripheral configuration (FUSE) are pre-programmed but can be altered by the user. Altered values in the configuration fuse will be effective only after a Reset.

**Note:** When writing the fuses write all reserved bits to '1'.

This device provides a User Row fuse area (USERROW) that can hold application data. The USERROW can be programmed on a locked device by the UPDI. This can be used for final configuration without having programming or debugging capabilities enabled.

### Related Links

[Signature Row Description](#)

[Fuse Description](#)

### 6.10.1 SIGROW - Signature Row Summary

Offset	Name	Bit Pos.								
0x00	DEVICEID0	7:0								DEVICEID[7:0]
0x01	DEVICEID1	7:0								DEVICEID[7:0]
0x02	DEVICEID2	7:0								DEVICEID[7:0]
0x03	SERNUM0	7:0								SERNUM[7:0]
0x04	SERNUM1	7:0								SERNUM[7:0]
0x05	SERNUM2	7:0								SERNUM[7:0]
0x06	SERNUM3	7:0								SERNUM[7:0]
0x07	SERNUM4	7:0								SERNUM[7:0]
0x08	SERNUM5	7:0								SERNUM[7:0]
0x09	SERNUM6	7:0								SERNUM[7:0]
0x0A	SERNUM7	7:0								SERNUM[7:0]
0x0B	SERNUM8	7:0								SERNUM[7:0]
0x0C	SERNUM9	7:0								SERNUM[7:0]
0x0D	Reserved									
...										
0x21										
0x22	OSC16ERR3V	7:0								OSC16ERR3V[7:0]
0x23	OSC16ERR5V	7:0								OSC16ERR5V[7:0]
0x24	OSC20ERR3V	7:0								OSC20ERR3V[7:0]
0x25	OSC20ERR5V	7:0								OSC20ERR5V[7:0]

### 6.10.2 Signature Row Description

### 6.10.2.1 Device ID n

**Name:** DEVICEIDn  
**Offset:** 0x00 + n\*0x01 [n=0..2]  
**Reset:** [Device ID]  
**Property:** -

Each device has a device ID identifying the device and its properties; such as memory sizes, pin count, and die revision. This can be used to identify a device and hence, the available features by software. The Device ID consists of three bytes: SIGROW.DEVICEID[2:0].

Bit	7	6	5	4	3	2	1	0
	DEVICEID[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

**Bits 7:0 – DEVICEID[7:0]** Byte n of the Device ID



### 6.10.2.2 Serial Number Byte n

**Name:** SERNUMn  
**Offset:** 0x03 + n\*0x01 [n=0..9]  
**Reset:** [device serial number]  
**Property:** -

Each device has an individual serial number, representing a unique ID. This can be used to identify a specific device in the field. The serial number consists of ten bytes: SIGROW.SERNUM[9:0].

Bit	7	6	5	4	3	2	1	0
	SERNUM[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

**Bits 7:0 – SERNUM[7:0]** Serial Number Byte n

### 6.10.2.3 OSC16 Error at 3V

**Name:** OSC16ERR3V  
**Offset:** 0x22  
**Reset:** [Oscillator frequency error value]  
**Property:** -

Bit	7	6	5	4	3	2	1	0
	OSC16ERR3V[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

**Bits 7:0 – OSC16ERR3V[7:0]** OSC16 Error at 3V

These registers contain the signed oscillator frequency error value when running at internal 16 MHz at 3V, as measured during production.