Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

ATWILC1000-MR110xB

IEEE 802.11 b/g/n Link Controller Module

Description

The ATWILC1000-MR110xB module is a low-power consumption IEEE 802.11 b/g/n IoT (Internet of Things) module, which is specifically optimized for low power IoT applications. This module features small form factor (21.7mm x 14.7mm x 2.1mm) while fully integrating Power Amplifier (PA), Low Noise Amplifier (LNA), Transmit/Receive (T/R), switch, power management, and PCB antenna. With advanced security, it is interoperable with various vendors using IEEE 802.11b/g/n Access Points in wireless LAN. The module provides Serial Peripheral Interface (SPI) and Secure Digital Input Output (SDIO) to interface with the host controller.

Note that all references to the ATWILC1000-MR110xB module include all the module devices listed below unless otherwise noted:

- ATWILC1000-MR110PB
- ATWILC1000-MR110UB

Features

- Compliant with IEEE 802.11 b/g/n 20 MHz (1x1) solution
- Supports Single spatial stream in 2.4 GHz ISM band
- Integrated Power Amplifier (PA) and Transmit/Receive (T/R) switch
- Superior sensitivity and range through advanced PHY signal processing
- Advanced equalization and channel estimation
- Advanced carrier and timing synchronization
- Wi-Fi Direct® and Soft-AP support
- Supports IEEE 802.11 WEP, WPA, WPA2 and WPA2-Enterprise security
- Superior Medium Access Control (MAC) throughput through hardware accelerated two-level A-MSDU/A-MPDU frame aggregation and block acknowledgement
- On-chip memory management engine to reduce the host load
- SPI and SDIO host interfaces
- Operating temperature ranges from -40°C to +85°C
- Input/Output operating voltage of 1.8V to 3.6V
- Built-in 26 MHz crystal
- Power-save modes:
  - <1µA Power-Down mode typical at 3.3V I/O
  - 380µA Doze mode with chip settings preserved (used for beacon monitoring)
  - On-chip low power Sleep oscillator
  - Fast host wake-up from Doze mode by a pin or the host I/O transaction
- Wi-Fi Alliance® certified for connectivity and optimizations

– ID: WFA65340

Table of Contents

Description....1

Features.... 1

1. Ordering Information and Module Marking.... 5

2. Block Diagram.... 6

3. Pinout and Package Information.... 7

4. Electrical Specifications.... 11

   4.1. Absolute Ratings.... 11
   4.2. Recommended Operating Conditions.... 11
   4.3. Receiver Performance.... 11
   4.4. Transmitter Performance.... 13
   4.5. Timing Characteristics.... 14

5. Power Management.... 19

   5.1. Current Consumption in Various Device States.... 19
   5.2. Restrictions for Power States.... 20
   5.3. Power-Up/Down Sequence.... 20
   5.4. Digital I/O Pin Behavior During Power-Up Sequences.... 21

6. CPU and Memory Subsystems.... 23

   6.1. Processor.... 23
   6.2. Memory Subsystem.... 23
   6.3. Nonvolatile Memory (eFuse).... 23

7. WLAN Subsystem.... 25

   7.1. MAC.... 25
   7.2. PHY.... 26
   7.3. Radio.... 27

8. External Interfaces.... 28

   8.1. Interfacing with the Host Microcontroller.... 28
   8.2. SPI Slave Interface.... 29
   8.3. SDIO Slave Interface.... 29
   8.4. UART Debug Interface.... 30
   8.5. I^2C Slave Interface.... 31

9. Notes on Interfacing with the ATWILC1000-MR110xB.... 32

10. Application Reference Design.... 33

11. Module Outline Drawings.... 35

12. Design Consideration.... 38

12.1. ATWILC1000-MR110PB Placement and Routing Guidelines..... 38
12.2. Printed PCB Antenna Performance of ATWILC1000-MR110PB..... 39
12.3. ATWILC1000-MR110UB Placement and Routing Guidelines..... 42

13. Reflow Profile Information..... 44
13.1. Storage Condition..... 44
13.2. Solder Paste..... 44
13.3. Stencil Design..... 44
13.4. Printing Process..... 44
13.5. Baking Conditions..... 44
13.6. Soldering and Reflow Condition..... 45

14. Module Assembly Considerations..... 47

15. Regulatory Approval..... 48
15.1. United States..... 48
15.2. Canada..... 50
15.3. Europe..... 51

16. Reference Documentation..... 53

17. Document Revision History..... 54

The Microchip Web Site..... 57

Customer Change Notification Service..... 57

Customer Support..... 57

Microchip Devices Code Protection Feature..... 57

Legal Notice..... 58

Trademarks..... 58

Quality Management System Certified by DNV..... 59

Worldwide Sales and Service..... 60

1. Ordering Information and Module Marking

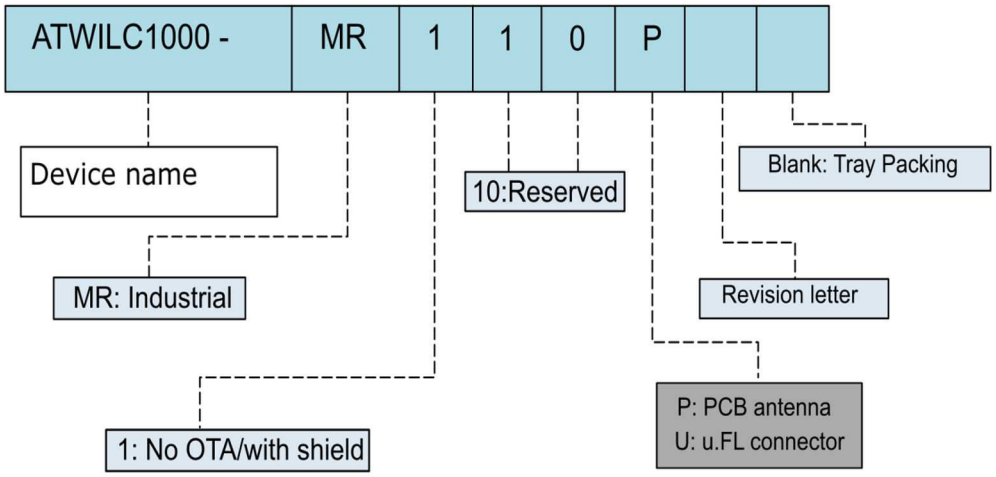
The following table provides the ordering details of the ATWILC1000-MR110xB module.

Table 1-1. Ordering Details

Model Number	Ordering Code	Package	No. of Pins	Description	Regulatory Certification
ATWILC1000-MR110PB	ATWILC1000-MR110PB	21.7x14.7x2.1 mm	28	Certified module with ATWILC1000B-MU chip and PCB antenna	FCC, IC, CE
ATWILC1000-MR110UB	ATWILC1000-MR110UB	21.7x14.7x2.1 mm	28	Certified module with ATWILC1000B-MU chip and uFL connector	FCC

The following figure provides the marking information of the ATWILC1000-MR110xB module.

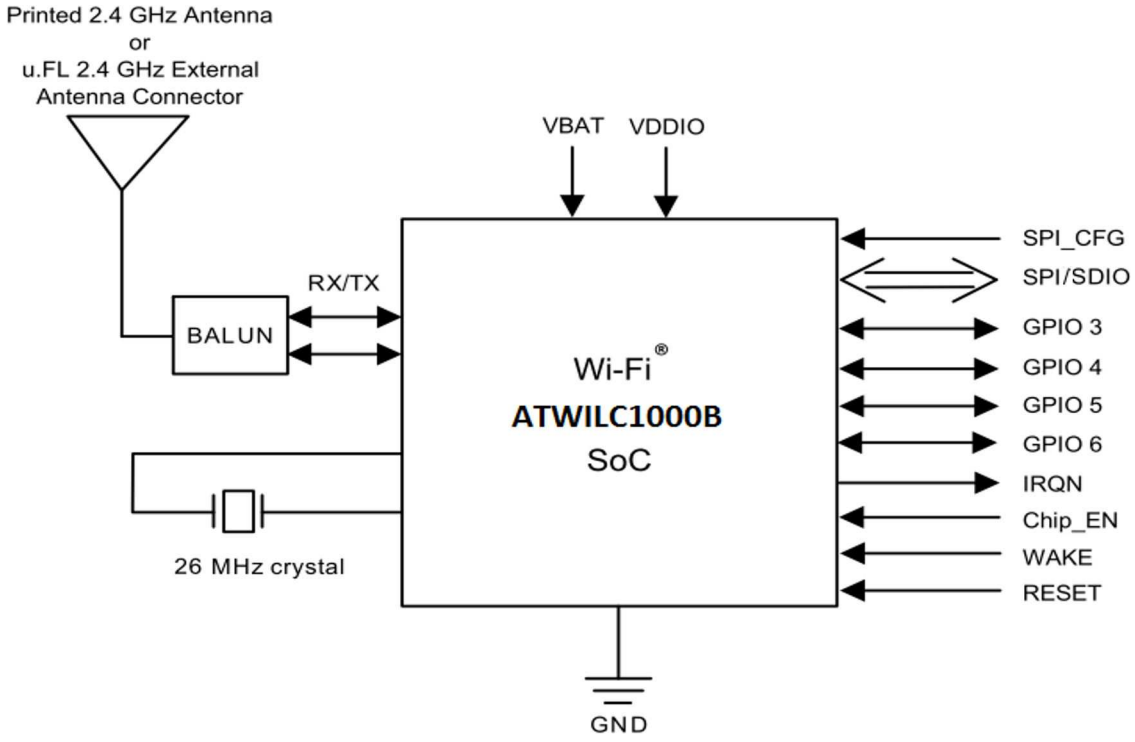
Figure 1-1. Marking Information



2. Block Diagram

The following figure provides a basic overview of the ATWILC1000-MR110xB module.

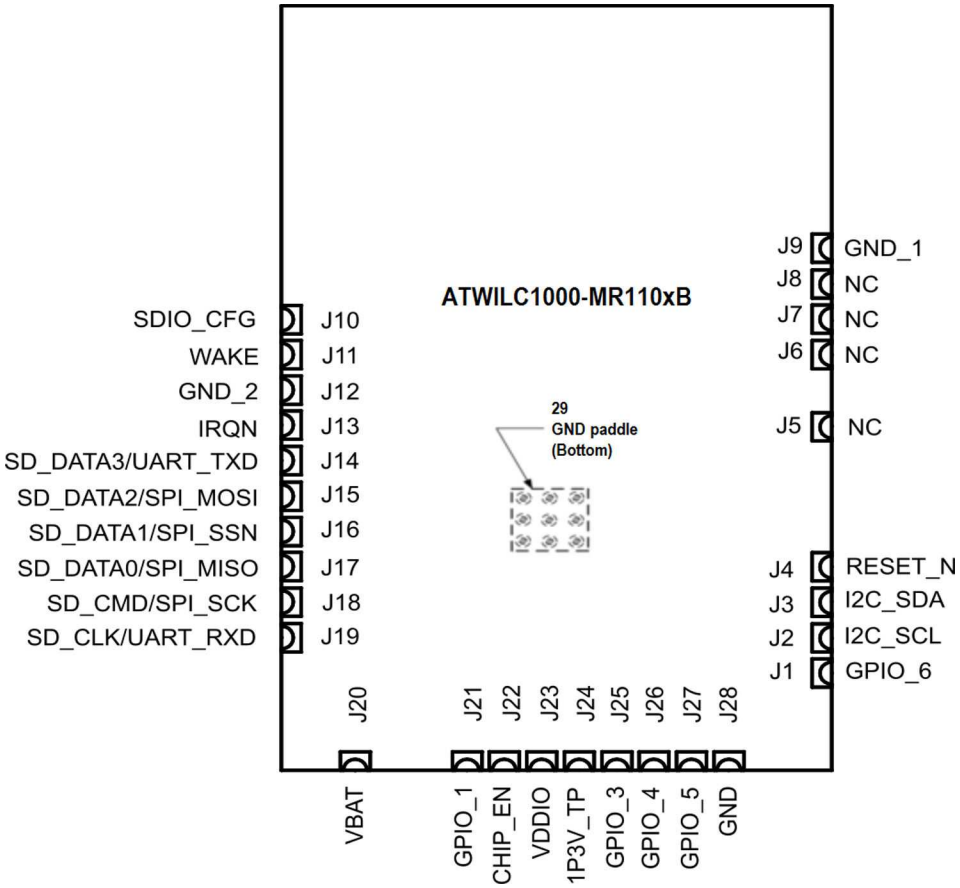
Figure 2-1. ATWILC1000-MR110xB Module Block Diagram



3. Pinout and Package Information

The ATWILC1000-MR110xB package has an exposed paddle that must be connected to the system board ground. The module pin assignment is shown in the following figure.

Figure 3-1. Pin Assignment



Note: This pin assignment is applicable for both ATWILC1000-MR110PB and ATWILC1000-MR110UB modules.

The following table describes the pin description of this module.

Table 3-1. Pin Details

Pin No.	Name	Type	Description	Programmable Pull up Resistor
1	GPIO_6	I/O	General purpose I/O.	-
2	I^2C_SCL	I/O	I^2C slave clock. Used only for development debug purposes. It is recommended to add test point for this pin.	-
3	I^2C_SDA	I/O	I^2C slave data. Used only for development debug purposes. It is recommended to add test point for this pin.	Yes
4	RESET_N	I	Active-low hard reset. When this pin is asserted low, the module is placed in the	Yes

Pin No.	Name	Type	Description	Programmable Pull up Resistor
			reset state. When this pin is asserted high, the module is out of reset and functions normally. Connect to a host output that defaults low at power-up. If the host output is tri-stated, add a 1 MΩ pull down resistor to ensure a low level at power-up.	
5	NC	–	No connection	-
6	NC	–	No connection	-
7	NC	–	No connection	-
8	NC	–	No connection	-
9	GND_1	Ground	-	-
10	SDIO_SPI_CFG	I	Connect to VDDIO through a 1MΩ resistor to enable the SPI interface. Connect to ground to enable SDIO interface.	No
11	WAKE	I	Host wake control.	No
12	GND_2	Ground	-	-
13	IRQN	O	The ATWILC1000-MR110xB device interrupt output. Connect to a host interrupt pin.	No
14	SD_DAT3	SDIO=I/O UART=O	SDIO Data Line 3 from the ATWILC1000-MR110xB when module is configured for SDIO.	Yes
15	SD_DAT2/ SPI_RXD	SDIO=I/O SPI=I	SDIO Data Line 2 signal from ATWILC1000-MR110xB when module is configured for SDIO. SPI MOSI (Master Out Slave In) pin when module is configured for SPI.	Yes
16	SD_DAT1/ SPI_SSN	SDIO=I/O SPI=I	SDIO Data Line 1 from ATWILC1000-MR110xB when module is configured for SDIO. Active low SPI slave select from the ATWILC1000 when module is configured for SPI.	Yes
17	SD_DAT0/ SPI_TXD	SDIO=I/O SPI=O	SDIO Data Line 0 from the ATWILC1000-MR110xB when module is configured for SDIO. SPI MISO (Master In Slave Out) pin from ATWILC1000 when module is configured for SPI.	Yes
18	SD_CMD/ SPI_CLK	SDIO=I/O	SDIO CMD line from ATWILC1000-MR110xB when module is configured for	Yes

Pin No.	Name	Type	Description	Programmable Pull up Resistor
		SPI=I	SDIO. SPI Clock from ATWILC1000 when module is configured for SPI.	
19	SD_CLK	SDIO=I UART=I	SDIO clock line for the ATWILC1000-MR110xB when module is configured for SDIO.	Yes
20	VBATT	Power supply	Power supply pin for the DC/DC convertor	Yes
21	GPIO_1	I/O	General purpose I/O	Yes
22	CHIP_EN	I	Module enable. High level enables module, low level places module in power-down mode. Connect to a host Output that defaults low at power-up. If the host output is tri-stated, add a 1MΩ pull down resistor if necessary to ensure a low level at power-up.	No
23	VDDIO	Power supply	I/O power supply. Must match host I/O voltage.	-
24	1P3V_TP	-	1.3V VDD Core Test Point. Decouple with 10uF and 0.01uF to GND	
25	GPIO_3	I/O	General purpose I/O. By default, UART receive input to ATWILC1000-MR110xB. Used only for development debug purposes. It is recommended to add test point for this pin.	Yes
26	GPIO_4	I/O	General purpose I/O.	Yes
27	GPIO_5	I/O	General purpose I/O. By default, UART transmit output from ATWILC1000-MR110xB. Used only for development debug purposes. It is recommended to add test point for this pin.	Yes
28	GND_3	Ground	-	-
29	Paddle	Ground	Exposed paddle GND. This pad must be soldered to system ground	-

The following table provides the ATWILC1000-MR110xB module package dimensions

Table 3-2. ATWILC1000-MR110xB Module Package Information

Parameter	Value	Units
Package Size	21.72 x 14.73	mm
Pad Count	28	-

Parameter	Value	Units
Total Thickness	2.11	mm
Pad Pitch	1.016	
Pad Width	0.82	
Exposed Pad size	3.7 x 3.7	

4. Electrical Specifications

4.1 Absolute Ratings

The absolute maximum ratings for this module are listed in the following table.

Table 4-1. ATWILC1000-MR110xB Module Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VBATT	Input supply voltage	-0.3	5.0	V
VDDIO	I/O voltage	-0.3	5.0	V

Caution: Stresses beyond those listed under "Absolute Maximum Ratings" cause permanent damage to the device. This is a stress rating only. The functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods affects the device reliability.

4.2 Recommended Operating Conditions

The recommended operating conditions for this module is listed in the following table.

Table 4-2. ATWILC1000-MR110xB Module Recommended Operating Conditions

Symbol	Min.	Typ.	Max.	Unit
VBATT	3.0	3.3	4.2	V
VDDIO	1.8	3.3	3.6	V
Operating temperature	-40		+85	ºC

Note:

1. VBATT should be equal to or greater than VDDIO.
2. The voltage of VDDIO is dependent on system I/O voltage.
3. Test Conditions: -40ºC to +85ºC

4.3 Receiver Performance

The following are typical conditions for radio receiver performance:

VBATT at 3.3 V; VDDIO at 3.3V; temperature at 25°C and WLAN Channel 6(2437 MHz).

The following table provides the receiver performance characteristics for this module.

Table 4-3. Receiver Performance

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency	-	2,412	-	2,472	MHz
Sensitivity 802.11b	1 Mbps DSSS	-	-94	-	dBm
	2 Mbps DSSS	-	-91	-	
	5.5 Mbps DSSS	-	-89	-	
	11 Mbps DSSS	-	-86	-	
Sensitivity 802.11g	6 Mbps OFDM	-	-88	-	dBm
	9 Mbps OFDM	-	-87	-	
	12 Mbps OFDM	-	-86	-	
	18 Mbps OFDM	-	-84	-	
	24 Mbps OFDM	-	-82	-	
	36 Mbps OFDM	-	-78	-	
	48 Mbps OFDM	-	-74	-	
	54 Mbps OFDM	-	-73	-	
Sensitivity 802.11n (BW at 20 MHz)	MCS 0	-	-87	-	dBm
	MCS 1	-	-85	-	
	MCS 2	-	-83	-	
	MCS 3	-	-80	-	
	MCS 4	-	-76	-	
	MCS 5	-	-73	-	
	MCS 6	-	-71	-	
	MCS 7	-	-69	-	
Maximum Receive Signal Level	1-11 Mbps DSSS		0	-	dBm
	6-54 Mbps OFDM		-5	-	
	MCS 0 – 7		-5	-	
Adjacent Channel Rejection	1 Mbps DSSS (30 MHz offset)	-	50	-	dB
	11 Mbps DSSS (25 MHz offset)	-	43	-	
	6 Mbps OFDM (25 MHz offset)	-	40	-	
	54 Mbps OFDM (25 MHz offset)	-	25	-	
	MCS 0 – 20 MHz BW (25 MHz offset)	-	40	-	
	MCS 7 – 20 MHz BW (25 MHz offset)	-	20	-	
Cellular Blocker Immunity	776-794 MHz CDMA	-	-14	-	dBm
	824-849 MHz GSM	-	-10	-	

Parameter	Description	Min.	Typ.	Max.	Unit
	880-915 MHz GSM	-	-10	-	
	1710-1785 MHz GSM	-	-15	-	
	1850-1910 MHz GSM	-	-15	-	
	1850-1910 MHz WCDMA	-	-24	-	
	1920-1980 MHz WCDMA	-	-24	-	

4.4 Transmitter Performance

The following are typical conditions for radio transmitter performance:

VBATT at 3.3 V; VDDIO at 3.3V; temperature at 25°C and WLAN Channel 6(2437 MHz).

The following table provides the transmitter performance characteristics for this module.

Table 4-4. Transmitter Performance

Parameter	Description	Unit	Minimum	Typical	Maximum
Frequency	-	MHz	2,412	-	2,472
Output Power[1-2], ON_Transmit	802.11b 1Mbps	dBm	-	17.6	-
	802.11b 11Mbps	dBm	-	18.2	-
	802.11g 6Mbps	dBm	-	18.7	-
	802.11g 54Mbps	dBm	-	16.7	-
	802.11n MCS 0	dBm	-	17.3	-
	802.11n MCS 7	dBm	-	13.8	-
Tx Power Accuracy	-	dB	-	±1.5[2]	-
Carrier Suppression	802.11b mode	dBc	-	-19.4	-
	802.11g mode	dBc	-	-27.5	-
	802.11n mode	dBc	-	-21.1	-
Out of Band Transmit Power	76-108	dBm/Hz	-	-125	-
	776-794	dBm/Hz	-	-125	-
	869-960	dBm/Hz	-	-125	-
	925-960	dBm/Hz	-	-125	-
	1570-1580	dBm/Hz	-	-125	-
	1805-1880	dBm/Hz	-	-125	-
	1930-1990	dBm/Hz	-	-125	-
	2110-2170	dBm/Hz	-	-125	-

Parameter	Description	Unit	Minimum	Typical	Maximum
Harmonic Output Power[4]	2nd	dBm/MHz	-	-28	-
	3rd	dBm/MHz	-	-33	-
	4th	dBm/MHz	-	-40	-
	5th	dBm/MHz	-	-28	-

Note:

1. Measured at 802.11 spec compliant EVM/Spectral Mask
2. Measured after RF matching network
3. Operating temperature range is -40°C to +85°C. RF performance is guaranteed at room temperature of 25°C with a 2-3dB change at boundary conditions.
4. Measured at 11Mbps, DG(Digital Gain)= -7, WLAN Channel 6 (2437 MHz).
5. With respect to TX power, different (higher/lower) RF output power settings may be used for specific antennas and/or enclosures, in which case recertification may be required.
6. The availability of some specific channels and/or operational frequency bands are country dependent and should be programmed at the Host product factory to match the intended destination. Regulatory bodies prohibit exposing the settings to the end user. This requirement needs to be taken care of via Host implementation.

4.5 Timing Characteristics

4.5.1 SPI Timing

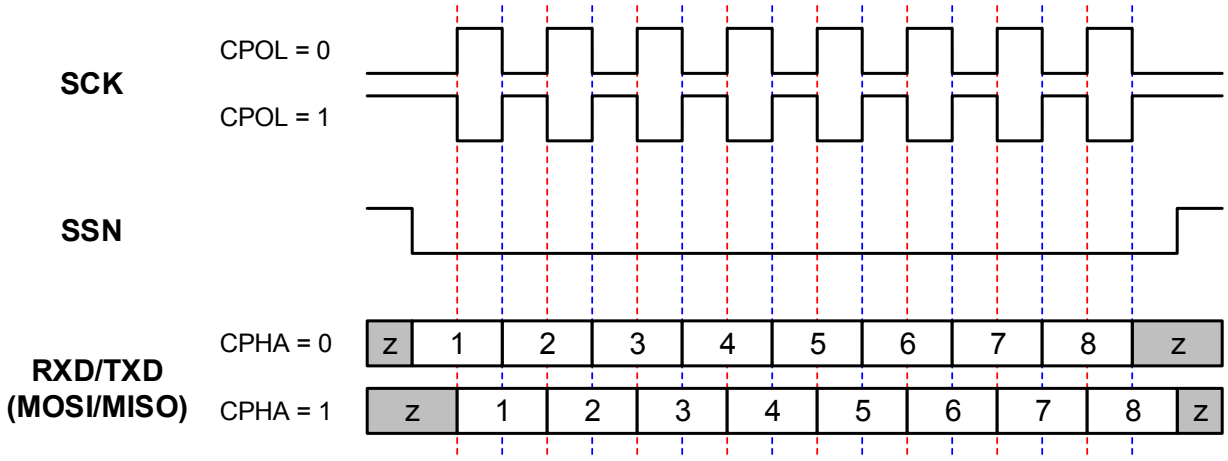
The SPI slave interface supports four standard modes as determined by the Clock Polarity (CPOL) and Clock Phase (CPHA) settings. These modes are illustrated in the following table.

Table 4-5. SPI Slave Modes

Mode	CPOL	CPHA
0	0	0
1	0	1
2	1	0
3	1	1

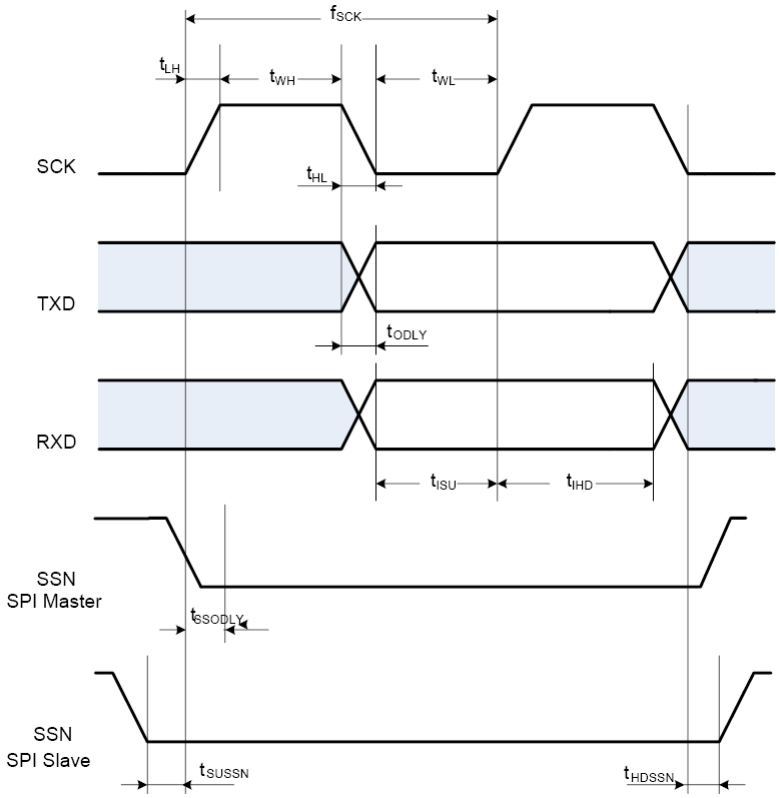
The red lines in the following figure correspond to clock phase at 0 and the blue lines correspond to clock phase at 1.

Figure 4-1. SPI Slave Clock Polarity and Clock Phase Timing



The SPI timing is shown in the following figure.

Figure 4-2. SPI Timing Diagram (SPI MODE CPOL=0, CPHA=0)



The SPI timing parameters are provided in the following table.

Table 4-6. SPI Slave Timing Parameters[1]

Parameter	Symbol	Min.	Max.	Units
Clock Input Frequency[2]	f_{SCK}	-	48	MHz
Clock Low Pulse Width	t_{WL}	4	-	ns
Clock High Pulse Width	t_{WH}	5	-	

Parameter	Symbol	Min.	Max.	Units
Clock Rise Time	t_{LH}	0	7	
Clock Fall Time	t_{HL}	0	7	
TXD Output Delay[3]	t_{ODLY}	4	9 from SCK fall 12.5 from SCK rise	
RXD Input Setup Time	t_{ISU}	1	-	
RXD Input Hold Time	t_{IHD}	5	-	
SSN Input Setup Time	t_{SUSSN}	3	-	
SSN Input Hold Time	t_{HDSSN}	5.5	-	

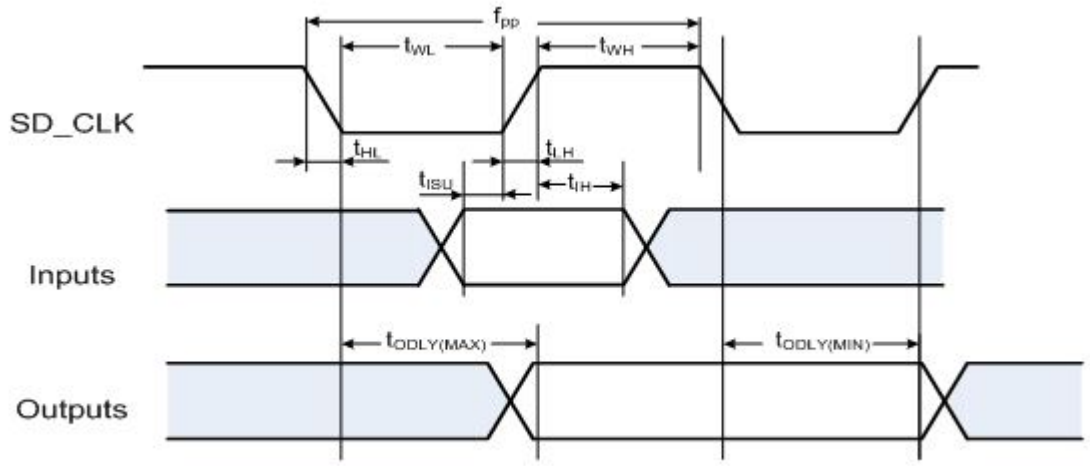
Note:

1. Timing is applicable to all SPI modes.
2. Maximum clock frequency specified is limited by the SPI slave interface internal design; actual maximum clock frequency can be lower and depends on the specific PCB layout.
3. Timing is based on 15pF output loading.

4.5.2 SDIO Timing

The SDIO Slave interface timing is shown in following figure.

Figure 4-3. SDIO Timing Diagram



Slave timing parameters are provided in the following table.

Table 4-7. SDIO Timing Parameters

Parameter	Symbol	Min	Max	Units
Clock Input Frequency[1]	f_{PP}	0	50	MHz
Clock Low Pulse Width	t_{WL}	9	-	ns

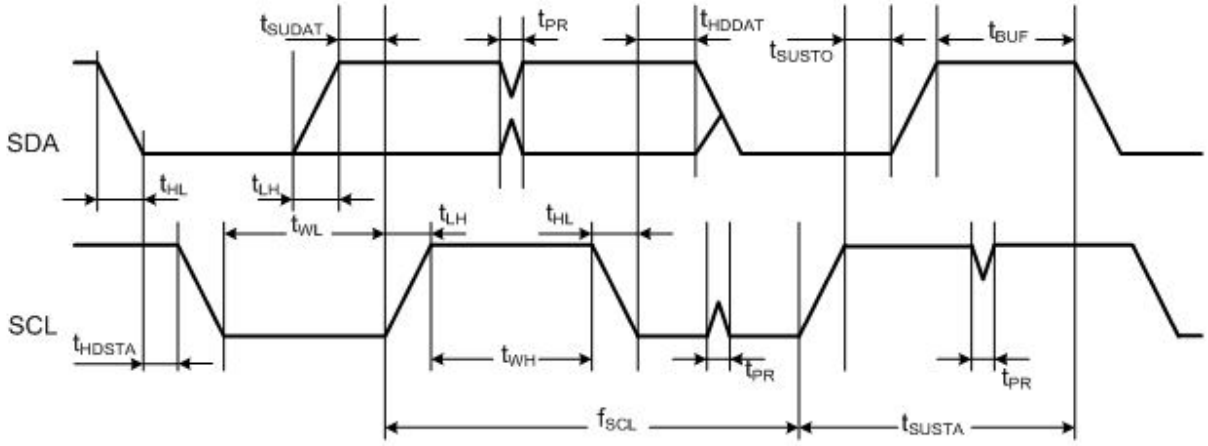
Parameter	Symbol	Min	Max	Units
Clock High Pulse Width	t_{WH}	4.5	-	
Clock Rise Time	t_{LH}	0	5	
Clock Fall Time	t_{HL}	0	5	
Input Setup Time	t_{ISU}	6	-	
Input Hold Time	t_{IH}	4	-	
Output Delay[2]	t_{ODLY}	3	11	

1. Maximum clock frequency specified is limited by the SDIO Slave interface internal design; actual maximum clock frequency can be lower and depends on the specific PCB layout.
2. Timing based on 15pF output loading.

4.5.3 I²C Timing

The following figure illustrates I²C Slave timing.

Figure 4-4. I²C Timing Diagram



The following table provides I²C Slave timing parameters.

Table 4-8. I2C Timing Parameters

Parameter	Symbol	Min	Max	Units	Remarks
SCL Clock Frequency	f_{SCL}	0	400	kHZ	-
SCL Low Pulse Width	t_{WL}	1.3	-	µs	-
SCL High Pulse Width	t_{WH}	0.6	-	µs	-
SCL, SDA Fall Time	t_{HL}	-	300	ns	-

Parameter	Symbol	Min	Max	Units	Remarks
SCL, SDA Rise Time	t_{LH}	-	300	ns	This is dictated by external components
START Setup Time	t_{SUSTA}	0.6	-	µs	-
START Hold Time	t_{HDSTA}	0.6	-	µs	-
SDA Setup Time	t_{SUDAT}	100	-	ns	-
SDA Hold Time	t_{HDDAT}	0	-	ns	Slave and Master Default
		40	-	ns	Master Programming Option
STOP Setup time	t_{SUSTO}	0.6	-	µs	-
Bus Free Time Between STOP and START	t_{BUF}	1.3	-	µs	-
Glitch Pulse Reject	t_{PR}	0	50	ns	-

5. Power Management

The ATWILC1000-MR110xB module has several device states:

- On states:
  - ON_Transmit – device actively transmits an 802.11 signal. Highest output power and nominal current consumption.
  - ON_Receive – device actively receivies an 802.11 signal. Lowest sensitivity and nominal current consumption.
  - ON_Doze – device is powered on but it does not actively transmit or receive the data.
  - Power_Down – device core supply is powered off.

The following pins are used to switch between the ON and Power_Down states:

- CHIP_EN – this pin (pin 22) enables or disables the DC/DC converter.
- VDDIO – I/O supply voltage from external supply.

In the ON states, VDDIO is ON and CHIP_EN is high (at VDDIO voltage level). To change from the ON states to Power_Down state, connect the RESETN and CHIP_EN pin to logic low (GND) by following the power down sequence mentioned in Power-Up/Down Sequence. When VDDIO is off and CHIP_EN is low, the chip is powered off with no leakage (also see Restrictions for Power States).

5.1 Current Consumption in Various Device States

The following table provides this module's current consumption in various device states.

Table 5-1. Current Consumption

Device State	Code Rate	Output Power (dBm)	Current Consumption[1]	
			I_{VBATT}	I_{VDDIO}
ON_Transmit	802.11b 1Mbps	17.6	266 mA	22 mA
	802.11b 11Mbps	18.5	239 mA	22 mA
	802.11g 6Mbps	18.6	249 mA	22 mA
	802.11g 54Mbps	16.9	173 mA	22 mA
	802.11n MCS 0	17.7	253 mA	22 mA
	802.11n MCS 7	14.0	164 mA	22 mA
ON_Receive	802.11b 1Mbps	N/A	63 mA	22 mA
	802.11b 11Mbps	N/A	63 mA	22 mA
	802.11g 6Mbps	N/A	63 mA	22 mA
	802.11g 54Mbps	N/A	63 mA	22 mA
	802.11n MCS 0	N/A	63 mA	22 mA
	802.11n MCS 7	N/A	63 mA	22 mA

Device State	Code Rate	Output Power (dBm)	Current Consumption[1]	
ON_Doze	N/A	N/A	380µA	<10µA
Power_Down	N/A	N/A	1.25 uA(2)	

Note:

1. The power consumption values are measured when VBAT is 3.3V and VDDIO is 3.3V at 25°C.
2. Current consumption mentioned for these states is the sum of current consumed in VDDIO and VBAT voltage rails.

5.2 Restrictions for Power States

When no power is supplied to the device, the DC/DC Converter output and VDDIO are both turned off (at ground potential). In this case, a voltage cannot be applied to the device pins because each pin contains an ESD diode from the pin to supply. This diode will turn on when voltage higher than one diode-drop is supplied to the pin.

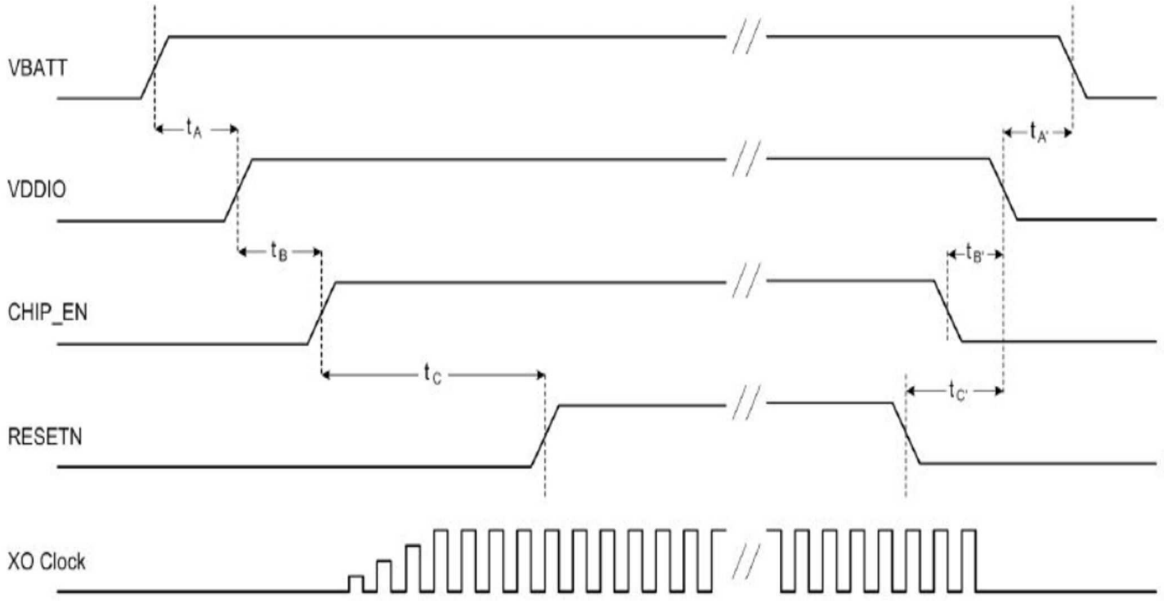
If a voltage must be applied to the signal pads while the chip is in a low power state, the VDDIO supply must be on, so the Sleep mode or power-down state must be used.

Similarly, to prevent the pin-to-ground diode from turning on, do not apply a voltage that is more than one diode-drop below ground to any pin.

5.3 Power-Up/Down Sequence

The following figure illustrates the power-up/down sequence for the ATWILC1000-MR110xB module.

Figure 5-1. Power-Up/Down Sequence



The following table provides power-up/down sequence timing parameters.

Table 5-2. Power-Up/Down Sequence Timing

Parameter	Min.	Max.	Units	Description	Notes
t_A	0	-	ms	VBAT rise to VDDIO rise	VBAT and VDDIO can rise simultaneously or connected together. VDDIO must not rise before VBAT.
t_B	0	-	ms	VDDIO rise to CHIP_EN rise	CHIP_EN must not rise before VDDIO. CHIP_EN must be driven high or low and must not be left floating.
t_C	5	-	ms	CHIP_EN rise to RESETN rise	This delay is required to stabilize the XO clock before RESETN removal. RESETN must be driven high or low and must not be left floating.
$t_{A'}$	0	-	ms	VDDIO fall to VBAT fall	VBAT and VDDIO fall simultaneously or connected together. VBAT must not fall before VDDIO.
$t_{B'}$	0	-	ms	CHIP_EN fall to VDDIO fall	VDDIO must not fall before CHIP_EN. CHIP_EN and RESETN must fall simultaneously.
$t_{C'}$	0	-	ms	RESETN fall to VDDIO fall	VDDIO must not fall before RESETN. RESETN and CHIP_EN fall simultaneously.

5.4 Digital I/O Pin Behavior During Power-Up Sequences

The following table represents the digital I/O pin states corresponding to the device power modes.

Table 5-3. Digital I/O Pin Behavior in Different Device States

Device State	VDDIO	CHIP_EN	RESETN	Output Driver	Input Driver	Pull Up/Down Resistor (96 kOhm)
Power_Down: core supply OFF	High	Low	Low	Disabled (Hi-Z)	Disabled	Disabled
Power-On Reset: core supply and hard reset ON	High	High	Low	Disabled (Hi-Z)	Disabled	Enabled
Power-On Default: core supply ON, device out of reset and not programmed	High	High	High	Disabled (Hi-Z)	Enabled	Enabled
On_Doze/ On_Transmit/	High	High	High	Programmed by firmware for each pin: enabled or disabled	Opposite of Output Driver state	Programmed by firmware for each pin: enabled or disabled

Device State	VDDIO	CHIP_EN	RESETN	Output Driver	Input Driver	Pull Up/Down Resistor (96 kOhm)
On_Receive: core supply ON, device programmed by firmware						

6. CPU and Memory Subsystems

6.1 Processor

This ATWILC1000-MR110xB module has a Cortus APS3 32-bit processor. This processor performs many of the MAC functions including but not limited to association, authentication, power management, security key management, and MSDU aggregation/deaggregation. In addition, the processor provides flexibility for various modes of operation, such as STA and AP modes.

6.2 Memory Subsystem

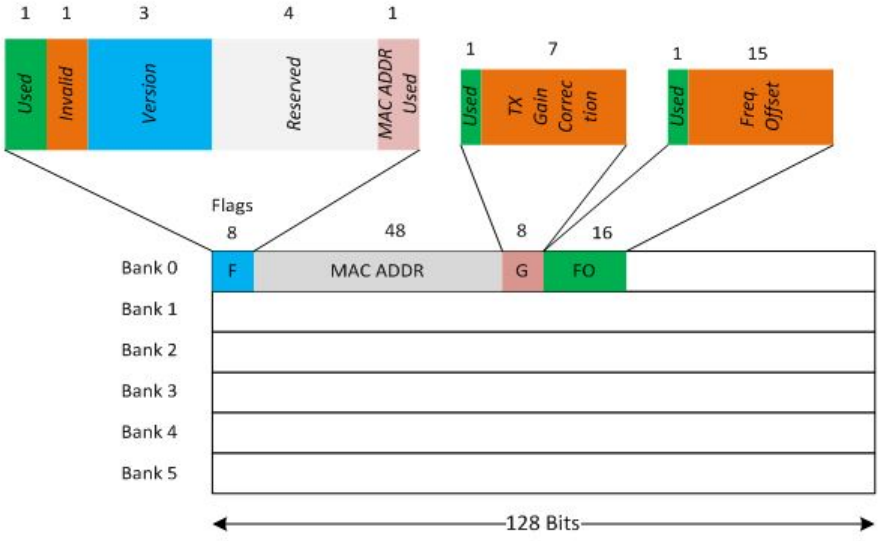
The APS3 core uses a 128 KB instruction/boot ROM along with a 160 KB instruction RAM and a 64 KB data RAM. In addition, the device uses a 128 KB shared RAM, accessible by the processor and MAC that allows the APS3 core to perform various data management tasks on the Tx and Rx data packets.

6.3 Nonvolatile Memory (eFuse)

This ATWILC1000-MR110xB module has 768 bits of nonvolatile eFuse memory that is read by the CPU after device reset. This nonvolatile One-Time-Programmable (OTP) memory is used to store customer specific parameters, such as MAC address; various calibration information, such as Tx power, crystal frequency offset etc; and other software-specific configuration parameters. The eFuse is partitioned into six 128 bit banks. Each bank has the same bit map, mentioned in the following figure. The purpose of the first 80 bits in each bank is fixed, and the remaining 48 bits are general purpose software dependent bits. Each bank is programmed independently, which allows for several updates of the device parameters following the initial programming. For example, if the MAC address has to be changed, Bank 1 has to be programmed with the new MAC address along with the values of TX gain correction and Frequency offset if they are used and programmed in the Bank 0. The contents of Bank 0 have to be invalidated in this case by programming the Invalid bit in the Bank 0. This will allow the firmware to use the MAC address from Bank 1.

By default, all the ATWILC1000-MR110PB and ATWILC1000-MR110UB modules are programmed with the MAC address and the Frequency offset bits of Bank 0.

Figure 6-1. eFuse Bit Map



7. WLAN Subsystem

The WLAN subsystem is composed of the Media Access Controller (MAC), Physical Layer (PHY), and the radio.

7.1 MAC

7.1.1 Description

This module is designed to operate at low power, while providing high data throughput. The IEEE 802.11 MAC functions are implemented with a combination of dedicated datapath engines, hardwired control logic, and a low power, high-efficiency microprocessor. The combination of dedicated logic with a programmable processor provides optimal power efficiency and real time response while providing the flexibility to accommodate evolving standards and future feature enhancements.

The dedicated datapath engines are used to implement data path functions with heavy computational requirements. For example, a Frame Check Sequence (FCS) engine checks the Cyclic Redundancy Check (CRC) of the transmitting and receiving packets, and a cipher engine performs all the required encryption and decryption operations for the WEP, WPA-TKIP, WPA2 CCMP-AES and WPA2 Enterprise security requirements.

Control functions, which have real time requirements, are implemented using hardwired control logic modules. These logic modules offer real time response while maintaining configurability through the processor. Examples of hardwired control logic modules are the channel access control module (implements EDCA/HCCA, Beacon Tx control, interframe spacing, and so on), protocol timer module (responsible for the Network Access vector, back-off timing, timing synchronization function, and slot management), MAC Protocol Data Unit (MPDU) handling module, aggregation/deaggregation module, block ACK controller (implements the protocol requirements for burst block communication), and Tx/Rx control Finite State Machine (FSM) (coordinate data movement between PHY and MAC interface, cipher engine, and the Direct Memory Acces (DMA) interface to the Tx/Rx FIFOs).

Following are the characteristics of MAC functions implemented solely in software on the microprocessor:

- Functions with high memory requirements or complex data structures. Examples are association table management and power save queuing.
- Functions with low computational load or without critical real time requirements. Examples are authentication and association.
- Functions that require flexibility and upgradeability. Examples are beacon frame processing and QoS scheduling.

7.1.2 Features

The ATWILC1000-MR110xB IEEE 802.11 MAC supports the following functions:

- IEEE 802.11b/g/n
- IEEE 802.11e WMM QoS EDCA/PCF multiple access categories traffic scheduling
- Advanced IEEE 802.11n features:
  - Transmission and reception of aggregated MPDUs (A-MPDU)
  - Transmission and reception of aggregated MSDUs (A-MSDU)
  - Immediate block acknowledgment
  - Reduced Interframe Spacing (RIFS)
- Supports IEEE 802.11i and WFA security with key management