Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

ATWILC1000B-MUT

IEEE 802.11 b/g/n Link Controller SoC

DATASHEET

Description

Atmel® ATWILC1000B is a single chip IEEE® 802.11b/g/n Radio/Baseband/MAC link controller optimized for low-power mobile applications. ATWILC1000B supports single stream 1x1 802.11n mode providing up to 72Mbps PHY rate. The ATWILC1000B features fully integrated Power Amplifier, LNA, Switch, and Power Management. Implemented in 65nm CMOS technology, the ATWILC1000B offers very low power consumption while simultaneously providing high performance and minimal bill of materials.

The ATWILC1000B supports 2- and 3-wire Bluetooth® coexistence protocols. The ATWILC1000B provides multiple peripheral interfaces including UART, SPI, I^2C, and SDIO. The only external clock source needed for the ATWILC1000B is a high-speed crystal or oscillator with a wide range of reference clock frequencies supported (12-40MHz). The ATWILC1000B is available in both QFN and Wafer Level Chip Scale Package (WLCSP) packaging.

Features

- IEEE 802.1 b/g/n 20MHz (1x1) solution
- Single spatial stream in 2.4GHz ISM band
- Integrated PA and T/R Switch
- Superior Sensitivity and Range via advanced PHY signal processing
- Advanced Equalization and Channel Estimation
- Advanced Carrier and Timing Synchronization
- Wi-Fi Direct and Soft-AP support
- Supports IEEE 802.11 WEP, WPA, and WPA2 Security
- Supports China WAPI security
- Superior MAC throughput via hardware accelerated two-level A-MSDU/A-MPDU frame aggregation and block acknowledgement
- On-chip memory management engine to reduce host load
- SPI, SDIO, UART, and I^2C host interfaces
- 2- or 3-wire Bluetooth coexistence interface
- Operating temperature range of -40°C to +85°C
- Power save modes:
  - <1µA Power Down mode typical @3.3V I/O
  - 380µA Doze mode with chip settings preserved (used for beacon monitoring)
  - On-chip low power sleep oscillator
  - Fast host wake-up from Doze mode by a pin or host I/O transaction

Table of Contents

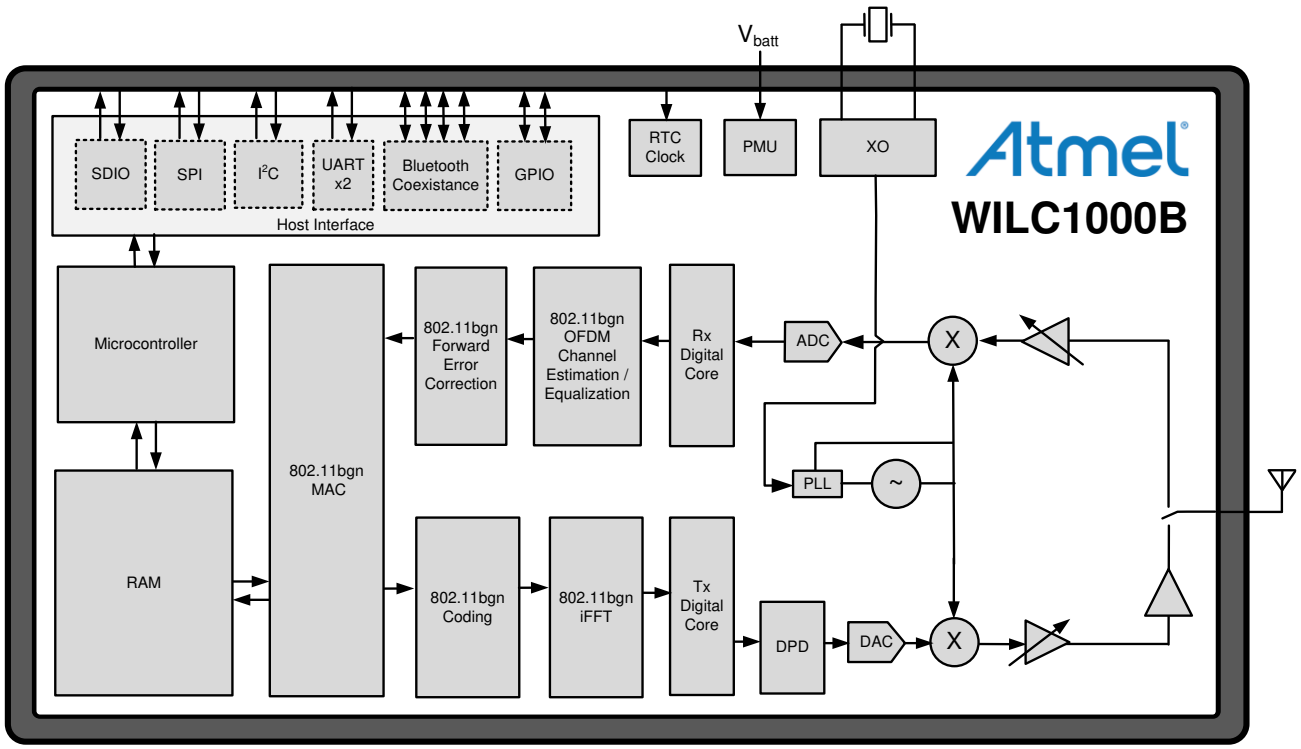
1 Ordering Information and IC Marking

Table 1-1. Ordering Details

Atmel official part number (for ordering)	Package type	IC marking
ATWILC1000B-MU-T	5x5 QFN in Tape and Reel	ATWILC1000B
ATWILC1000B-UU-T	3.25x3.25 WLCSP in Tape and Reel	ATWILC1000B

2 Block Diagram

Figure 2-1. ATWILC1000B Block Diagram



3 Pinout and Package Information

3.1 Pin Description

ATWILC1000B is offered in an exposed pad 40-pin QFN package. This package has an exposed paddle that must be connected to the system board ground. The QFN package pin assignment is shown in Figure 3-1. The color shading is used to indicate the pin type as follows:

- Green – power
- Red – analog
- Blue – digital I/O
- Yellow – digital input
- Grey – unconnected or reserved

The ATWILC1000B pins are described in Table 3-1.

Figure 3-1. Pin Assignment

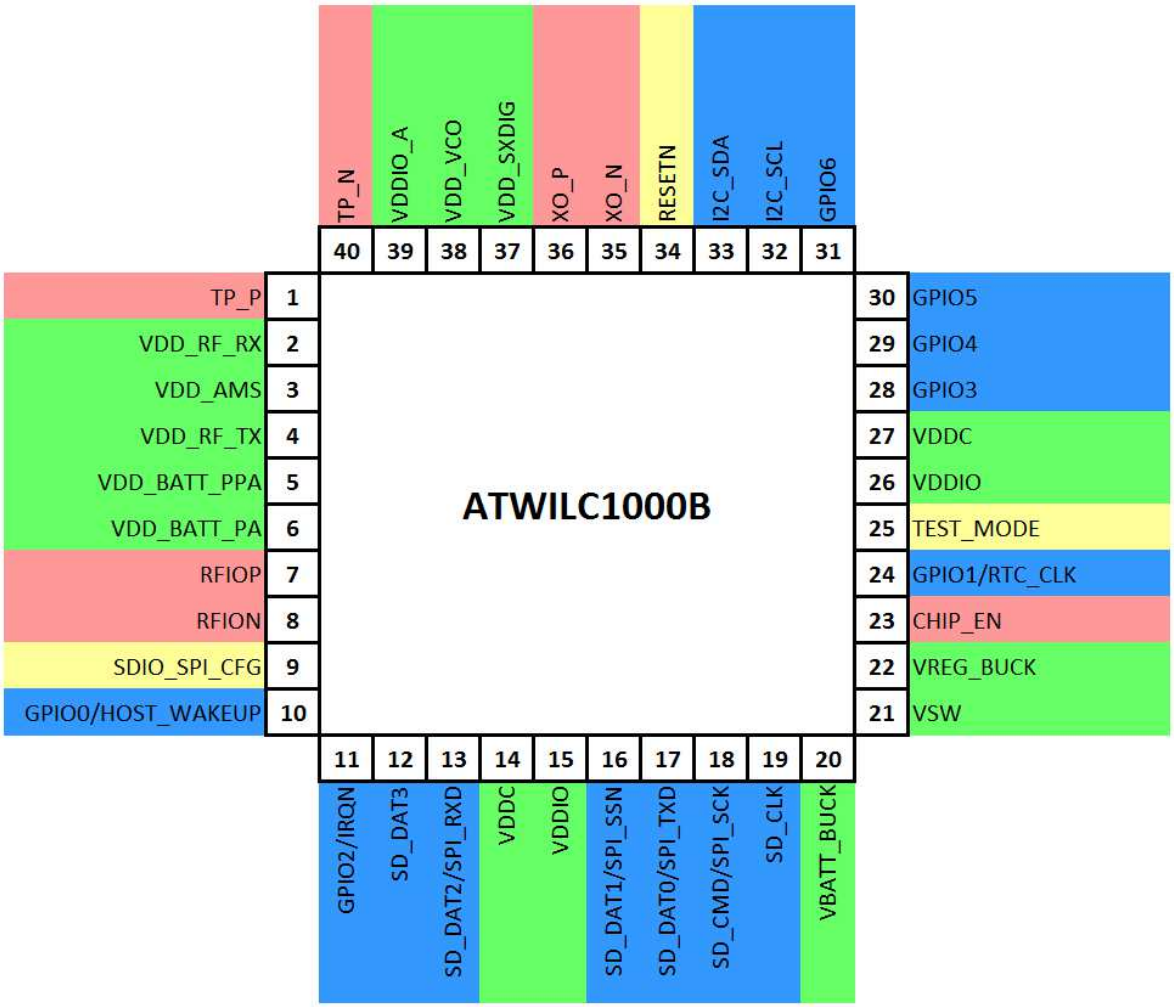


Table 3-1. Pin Description

Pin #	Pin Name	Pin Type	Description
1	TP_P	Analog	Test Pin/Customer No Connect
2	VDD_RF_RX	Power	Tuner RF Supply (see Section 9.1)
3	VDD_AMS	Power	Tuner BB Supply (see Section 9.1)
4	VDD_RF_TX	Power	Tuner RF Supply (see Section 9.1)
5	VDD_BATT_PPA	Power	PA 1st Stage Supply (see Section 9.1)
6	VDD_BATT_PA	Power	PA 2nd Stage Supply (see Section 9.1)
7	RFIOP	Analog	Pos. RF Differential I/O (see Table 9-3)
8	RFION	Analog	Neg. RF Differential I/O (see Table 9-3)
9	SDIO_SPI_CFG	Digital Input	Tie to 1 for SPI, 0 for SDIO
10	GPIO0/HOST_WAKE	Digital I/O, Programmable Pull-Up	GPIO0/SLEEP Mode Control
11	GPIO2/IRQN	Digital I/O, Programmable Pull-Up	GPIO2/Device Interrupt
12	SD_DAT3	Digital I/O, Programmable Pull-Up	SDIO Data3

Pin #	Pin Name	Pin Type	Description
13	SD_DAT2/SPI_RXD	Digital I/O, Programmable Pull-Up	SDIO Data2/SPI Data RX
14	VDDC	Power	Digital Core Power Supply (see Section 9.1)
15	VDDIO	Power	Digital I/O Power Supply (see Section 9.1)
16	SD_DAT1/SPI_SSN	Digital I/O, Programmable Pull-Up	SDIO Data1/SPI Slave Select
17	SD_DAT0/SPI_TXD	Digital I/O, Programmable Pull-Up	SDIO Data0/SPI Data TX
18	SD_CMD/SPI_SCK	Digital I/O, Programmable Pull-Up	SDIO Command/SPI Clock
19	SD_CLK	Digital I/O, Programmable Pull-Up	SDIO Clock
20	VBATT_BUCK	Power	Battery Supply for DC/DC Converter (see Section 9.1)
21	VSW	Power	Switching output of DC/DC Converter (see Section 9.1)
22	VREG_BUCK	Power	Core Power from DC/DC Converter (see Section 9.1)
23	CHIP_EN	Analog	PMU Enable
24	GPIO1/RTC_CLK	Digital I/O, Programmable Pull-Up	GPIO1/32kHz Clock Input
25	TEST_MODE	Digital Input	Test Mode – Customer Tie to GND
26	VDDIO	Power	Digital I/O Power Supply (see Section 9.1)
27	VDDC	Power	Digital Core Power Supply (see Section 9.1)
28	GPIO3	Digital I/O, Programmable Pull-Up	GPIO3/SPI_SCK_Flash
29	GPIO4	Digital I/O, Programmable Pull-Up	GPIO4/SPI_SSN_Flash
30	GPIO5	Digital I/O, Programmable Pull-Up	GPIO5/SPI_TXD_Flash
31	GPIO6	Digital I/O, Programmable Pull-Up	GPIO6/SPI_RXD_Flash
32	I2C_SCL	Digital I/O, Programmable Pull-Up	I2C Slave Clock (high-drive pad, see Table 4-3)
33	I2C_SDA	Digital I/O, Programmable Pull-Up	I2C Slave Data (high-drive pad, see Table 4-3)
34	RESETN	Digital Input	Active-Low Hard Reset
35	XO_N	Analog	Crystal Oscillator N
36	XO_P	Analog	Crystal Oscillator P
37	VDD_SXDIG	Power	SX Power Supply (see Section 9.1)
38	VDD_VCO	Power	VCO Power Supply (see Section 9.1)
39	VDDIO_A	Power	Tuner VDDIO Power Supply (see Section 9.1)
40	TPN	Analog	Test Pin/Customer No Connect
41[1]	PADDLE VSS	Power	Connect to System Board Ground

Notes: 1. Applies to QFN package only.

3.2 Package Description

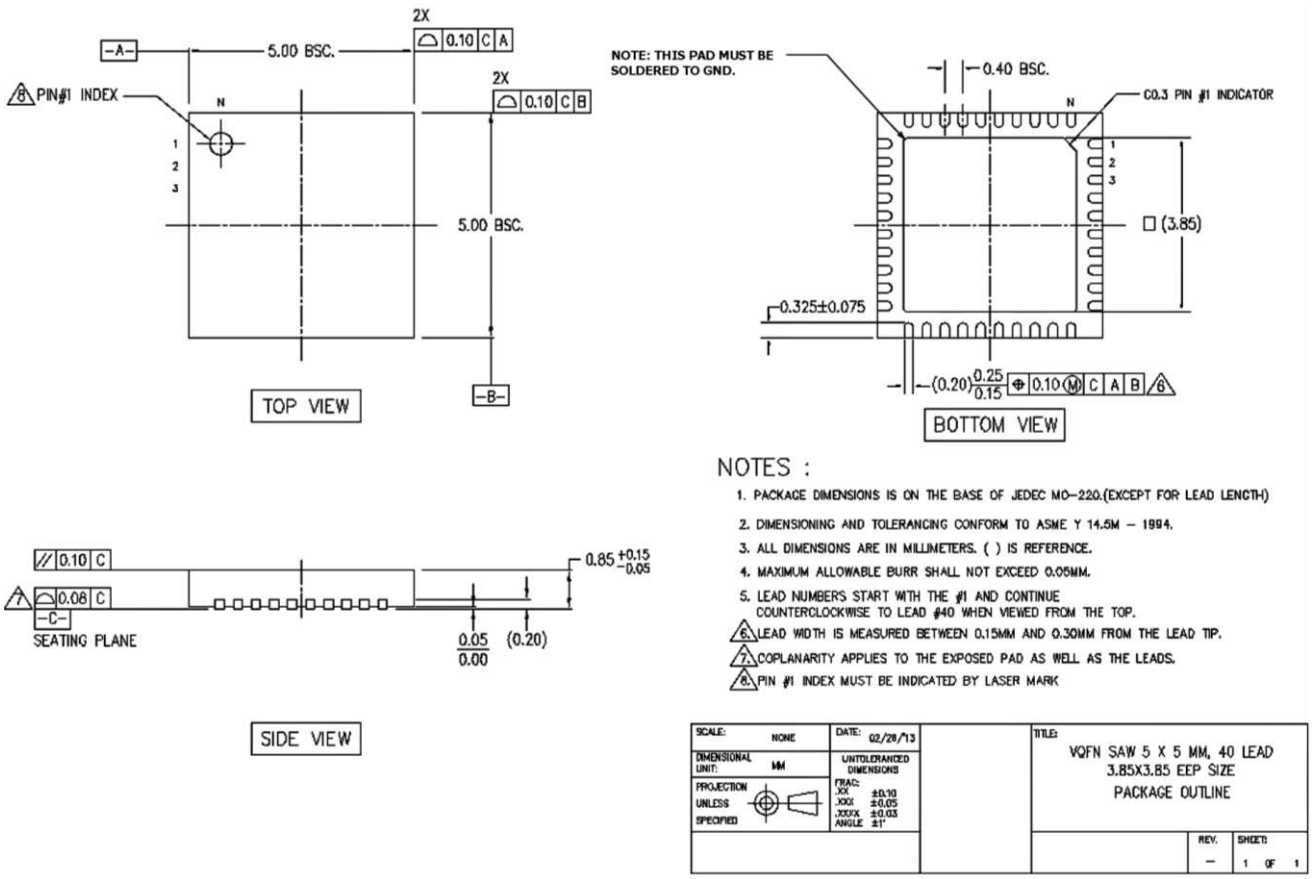
The ATWILC1000B QFN package information is provided in Table 3-2.

Table 3-2. QFN Package Information

Parameter	Value	Units	Tolerance
Package Size	5x5	mm	±0.1mm
QFN Pad Count	40		
Total Thickness	0.85	mm	±0.05mm
QFN Pad Pitch	0.40		
Pad Width	0.20		
Exposed Pad size	3.7x3.7		

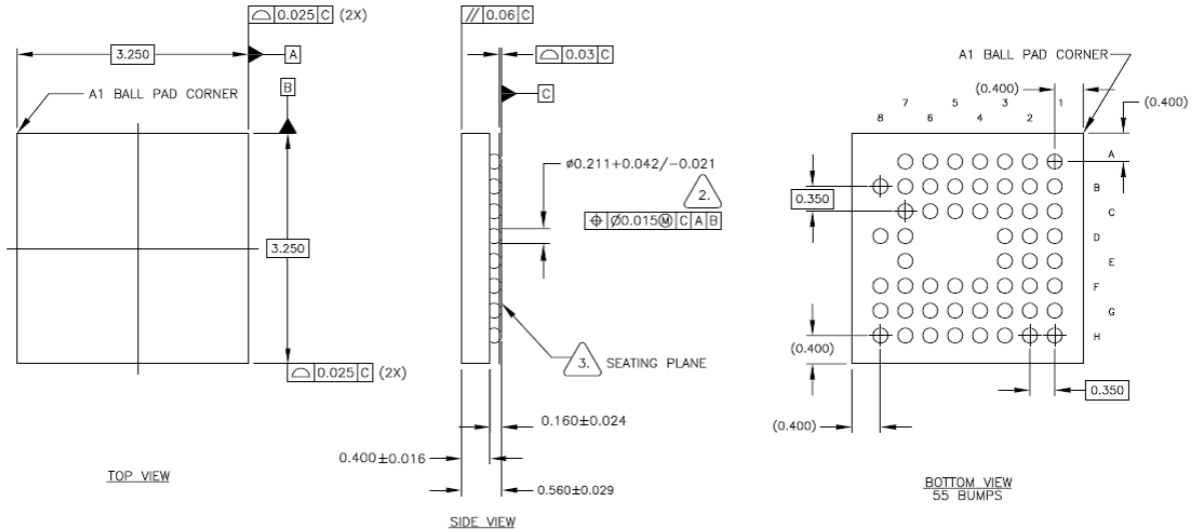
The ATWILC1000B 40L QFN package view is shown in Figure 3-2.

Figure 3-2. QFN Package



The QFN package is a qualified Green Package.

Figure 3-3. WLCSP Package



4. REFERENCE SPECIFICATION:
   A. AWW SPEC #001-2234: PACKING OPERATION PROCEDURE
   B. AWW SPEC #001-2062: MARKING

3. PRIMARY DATUM C AND SEATING PLACE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS

2. DIMENSIONS IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMENTER, PARALLEL TO PRIMARY DATUM C

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994

NOTES: UNLESS OTHERWISE SPECIFIED

DIMENSIONS IN MILLIMETERS UNLESS SPECIFIED	BODY X	BODY Y	BODY Z	BALL COUNT
DECIMAL X.X ±0.1, X.XX ±0.05, X.XXX ±0.030 ANGULAR ±1°	3.250	3.250	0.560	55
	BALL DIAMETER	RAW BALL DIAMETER		
	0.350	0.200		
	WILC3000B-MUT WLCSP			

Figure 3-4. WLCSP WILC1000B UU

8	7	6	5	4	3	2	1	
	VDDA_IO	VDDSXDIG	GNDSXDIG	XON	RESET	I2C_SCL	GPIO_6	A
NC	VDDRF	TPN	GNDIO	XOP	I2C_SDA	GPIO_5	GPIO_16	B
	GNDRF_RX	TPP	GPIO_13	GPIO_18	GPIO_17	GPIO_15	VDD	C
GNDBATT_PPA	VDDBATT				GPIO_4	TESTMODE	VDDIO	D
	GNDBATT_PA				GPIO_3	RTC_CLK	VSS	E
TXP	GNDAMS	HOST_WAKEUP	IRQN	SD_DAT3	VREGBUCK	CHIPEN	GND_BIAS	F
TXN	SDIO_SPI_CFG	GPIO_12	SD_DAT2	SD_DAT1	SD_DAT0_SPI_TXD	SD_CLK	GNDBUCK	G
VDDAMS	GPIO_11	VDD	VDDIO	VSS	SD_CMD_SPI_SCK	VBATT_BUCK	VSW	H

4 Electrical Specifications

4.1 Absolute Ratings

Table 4-1. Absolute Maximum Ratings

Characteristic	Symbol	Min.	Max.	Unit
Core Supply Voltage	VDDC	-0.3	1.5	V
I/O Supply Voltage	VDDIO	-0.3	5.0	
Battery Supply Voltage	VBATT	-0.3	5.0	
Digital Input Voltage	V_{IN}	-0.3	VDDIO	
Analog Input Voltage	V_{AIN}	-0.3	1.5	
ESD Human Body Model	V_{ESDHBM}	-1000, -2000 (see notes below)	+1000, +2000 (see notes below)	
Storage Temperature	T_A	-65	150	ºC
Junction Temperature			125	
RF input power max			23	dBm

Notes:
1. V_{IN} corresponds to all the digital pins.
2. V_{AIN} corresponds to the following analog pins: VDD_RF_RX, VDD_RF_TX, VDD_AMS, RFIOP, RFION, XO_N, XO_P, VDD_SXDIG, VDD_VCO.
3. For V_{ESDHBM}, each pin is classified as Class 1, or Class 2, or both:
   - The Class 1 pins include all the pins (both analog and digital)
   - The Class 2 pins are all digital pins only
   - V_{ESDHBM} is ±1kV for Class1 pins. V_{ESDHBM} is ±2kV for Class2 pins

4.2 Recommended Operating Conditions

Table 4-2. Recommended Operating Conditions

Characteristic	Symbol	Min.	Typ.	Max.	Unit
I/O Supply Voltage Low Range	$VDDIO_L$	1.62	1.80	2.00	V
I/O Supply Voltage Mid-Range	$VDDIO_M$	2.00	2.50	3.00	
I/O Supply Voltage High Range	$VDDIO_H$	3.00	3.30	3.60	
Battery Supply Voltage	VBATT	2.5A	3.60	4.20	
Operating Temperature		-40		85	ºC

Notes:
1. ATWILC1000B is functional across this range of voltages; however, optimal RF performance is guaranteed for VBATT in the range 3.0V < VBATT < 4.2V.
2. I/O supply voltage is applied to the following pins: VDDIO_A, VDDIO.
3. Battery supply voltage is applied to following pins: VDD_BATT_PPA, VDD_BATT_PA, VBATT_BUCK.
4. Refer to Section 9.1 and Table 9-3 for the details of power connections.

4.3 DC Electrical Characteristics

Table 4-3 provides the DC characteristics for the ATWILC1000B digital pads.

Table 4-3. DC Electrical Characteristics

VDDIO condition	Characteristic	Min.	Typ.	Max.	Unit
$VDDIO_L$	Input Low Voltage V_{IL}	-0.30		0.60	V
	Input High Voltage V_{IH}	VDDIO-0.60		VDDIO+0.30	
	Output Low Voltage V_{OL}			0.45	
	Output High Voltage V_{OH}	VDDIO-0.50			
$VDDIO_M$	Input Low Voltage V_{IL}	-0.30		0.63	
	Input High Voltage V_{IH}	VDDIO-0.60		VDDIO+0.30	
	Output Low Voltage V_{OL}			0.45	
	Output High Voltage V_{OH}	VDDIO-0.50			
$VDDIO_H$	Input Low Voltage V_{IL}	-0.30		0.65	
	Input High Voltage V_{IH}	VDDIO-0.60		VDDIO+0.30 (up to 3.60)	
	Output Low Voltage V_{OL}			0.45	
	Output High Voltage V_{OH}	VDDIO-0.50			
All	Output Loading			20	pF
All	Digital Input Load			6	
$VDDIO_L$	Pad Drive Strength (regular pads [1])	1.7	2.4		mA
$VDDIO_M$	Pad Drive Strength (regular pads [1])	3.4	6.5		
$VDDIO_H$	Pad Drive Strength (regular pads [1])	10.6	13.5		
$VDDIO_L$	Pad Drive Strength (high-drive pads [1])	3.4	4.8		
$VDDIO_M$	Pad Drive Strength (high-drive pads [1])	6.8	13		
$VDDIO_H$	Pad Drive Strength (high-drive pads [1])	21.2	27		

Note: 1. The following are high-drive pads: I2C_SCL, I2C_SDA; all other pads are regular.

5 Clocking

5.1 Crystal Oscillator

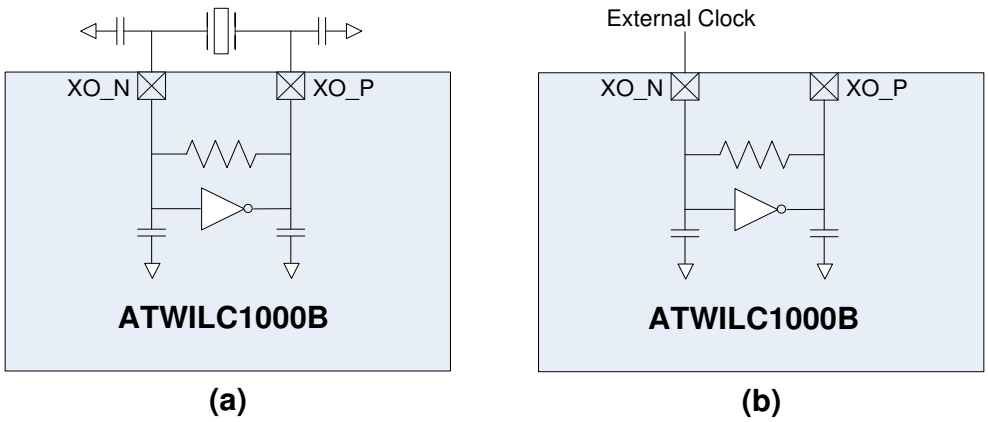
Table 5-1. Crystal Oscillator Parameters

Parameter	Min.	Typ.	Max.	Unit
Crystal Resonant Frequency	12	26	40	MHz
Crystal Equivalent Series Resistance		50	150	Ω
Stability – Initial Offset (1)	-100		100	ppm
Stability - Temperature and Aging	-25		25	

Note: 1. Initial offset must be calibrated to maintain ±25ppm in all operating conditions. This calibration is performed during final production testing.

The block diagram in Figure 5-1(a) shows how the internal Crystal Oscillator (XO) is connected to the external crystal. The XO has 5pF internal capacitance on each terminal XO_P and XO_N. To bypass the crystal oscillator with an external reference, an external signal capable of driving 5pF can be applied to the XO_N terminal as shown Figure 5-1(b).

Figure 5-1. XO Connections



(a) Crystal Oscillator is Used

b) Crystal Oscillator is Bypassed

Table 5-2 specifies the electrical and performance requirements for the external clock.

Table 5-2. Bypass Clock Specification

Parameter	Min.	Max.	Unit	Comments
Oscillation frequency	12	32	MHz	Must be able to drive 5pF load @ desired frequency
Voltage swing	0.5	1.2	Vpp	Must be AC coupled
Stability – Temperature and Aging	-25	+25	ppm	
Phase Noise		-130	dBc/Hz	At 10kHz offset
Jitter (RMS)		<1psec		Based on integrated phase noise spectrum from 1kHz to 1MHz

5.2 Low-Power Oscillator

ATWILC1000B has an internally-generated 32kHz clock to provide timing information for various sleep functions. Alternatively, ATWILC1000B allows for an external 32kHz clock to be used for this purpose, which is provided through Pin 24 (RTC_CLK). Software selects whether the internal clock or external clock is used.

The internal low-power clock is ring-oscillator based and has accuracy within 10,000ppm. When using the internal low-power clock, the advance wakeup time in beacon monitoring mode has to be increased by about 1% of the sleep time to compensate for the oscillator inaccuracy. For example, for the DTIM interval value of 1, wakeup time has to be increased by 1ms.

For any application targeting very low power consumption, an external 32kHz RTC clock should be used.

6 CPU and Memory Subsystems

6.1 Processor

ATWILC1000B has a Cortus APS3 32-bit processor. This processor performs many of the MAC functions, including but not limited to association, authentication, power management, security key management, and MSDU aggregation/de-aggregation. In addition, the processor provides flexibility for various modes of operation, such as STA and AP modes.

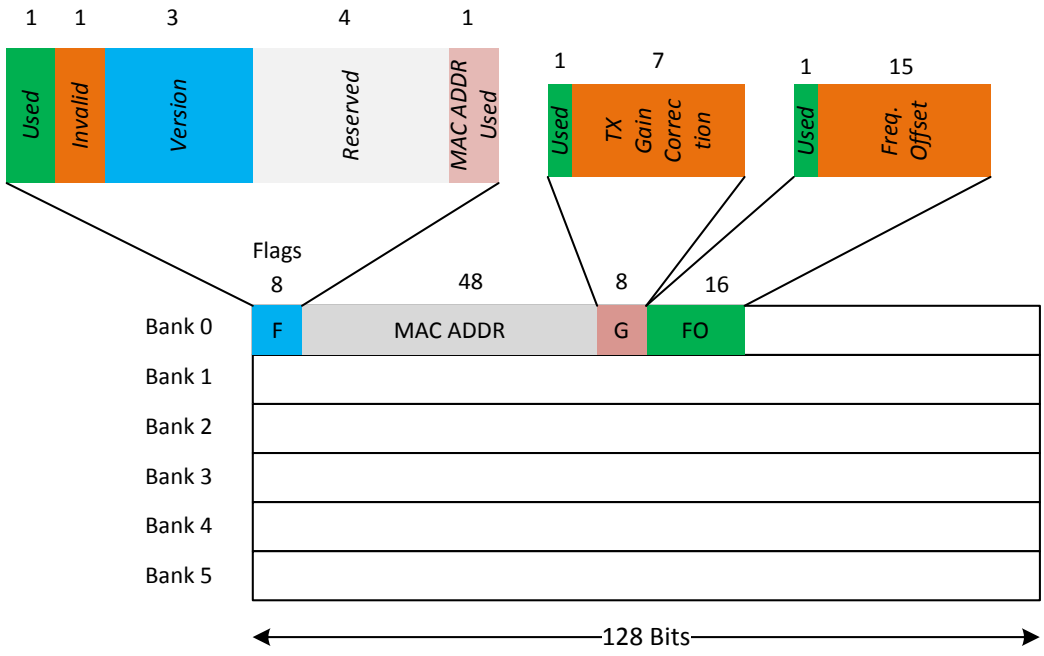
6.2 Memory Subsystem

The APS3 core uses a 128KB instruction/boot ROM along with a 160KB instruction RAM and a 64KB data RAM. In addition, the device uses a 128KB shared RAM, accessible by the processor and MAC, which allows the APS3 core to perform various data management tasks on the TX and RX data packets.

6.3 Non-volatile Memory (eFuse)

ATWILC1000B has 768 bits of non-volatile eFuse memory that can be read by the CPU after device reset. This non-volatile one-time-programmable (OTP) memory can be used to store customer-specific parameters, such as MAC address; various calibration information, such as TX power, crystal frequency offset, etc.; and other software-specific configuration parameters. The eFuse is partitioned into six 128-bit banks. Each bank has the same bit map, which is shown in Figure 6-1. The purpose of the first 80 bits in each bank is fixed, and the remaining 48 bits are general-purpose software dependent bits, or reserved for future use. Since each bank can be programmed independently, this allows for several updates of the device parameters following the initial programming e.g., updating MAC address. Refer to ATWILC1000B Programming Guide for the eFuse programming instructions.

Figure 6-1. eFuse Bit Map



7 WLAN Subsystem

The WLAN subsystem is composed of the Media Access Controller (MAC) and the Physical Layer (PHY). The following two subsections describe the MAC and PHY in detail.

7.1.1 Features

The ATWILC1000B IEEE802.11 MAC supports the following functions:

- IEEE 802.11b/g/n
- IEEE 802.11e WMM QoS EDCA/PCF multiple access categories traffic scheduling
- Advanced IEEE 802.11n features:
  - Transmission and reception of aggregated MPDUs (A-MPDU)
  - Transmission and reception of aggregated MSDUs (A-MSDU)
  - Immediate Block Acknowledgement
  - Reduced Interframe Spacing (RIFS)
- Support for IEEE 802.11i and WFA security with key management
  - WEP 64/128
  - WPA-TKIP
  - 128-bit WPA2 CCMP (AES)
- Support for WAPI security
- Advanced power management
  - Standard 802.11 Power Save Mode
  - Wi-Fi Alliance WMM-PS (U-APSD)
- RTS-CTS and CTS-self support
- Supports either STA or AP mode in the infrastructure basic service set mode
- Supports independent basic service set (IBSS)

7.1.2 Description

The ATWILC1000B MAC is designed to operate at low power while providing high data throughput. The IEEE 802.11 MAC functions are implemented with a combination of dedicated datapath engines, hardwired control logic, and a low-power, high-efficiency microprocessor. The combination of dedicated logic with a programmable processor provides optimal power efficiency and real-time response while providing the flexibility to accommodate evolving standards and future feature enhancements.

Dedicated datapath engines are used to implement data path functions with heavy computational requirements. For example, a FCS engine checks the CRC of the transmitting and receiving packets, and a cipher engine performs all the required encryption and decryption operations for the WEP, WPA-TKIP, WPA2 CCMP-AES, and WAPI security requirements.

Control functions which have real-time requirements are implemented using hardwired control logic modules. These logic modules offer real-time response while maintaining configurability via the processor. Examples of hardwired control logic modules are the channel access control module (implements EDCA/HCCA, Beacon TX control, interframe spacing, etc.), protocol timer module (responsible for the Network Access Vector, back-off timing, timing synchronization function, and slot management), MPDU handling module, aggregation/de-aggregation module, block ACK controller (implements the protocol requirements for burst block communication), and TX/RX control FSMs (coordinate data movement between PHY-MAC interface, cipher engine, and the DMA interface to the TX/RX FIFOs).

The MAC functions implemented solely in software on the microprocessor have the following characteristics:

- Functions with high memory requirements or complex data structures. Examples are association table management and power save queuing.
- Functions with low computational load or without critical real-time requirements. Examples are authentication and association.
- Functions which need flexibility and upgradeability. Examples are beacon frame processing and QoS scheduling.

7.2 PHY

7.2.1 Features

The ATWILC1000B IEEE802.11 PHY supports the following functions:

- Single antenna 1x1 stream in 20MHz channels
- Supports IEEE 802.11b DSSS-CCK modulation: 1, 2, 5.5, 11Mbps
- Supports IEEE 802.11g OFDM modulation: 6, 9, 12,18, 24, 36, 48, 54Mbps
- Supports IEEE 802.11n HT modulations MCS0-7, 20MHz, 800 and 400ns guard interval: 6.5, 7.2, 13.0, 14.4, 19.5, 21.7, 26.0, 28.9, 39.0, 43.3, 52.0, 57.8, 58.5, 65.0, 72.2Mbps
- IEEE 802.11n mixed mode operation
- Per packet TX power control
- Advanced channel estimation/equalization, automatic gain control, CCA, carrier/symbol recovery, and frame detection

7.2.2 Description

The ATWILC1000B WLAN PHY is designed to achieve reliable and power-efficient physical layer communication specified by IEEE 802.11b/g/n in single stream mode with 20MHz bandwidth. Advanced algorithms have been employed to achieve maximum throughput in a real world communication environment with impairments and interference. The PHY implements all the required functions such as FFT, filtering, FEC (Viterbi decoder), frequency and timing acquisition and tracking, channel estimation and equalization, carrier sensing and clear channel assessment, as well as the automatic gain control.

7.3 Radio

7.3.1 Receiver Performance

Radio Performance under Typical Conditions: VBATT=3.6V; VDDIO=3.3V; temp.: 25°C.

Table 7-1. Receiver Performance

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency		2,412		2,484	MHz
Sensitivity 802.11b	1Mbps DSS		-98		dBm
	2Mbps DSS		-94		
	5.5Mbps DSS		-92		
	11Mbps DSS		-88		
Sensitivity 802.11g	6Mbps OFDM		-90		dBm
	9Mbps OFDM		-89		

Parameter	Description	Min.	Typ.	Max.	Unit
	12Mbps OFDM		-88		
	18Mbps OFDM		-85		
	24Mbps OFDM		-83		
	36Mbps OFDM		-80		
	48Mbps OFDM		-76		
	54Mbps OFDM		-74		
Sensitivity 802.11n (BW=20MHz)	MCS 0		-89		dBm
	MCS 1		-87		
	MCS 2		-85		
	MCS 3		-82		
	MCS 4		-77		
	MCS 5		-74		
	MCS 6		-72		
	MCS 7		-70.5		
Maximum Receive Signal Level	1-11Mbps DSS	-10	0		dBm
	6-54Mbps OFDM	-10	0		
	MCS 0 – 7	-10	0		
Adjacent Channel Rejection	1Mbps DSS (30MHz offset)		50		dB
	11Mbps DSS (25MHz offset)		43		
	6Mbps OFDM (25MHz offset)		40		
	54Mbps OFDM (25MHz offset)		25		
	MCS 0 – 20MHz BW (25MHz offset)		40		
	MCS 7 – 20MHz BW (25MHz offset)		20		
Cellular Blocker Immunity	776-794MHz CDMA		-14		dBm
	824-849MHz GSM		-10		
	880-915MHz GSM		-10		
	1710-1785MHz GSM		-15		
	1850-1910MHz GSM		-15		
	1850-1910MHz WCDMA		-24		
	1920-1980MHz WCDMA		-24		

7.3.2 Transmitter Performance

Radio Performance under Typical Conditions: VBATT=3.6V; VDDIO=3.3V; temp.: 25°C.

Table 7-2. Transmitter Performance

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency		2,412		2,484	MHz
Output Power (1), ON_Transmit	802.11b 1Mbps		19.5		dBm
	802.11b 11Mbps		20.5		
	802.11g 6Mbps		19.5		
	802.11g 54Mbps		17.5		
	802.11n MCS 0		18.0		
	802.11n MCS 7		15.5		
TX Power Accuracy			±1.5 (2)		dB
Carrier Suppression			30.0		dBc
Harmonic Output Power	2nd		-33		dBm/MHz
	3rd		-38		

Notes: 1. Measured at 802.11 spec compliant EVM/Spectral Mask.
2. Measured at RF Pin assuming 50Ω differential.

8 External Interfaces

ATWILC1000B external interfaces include:

- I²C Slave for control
- SPI Slave and SDIO Slave for control and data transfer
- SPI Master for external Flash
- I²C Master for external EEPROM
- Two UARTs for debug, control, and data transfer
- General Purpose Input/Output (GPIO) pins
- Wi-Fi/Bluetooth coexistence interface

With the exception of the SPI Slave and SDIO Slave host interfaces, which are selected using the dedicated SDIO_SPI_CFG pin, the other interfaces can be assigned to various pins by programming the corresponding pin MUXing control register for each pin to a specific value between 0 and 6.The default values of these registers are 0, which is GPIO mode. The summary of the available interfaces and their corresponding pin MUX settings is shown in Table 8-1. For specific programming instructions, refer to ATWILC1000B Programming Guide.

Table 8-1. Pin-MUX Matrix of External Interfaces

Pin Name	Mux 0	Mux 1	Mux 2	Mux3	Mux4	Mux5	Mux6
GPIO0 / HOST_WAKEUP	GPIO_0	I_HOST_WAKEUP		O_UART1_TXD	IO_I2C_MASTER_SCL		IO_COE
GPIO2 / IRQN	GPIO_2	O_IRQN	O_UART1_TXD	I_UART1_RXD			IO_COE
SD_DAT3	GPIO_7	IO_SD_DAT3	IO_I2C_MASTER_SCL	O_UART1_TXD	O_SPI_SSN_FLASH	I_HOST_WAKEUP	IO_COE
SD_DAT2 / SPI_RXD		IO_SD_DAT2	I_SPI_RXD	I_UART1_RXD	O_UART2_TXD		
SD_DAT1 / SPI_SSN		IO_SD_DAT1	IO_SPI_SSN		O_UART2_RTS		
SD_DAT0 / SPI_TXD		IO_SD_DAT0	IO_SPI_TXD		I_UART2_RXD		
SD_CMD / SPI_SCK		IO_SD_CMD	IO_SPI_SCK		I_UART2_CTS	I_RTC_CLK	
SD_CLK	GPIO_8	I_SD_CLK	IO_I2C_MASTER_SDA	I_UART1_RXD	O_SPI_TXD_FLASH	O_UART1_TXD	IO_COE
GPIO1 / RTC_CLK	GPIO_1	I_RTC_CLK	O_UART1_TXD	I_UART1_RXD	IO_I2C_MASTER_SDA		IO_COE
GPIO_3	GPIO_3	O_SPI_SCK_FLASH		I_UART1_RXD		O_UART2_RTS	IO_COE
GPIO_4	GPIO_4	O_SPI_SSN_FLASH	IO_I2C_MASTER_SCL	I_UART2_RXD			IO_COE
GPIO_5	GPIO_5	O_SPI_TXD_FLASH	I_HOST_WAKEUP	O_UART1_TXD		I_UART2_CTS	IO_COE
GPIO_6	GPIO_6	I_SPI_RXD_FLASH	IO_I2C_MASTER_SDA	O_UART2_TXD			IO_COE
I2C_SCL		IO_I2C_SCL	O_UART1_TXD	I_RTC_CLK	IO_I2C_MASTER_SCL		IO_COE
I2C_SDA		IO_I2C_SDA	I_UART1_RXD		IO_I2C_MASTER_SDA		IO_COE

8.1 I²C Slave Interface

The I²C Slave interface, used primarily for control by the host processor, is a two-wire serial interface consisting of a serial data line (SDA, Pin 33) and a serial clock (SCL, Pin 32). It responds to the seven bit address value 0x60. The ATWILC1000B I²C supports I²C bus Version 2.1 - 2000 and can operate in standard mode (with data rates up to 100Kb/s) and fast mode (with data rates up to 400Kb/s).

The I²C Slave is a synchronous serial interface. The SDA line is a bidirectional signal and changes only while the SCL line is low, except for STOP, START, and RESTART conditions. The output drivers are open-drain to perform wire-AND functions on the bus. The maximum number of devices on the bus is limited by only the maximum capacitance specification of 400pF. Data is transmitted in byte packages.

For specific information, refer to the Philips Specification entitled “The I²C -Bus Specification, Version 2.1”.

The I²C Slave timing is provided in Figure 8-1 and Table 8-2.

Figure 8-1. I²C Slave Timing Diagram

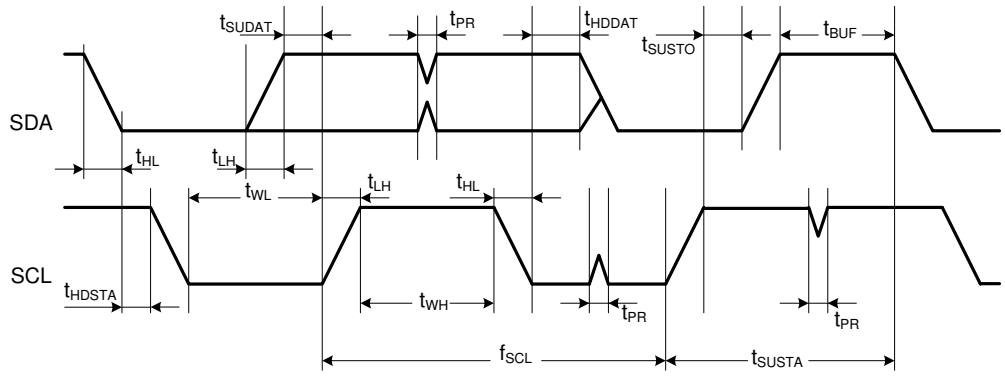


Table 8-2. I²C Slave Timing Parameters

Parameter	Symbol	Min.	Max.	Units	Remarks
SCL Clock Frequency	f_{SCL}	0	400	kHz	
SCL Low Pulse Width	t_{WL}	1.3		µs	
SCL High Pulse Width	t_{WH}	0.6			
SCL, SDA Fall Time	t_{HL}		300	ns	
SCL, SDA Rise Time	t_{LH}		300		This is dictated by external components
START Setup Time	t_{SUSTA}	0.6		µs	
START Hold Time	t_{HDSTA}	0.6			
SDA Setup Time	t_{SUDAT}	100		ns	
SDA Hold Time	t_{HDDAT}	0			Slave and Master Default
		40			Master Programming Option
STOP Setup time	t_{SUSTO}	0.6		µs	
Bus Free Time Between STOP and START	t_{BUF}	1.3			
Glitch Pulse Reject	t_{PR}	0	50	ns	

8.2 I²C Master Interface

ATWILC1000B provides an I²C bus master, which is intended primarily for accessing an external EEPROM memory through a software-defined protocol. The I²C Master is a two-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA can be configured on one of the following pins: SD_CLK (pin 19), GPIO1 (pin 24), GPIO6 (pin 31), or I2C_SDA (pin 33). SCL can be configured on one of the following pins: GPIO0 (pin 10), SD_DAT3 (pin 12), GPIO4 (pin 29), or I2C_SCL (pin 32). For more specific instructions refer to ATWILC1000B Programming Guide.

The I²C Master interface supports three speeds:

- Standard mode (100kb/s)
- Fast mode (400kb/s)
- High-speed mode (3.4Mb/s)

The timing diagram of the I²C Master interface is the same as that of the I²C Slave interface (see Figure 8-1). The timing parameters of I²C Master are shown in Table 8-3.

Table 8-3. I²C Master Timing Parameters

Parameter	Symbol	Standard Mode		Fast Mode		High-Speed Mode		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
SCL Clock Frequency	f_{SCL}	0	100	0	400	0	3400	kHz
SCL Low Pulse Width	t_{WL}	4.7		1.3		0.16		µs
SCL High Pulse Width	t_{WH}	4		0.6		0.06		
SCL Fall Time	t_{HLSCL}		300		300	10	40	ns
SDA Fall Time	t_{HLSDA}		300		300	10	80	
SCL Rise Time	t_{LHSCL}		1000		300	10	40	ns
SDA Rise Time	t_{LHSDA}		1000		300	10	80	
START Setup Time	t_{SUSTA}	4.7		0.6		0.16		µs
START Hold Time	t_{HDSTA}	4		0.6		0.16		
SDA Setup Time	t_{SUDAT}	250		100		10		ns
SDA Hold Time	t_{HDDAT}	5		40		0	70	
STOP Setup time	t_{SUSTO}	4		0.6		0.16		µs
Bus Free Time Between STOP and START	t_{BUF}	4.7		1.3				
Glitch Pulse Reject	t_{PR}			0	50			

8.3 SPI Slave Interface

ATWILC1000B provides a Serial Peripheral Interface (SPI) that operates as a SPI slave. The SPI Slave interface can be used for control and for serial I/O of 802.11 data. The SPI Slave pins are mapped as shown in Table 8-4. The RXD pin is same as Master Output, Slave Input (MOSI), and the TXD pin is same as Master Input, Slave Output (MISO). The SPI Slave is a full-duplex slave-synchronous serial interface that is available immediately following reset when pin 9 (SDIO_SPI_CFG) is tied to VDDIO.

Table 8-4. SPI Slave Interface Pin Mapping

Pin #	SPI Function
9	CFG: Must be tied to VDDIO
16	SSN: Active Low Slave Select
18	SCK: Serial Clock
13	RXD: Serial Data Receive (MOSI)
17	TXD: Serial Data Transmit (MISO)

When the SPI is not selected, i.e., when SSN is high, the SPI interface will not interfere with data transfers between the serial-master and other serial-slave devices. When the serial slave is not selected, its transmitted data output is buffered, resulting in a high impedance drive onto the serial master receive line.

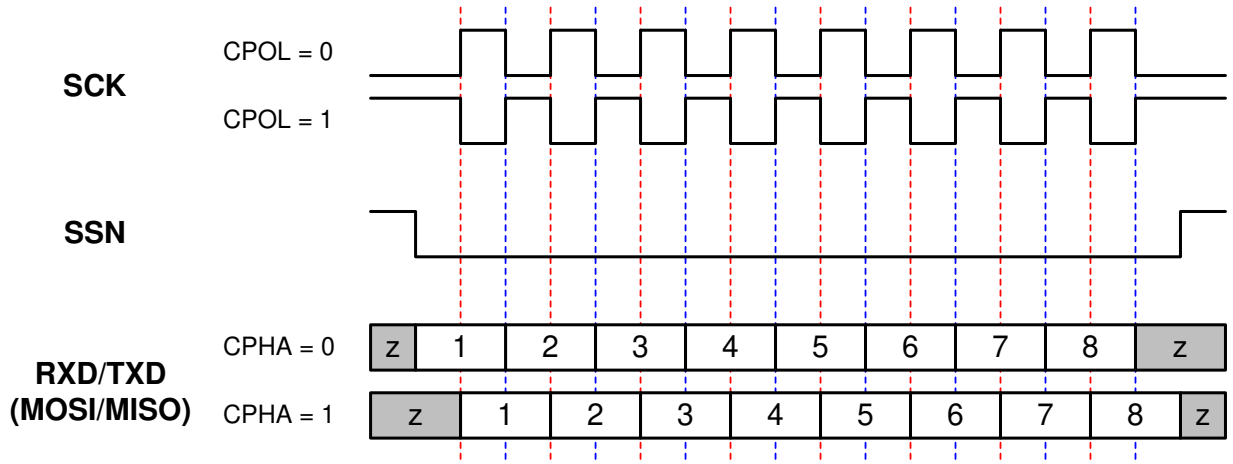
The SPI Slave interface responds to a protocol that allows an external host to read or write any register in the chip as well as initiate DMA transfers. For the details of the SPI protocol and more specific instructions refer to ATWILC1000B Programming Guide.

The SPI Slave interface supports four standard modes as determined by the Clock Polarity (CPOL) and Clock Phase (CPHA) settings. These modes are illustrated in Table 8-5 and Figure 8-2. The red lines in Figure 8-2 correspond to Clock Phase = 0 and the blue lines correspond to Clock Phase = 1.

Table 8-5. SPI Slave Modes

Mode	CPOL	CPHA
0	0	0
1	0	1
2	1	0
3	1	1

Figure 8-2. SPI Slave Clock Polarity and Clock Phase Timing



The SPI Slave timing is provided in Figure 8-3 and Table 8-6.

Figure 8-3. SPI Slave Timing Diagram

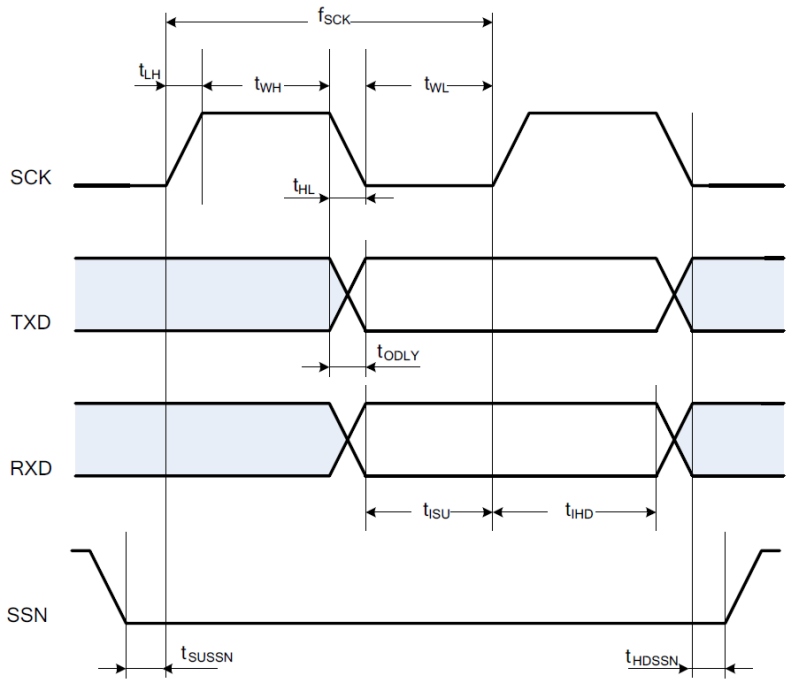


Table 8-6. SPI Slave Timing Parameters

Parameter	Symbol	Min.	Max.	Units
Clock Input Frequency	f_{SCK}		48	MHz
Clock Low Pulse Width	t_{WL}	5		ns
Clock High Pulse Width	t_{WH}	5		
Clock Rise Time	t_{LH}		5	
Clock Fall Time	t_{HL}		5	
Input Setup Time	t_{ISU}	5		
Input Hold Time	t_{IHD}	5		
Output Delay	t_{ODLY}	0	20	
Slave Select Setup Time	t_{SUSSN}	5		
Slave Select Hold Time	t_{HDSSN}	5		

8.4 SPI Master Interface

ATWILC1000B provides a SPI Master interface for accessing external Flash memory. The SPI Master pins are mapped as shown in Table 8-7. The TXD pin is same as Master Output, Slave Input (MOSI), and the RXD pin is same as Master Input, Slave Output (MISO). The SPI Master interface supports all four standard modes of clock polarity and clock phase shown in Table 8-5. External SPI Flash memory is accessed by a processor programming commands to the SPI Master interface, which in turn initiates a SPI master access to the Flash. For more specific instructions refer to ATWILC1000B Programming Guide.

Table 8-7. SPI Master Interface Pin Mapping

Pin #	Pin Name	SPI Function
28	GPIO3	SCK: Serial Clock Output
29	GPIO4	SCK: Active Low Slave Select Output
30	GPIO5	TXD: Serial Data Transmit Output (MOSI)
31	GPIO6	RXD: Serial Data Receive Input (MISO)

The SPI Master timing is provided in Figure 8-4 and Table 8-8.

Figure 8-4. SPI Master Timing Diagram

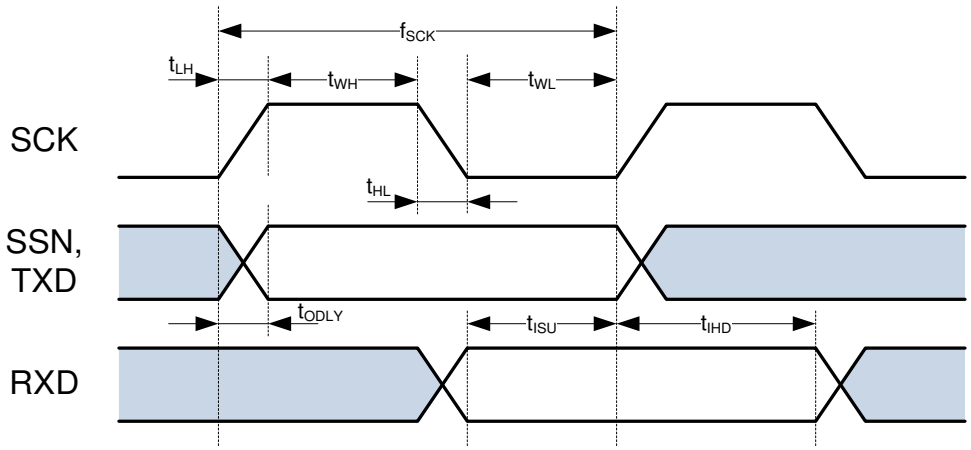


Table 8-8. SPI Master Timing Parameters

Parameter	Symbol	Min.	Max.	Units
Clock Output Frequency	f_{SCK}		48	MHz
Clock Low Pulse Width	t_{WL}	5		ns
Clock High Pulse Width	t_{WH}	5		
Clock Rise Time	t_{LH}		5	
Clock Fall Time	t_{HL}		5	
Input Setup Time	t_{ISU}	5		
Input Hold Time	t_{IHD}	5		
Output Delay	t_{ODLY}	0	5	

8.5 SDIO Slave Interface

The ATWILC1000B SDIO Slave is a full speed interface. The interface supports the 1-bit/4-bit SD transfer mode at the clock range of 0-50MHz. The Host can use this interface to read and write from any register within the chip as well as configure the ATWILC1000B for data DMA. To use this interface, pin 9 (SDIO_SPI_CFG) must be grounded. The SDIO Slave pins are mapped as shown in Table 8-9.