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WINC1500-MR210PA DATASHEET

IEEE 802.11 b/g/n IoT Module

Datasheet

Description

The ATWINC1500-MR210PA is a low-power consumption 802.11 b/g/n IoT (Internet of Things) module which is specifically optimized for low power IoT applications. The highly integrated module features small form factor (21.5mm x 14.5mm x3.4mm) while fully integrating Power Amplifier, LNA, Switch, Power Management, and PCB antenna. With seamless roaming capabilities and advanced security, it could be interoperable with various vendors' 802.11b/g/n Access Points in wireless LAN. The module provides SPI and UART to interface to host controller.

Features

- IEEE® 802.11 b/g/n 20MHz (1x1) solution
- Single spatial stream in 2.4GHz ISM band
- Integrated PA and T/R Switch
- Integrated PCB antenna
- Superior Sensitivity and Range via advanced PHY signal processing
- Advanced Equalization and Channel Estimation
- Advanced Carrier and Timing Synchronization
- Wi-Fi Direct and Soft-AP support
- Supports IEEE 802.11 WEP, WPA, WPA2 Security
- Supports China WAPI security
- Superior MAC throughput via hardware accelerated two-level A-MSDU/A-MPDU frame aggregation and block acknowledgement
- On-chip memory management engine to reduce host load
- SPI, UART, and I^2C host interfaces
- 2- or 3-wire Bluetooth® coexistence interface
- Operating temperature range of -40°C to +85°C
- I/O operating voltage of 2.7V to 3.6V
- Integrated Flash memory for system software
- Power Save Modes
  - 4µA Deep Power Down mode typical @3.3V I/O
  - 850µA Doze mode (Chip settings are preserved. Used for beacon monitoring mode)[1]

[1]See Power Consumption for module power modes.

  - On-chip low power sleep oscillator
  - Fast host wake-up from Doze mode by a pin or SPI transaction
- Fast Boot Options
  - On-Chip Boot ROM (Firmware instant boot)
  - SPI flash boot (firmware patches and state variables)
  - Low-leakage on-chip memory for state variables
  - Fast AP Re-Association (150ms)
- On-Chip Network Stack to offload MCU
  - Integrated Network IP stack to minimize host CPU requirements
  - Network features TCP, UDP, DHCP, ARP, HTTP, SSL, and DNS
- Small footprint host driver (4KB flash – less than 1KB RAM)

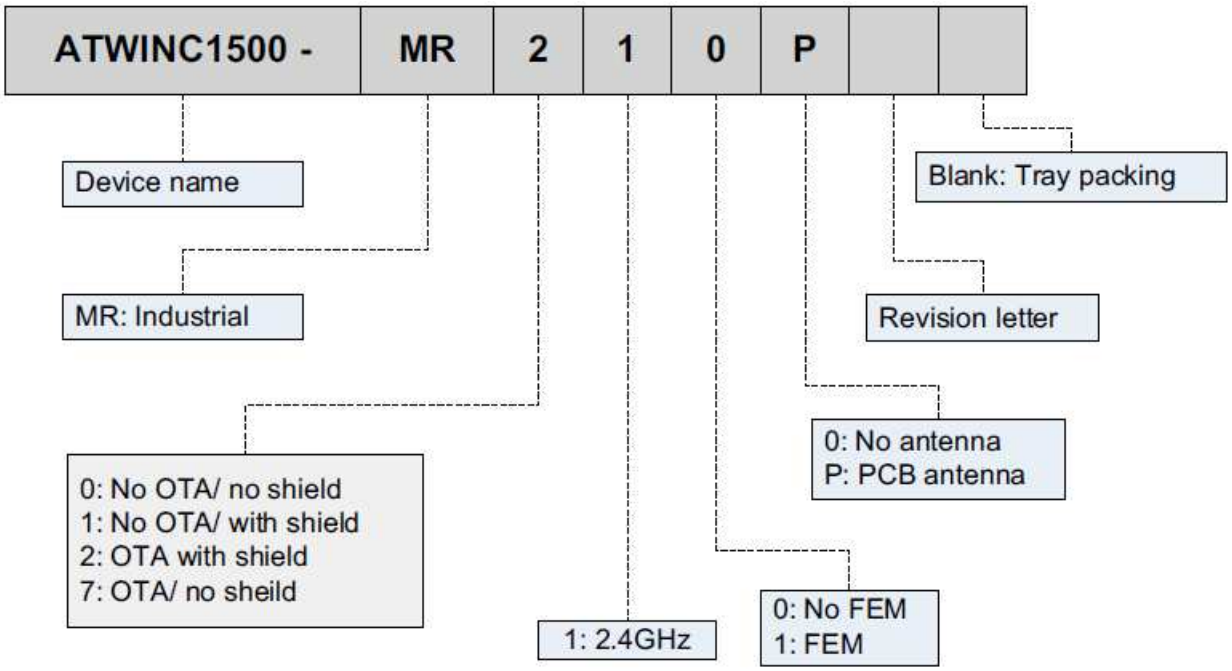
Table of Contents

1 Ordering Information and Module Marking

Table 1-1. Ordering Details

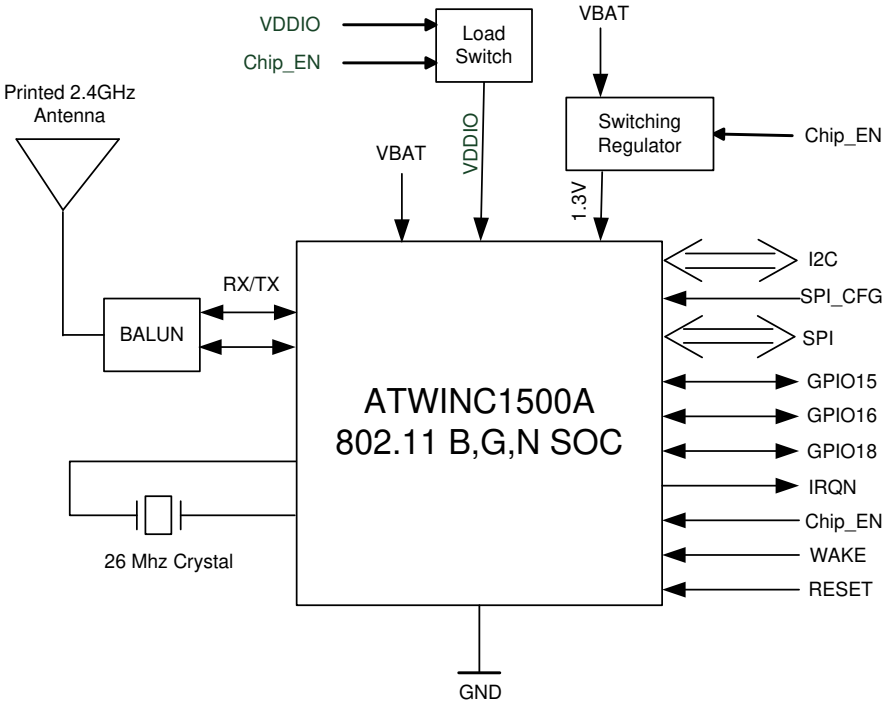
Ordering Code	Package	Description
ATWINC1500-MR210PA	22x15mm	Certified module with ATWINC1500A chip and PCB antenna

Figure 1-1. Marking Information



2 Block Diagram

Figure 2-1. Block Diagram of the Module



3 Pinout Information

3.1 Pin Description

Figure 3-1. Pin Assignment

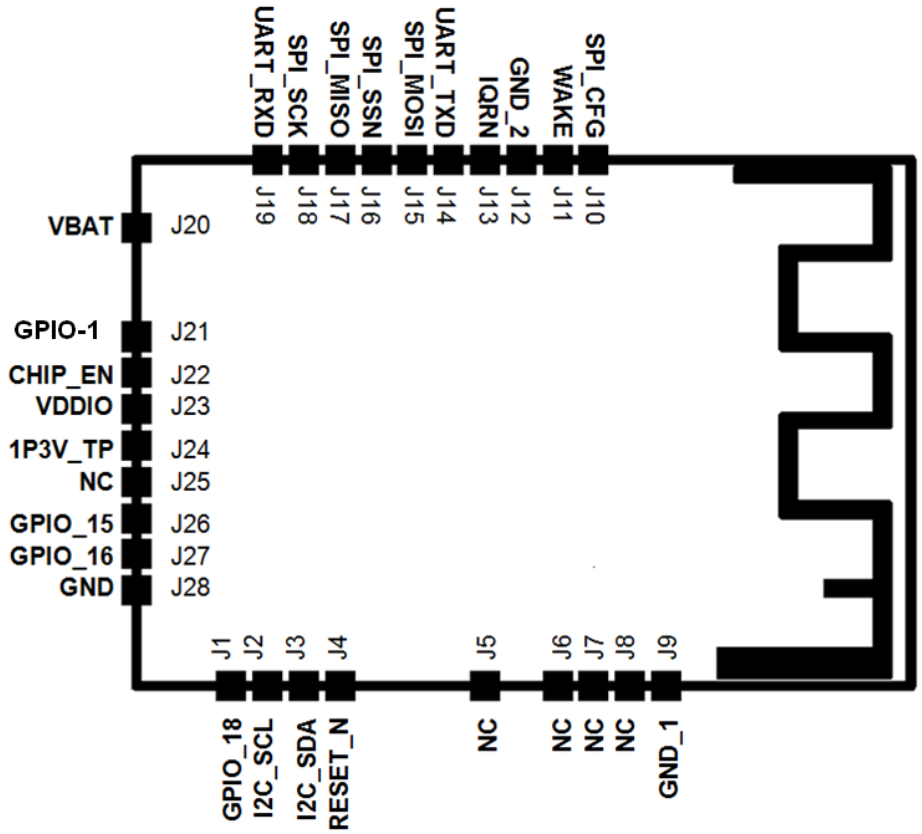


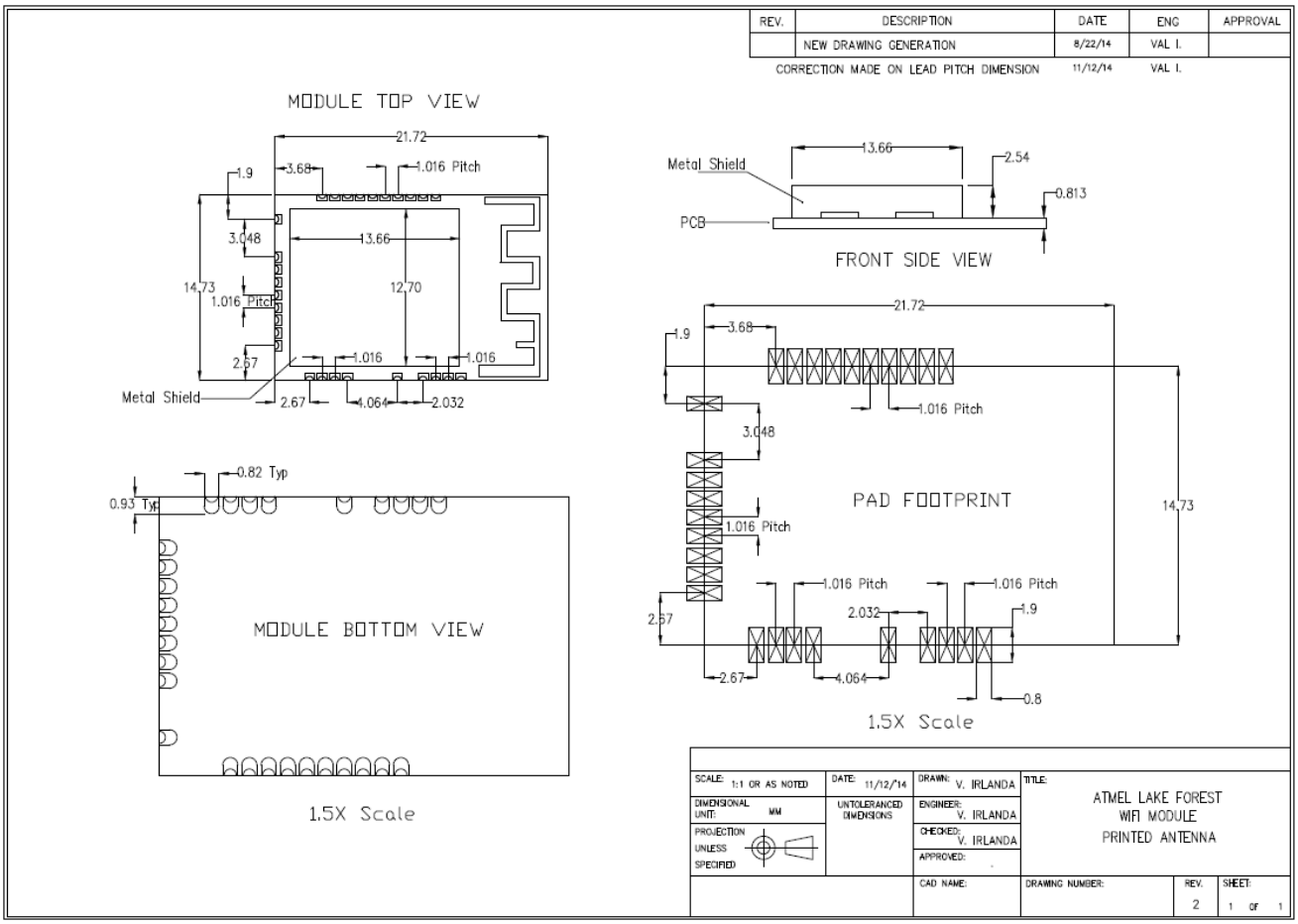
Table 3-1. Pin Description

NO	Name	Type	Description	Programmable Pull-up Resistor
1	GPIO_18	I/O	General purpose I/O.	Yes
2	I2C_SCL	I/O	I^2C Slave Clock. Currently used only for Atmel debug. Not for customer use. Leave unconnected.	Yes
3	I2C_SDA	I/O	I^2C Slave Data. Currently used only for Atmel debug. Not for customer use. Leave unconnected.	Yes
4	RESET_N	I	Active-Low Hard Reset. When asserted to a low level, the module will be placed in a reset state. When asserted to a high level, the module will run normally. Connect to a host output that defaults low at power up. If the host output is tri-stated, add a 1MΩ pull-down resistor to ensure a low level at power up.	No
5	NC	-	No connect	
6	NC	-	No connect	
7	NC	-	No connect	

NO	Name	Type	Description	Programmable Pull-up Resistor
8	NC	-	No connect	
9	GND_1	-	GND	
10	SPI_CFG	I	Tie to VDDIO through a 1MΩ resistor to enable the SPI interface.	No
11	WAKE	I	Host Wake control. Can be used to wake up the module from Doze mode. Connect to a host GPIO.	Yes
12	GND_2	-	GND	
13	IRQN	O	ATWINC1500-MR210PA Device Interrupt output. Connect to host interrupt input pin.	Yes
14	UART_TXD	O	UART Transmit Output from ATWINC1500-MR210P.	Yes
15	SPI_RXD	I	SPI MOSI (Master Out Slave In) pin.	Yes
16	SPI_SSN	I	SPI Slave Select. Active low.	Yes
17	SPI_TXD	O	SPI MISO (Master In Slave Out) pin.	Yes
18	SPI_SCK	I	SPI Clock.	Yes
19	UART_RXD	I	UART Receive input to ATWINC1500-MR210P.	Yes
20	VBATT	-	Battery power supply.	
21	GPIO_1	I	General Purpose I/O.	Yes
22	CHIP_EN	I	Module enable. High level enables module, low level places module in Power Down mode. Connect to a host Output that defaults low at power up. If the host output is tri-stated, add a 1MΩ pull-down resistor to ensure a low level at power up.	No
23	VDDIO	-	I/O Power Supply. Must match host I/O voltage.	
24	1P3V_TP	-	1.3V VDD Core Test Point. Leave unconnected.	
25	NC	-	No connect	
26	GPIO_15	I/O	General purpose I/O.	Yes
27	GPIO_16	I/O	General purpose I/O.	Yes
28	GND_3	-	GND	

3.2 Module Outline Drawing

Figure 3-2. Module Drawings – Top and Bottom Views (unit = mm)



4 Electrical Specifications

4.1 Absolute Ratings

Table 4-1. Voltages

Symbol	Description	Min.	Max.	Unit
VBAT	Input supply Voltage	-0.3	5.0	V
VDDIO	I/O Voltage	-0.3	4.6	V

4.2 Recommended Operating Conditions

Table 4-2. Recommended Operating Conditions

Test conditions: -40ºC - +85ºC				
Symbol	**Min.**	**Typ.**	**Max.**	**Unit**
VBAT	3.0	3.6	4.2	V
VDDIO	2.7	3.3	3.6	V

5 CPU and Memory Subsystems

5.1 Processor

ATWINC1500A has a Cortus APS3 32-bit processor. This processor performs many of the MAC functions, including but not limited to association, authentication, power management, security key management, and MSDU aggregation/de-aggregation. In addition, the processor provides flexibility for various modes of operation, such as STA and AP modes.

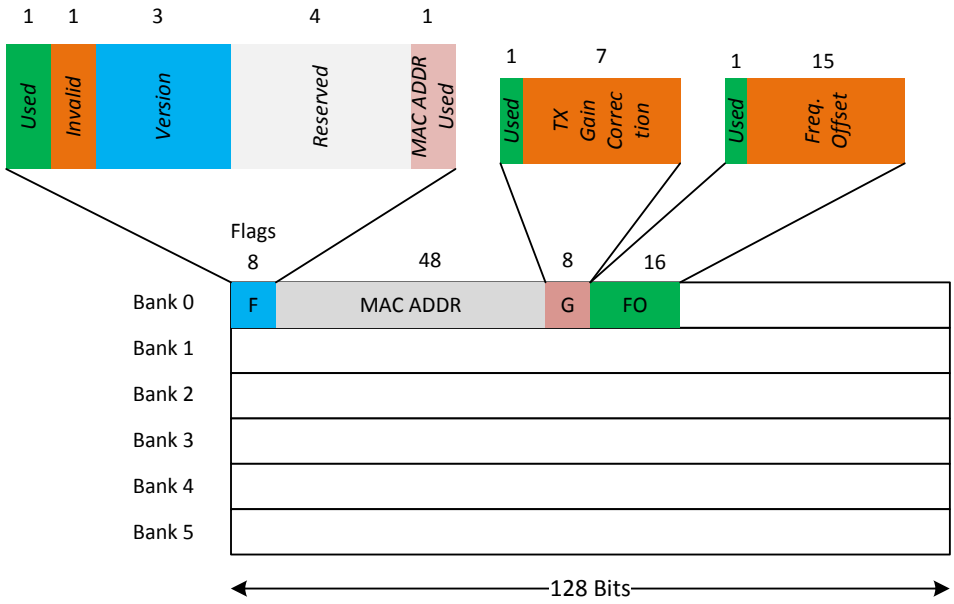
5.2 Memory Subsystem

The APS3 core uses a 128KB instruction/boot ROM along with a 128KB instruction RAM and a 64KB data RAM. ATWINC1500A also has 4Mb of flash memory, which can be used for system software. In addition, the device uses a 128KB shared RAM, accessible by the processor and MAC, which allows the APS3 core to perform various data management tasks on the TX and RX data packets.

5.3 Non-Volatile Memory (eFuse)

ATWINC1500A has 768 bits of non-volatile eFuse memory that can be read by the CPU after device reset. This non-volatile one-time-programmable (OTP) memory can be used to store customer-specific parameters, such as MAC address; various calibration information, such as TX power, crystal frequency offset, etc.; and other software-specific configuration parameters. The eFuse is partitioned into six 128-bit banks. Each bank has the same bit map, which is shown in Figure 5-1. The purpose of the first 80 bits in each bank is fixed, and the remaining 48 bits are general-purpose software dependent bits, or reserved for future use. Since each bank can be programmed independently, this allows for several updates of the device parameters following the initial programming, e.g. updating MAC address. Refer to ATWINC1500A Programming Guide for the eFuse programming instructions.

Figure 5-1. eFuse Bit Map



6 WLAN Subsystem

The WLAN subsystem is composed of the Media Access Controller (MAC) and the Physical Layer (PHY). The following two subsections describe the MAC and PHY in detail.

6.1 MAC

6.1.1 Features

The ATWINC1500A IEEE802.11 MAC supports the following functions:

- IEEE 802.11b/g/n
- IEEE 802.11e WMM QoS EDCA/PCF multiple access categories traffic scheduling
- Advanced IEEE 802.11n features:
  - Transmission and reception of aggregated MPDUs (A-MPDU)
  - Transmission and reception of aggregated MSDUs (A-MSDU)
  - Immediate Block Acknowledgement
  - Reduced Interframe Spacing (RIFS)
- Support for IEEE802.11i and WFA security with key management
  - WEP 64/128
  - WPA-TKIP
  - 128-bit WPA2 CCMP (AES)
- Support for WAPI security
- Advanced power management
  - Standard 802.11 Power Save Mode
  - Wi-Fi Alliance WMM-PS (U-APSD)
- RTS-CTS and CTS-self support
- Supports either STA or AP mode in the infrastructure basic service set mode
- Supports independent basic service set (IBSS)

6.1.2 Description

The ATWINC1500A MAC is designed to operate at low power while providing high data throughput. The IEEE 802.11 MAC functions are implemented with a combination of dedicated datapath engines, hardwired control logic, and a low-power, high-efficiency microprocessor. The combination of dedicated logic with a programmable processor provides optimal power efficiency and real-time response while providing the flexibility to accommodate evolving standards and future feature enhancements.

Dedicated datapath engines are used to implement data path functions with heavy computational. For example, an FCS engine checks the CRC of the transmitting and receiving packets, and a cipher engine performs all the required encryption and decryption operations for the WEP, WPA-TKIP, WPA2 CCMP-AES, and WAPI security requirements.

Control functions which have real-time requirements are implemented using hardwired control logic modules. These logic modules offer real-time response while maintaining configurability via the processor. Examples of hardwired control logic modules are the channel access control module (implements EDCA/HCCA, Beacon TX control, interframe spacing, etc.), protocol timer module (responsible for the Network Access Vector, back-off timing, timing synchronization function, and slot management), MPDU handling module, aggregation/de-aggregation module, block ACK controller (implements the protocol requirements for burst block communication), and TX/RX control FSMs (coordinate data movement between PHY-MAC interface, cipher engine, and the DMA interface to the TX/RX FIFOs).

The MAC functions implemented solely in software on the microprocessor have the following characteristics:

- Functions with high memory requirements or complex data structures. Examples are association table management and power save queuing.
- Functions with low computational load or without critical real-time requirements. Examples are authentication and association.
- Functions which need flexibility and upgradeability. Examples are beacon frame processing and QoS scheduling.

6.2 PHY

6.2.1 Features

The ATWINC1500A IEEE802.11 PHY supports the following functions:

- Single antenna 1x1 stream in 20MHz channels
- Supports IEEE 802.11b DSSS-CCK modulation: 1, 2, 5.5, 11Mbps
- Supports IEEE 802.11g OFDM modulation: 6, 9, 12,18, 24, 36, 48, 54Mbps
- Supports IEEE 802.11n HT modulations MCS0-7, 20MHz, 800 and 400ns guard interval: 6.5, 7.2, 13.0, 14.4, 19.5, 21.7, 26.0, 28.9, 39.0, 43.3, 52.0, 57.8, 58.5, 65.0, 72.2Mbps
- IEEE 802.11n mixed mode operation
- Per packet TX power control
- Advanced channel estimation/equalization, automatic gain control, CCA, carrier/symbol recovery, and frame detection

6.2.2 Description

The ATWINC1500A WLAN PHY is designed to achieve reliable and power-efficient physical layer communication specified by IEEE 802.11 b/g/n in single stream mode with 20MHz bandwidth. Advanced algorithms have been employed to achieve maximum throughput in a real world communication environment with impairments and interference. The PHY implements all the required functions such as FFT, filtering, FEC (Viterbi decoder), frequency and timing acquisition and tracking, channel estimation and equalization, carrier sensing and clear channel assessment, as well as the automatic gain control.

6.3 Radio

Table 6-1. Radio Performance under Typical Conditions: VBAT=3.3V; VDDIO=3.3V; Temp: 25ºC @ RF Pins

Feature	Description
Module Part Number	ATWINC1500-MR210P
WLAN Standard	IEEE 802.11b/g/n, Wi-Fi compliant
Host Interface	SPI, UART
Dimension	L x W x H: 21.72 x 14.73 x 3.5 (typical) mm
Frequency Range	2.412GHz ~ 2.4835GHz (2.4GHz ISM Band)
Number of Channels	11 for North America, 13 for Europe, and 14 for Japan
Modulation	802.11b : DQPSK, DBPSK, CCK 802.11g/n : OFDM /64-QAM,16-QAM, QPSK, BPSK
Output Power[1]	802.11b /11Mbps : 19dBm ± 1dB
	802.11g /54Mbps : 15.5dBm ± 1dB @ EVM -28dB
	802.11n /65Mbps : 13dBm ± 1dB @ EVM -30dB
Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0 PER @ -90dBm ± 1dB
	- MCS=1 PER @ -86dBm ± 1dB
	- MCS=2 PER @ -84dBm ± 1dB
	- MCS=3 PER @ -81.5dBm ± 1dB
	- MCS=4 PER @ -78dBm ± 1dB
	- MCS=5 PER @ -74dBm ± 1dB
	- MCS=6 PER @ -72.5dBm ± 1dB
	- MCS=7 PER @ -71.5dBm ± 1dB
Receive Sensitivity (11g) @10% PER	- 6Mbps PER @ -91dBm ± 1dB
	- 9Mbps PER @ -89dBm ± 1dB
	- 12Mbps PER @ -88.5dBm ± 1dB
	- 18Mbps PER @ -86.5dBm ± 1dB
	- 24Mbps PER @ -84dBm ± 1dB
	- 36Mbps PER @ -78.5dBm ± 1dB
	- 48Mbps PER @ -77dBm ± 1dB
	- 54Mbps PER @ -75dBm ± 1dB
Receive Sensitivity (11b)	- 1Mbps PER @ -98dBm ± 1dB
	- 2Mbps PER @ -95dBm ± 1dB
	- 5.5Mbps PER @ -93dBm ± 1dB
@8% PER	- 11Mbps PER @ -89dBm ± 1dB
Data Rate	802.11b : 1, 2, 5.5, 11Mbps
	802.11g : 6, 9, 12, 18, 24, 36, 48, 54Mbps

Feature	Description
Data Rate (20MHz ,normal GI,800ns)	802.11n: 6.5, 13, 19.5, 26, 39, 52, 58.5, 65Mbps
Data Rate (20MHz ,short GI,400ns)	802.11n : 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65,72.2Mbps
Maximum Input Level	802.11b : 0dBm typical
	802.11g/n : -5dBm typical
Operating temperature[2]	-40°C to 85°C
Storage temperature	-40°C to 85°C
Humidity	Operating Humidity 10% to 95% Non-Condensing Storage Humidity 5% to 95% Non-Condensing

Notes: 1. Measured at 802.11 spec compliant EVM/Spectral Mask.
2. RF performance guaranteed for Temp range -30 to 85deg. 1dB derating in performance at -40deg.

7 External Interfaces

7.1 SPI Interface

7.1.1 Overview

ATWINC1500-MR210PA has a Serial Peripheral Interface (SPI) that operates as a SPI slave. The SPI interface can be used for control and for serial I/O of 802.11 data. The SPI pins are mapped as shown in Table 7-1. The SPI is a full-duplex slave-synchronous serial interface that is available immediately following reset when pin 10 (SPI_CFG) is tied to VDDIO.

Table 7-1. SPI Interface Pin Mapping

Pin #	SPI Function
10	CFG: Must be tied to VDDIO
16	SSN: Active Low Slave Select
15	MOSI(RXD): Serial Data Receive
18	SCK: Serial Clock
17	MISO(TXD): Serial Data Transmit

When the SPI is not selected, i.e., when SSN is high, the SPI interface will not interfere with data transfers between the serial-master and other serial-slave devices. When the serial slave is not selected, its transmitted data output is buffered, resulting in a high impedance drive onto the MISO line.

The SPI interface responds to a protocol that allows an external host to read or write any register in the chip as well as initiate DMA transfers.

The SPI SSN, MOSI, MISO, and SCK pins of the ATWINC1500-MR210PA have internal programmable pull-up resistors (See Section 10.1). These resistors should be programmed to be disabled. Otherwise, if any of the SPI pins are driven to a low level while the ATWINC1500-MR210PA is in the low power sleep state, current will flow from the VDDIO supply through the pull-up resistors, increasing the current consumption of the module.

7.1.2 SPI Timing

The SPI timing is provided in Figure 7-1 and Table 7-2.

Figure 7-1. SPI Timing Diagram (SPI Mode CPOL=0, CPHA=0)

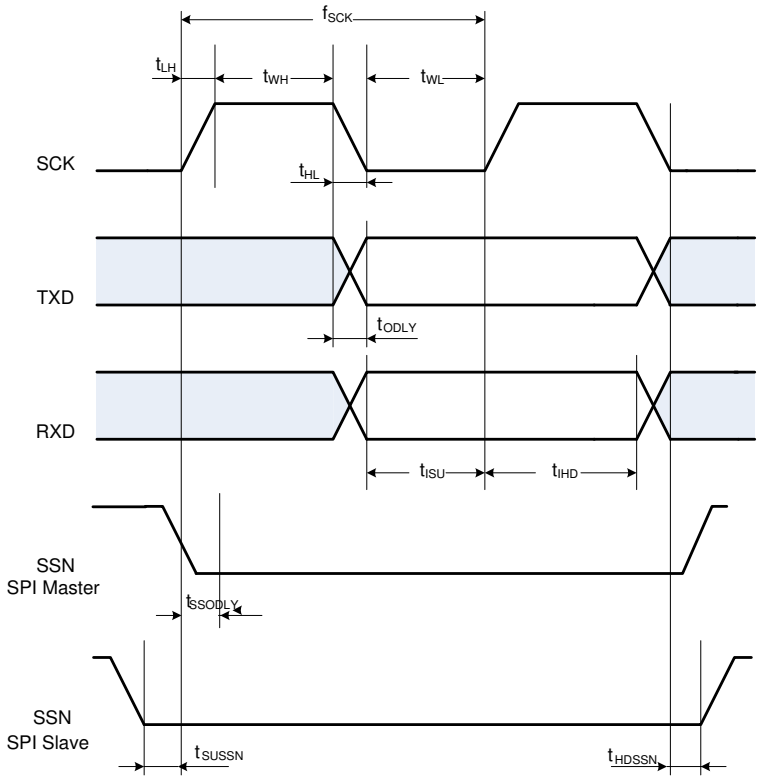


Table 7-2. SPI Slave Timing Parameters

Parameter	Symbol	Min	Max	Units	Remarks
Clock Input Frequency	f_{SCK}		48	MHz	
Clock Low Pulse Width	t_{WL}	15		ns	
Clock High Pulse Width	t_{WH}	15		ns	
Clock Rise Time	t_{LH}		10	ns	
Clock Fall Time	t_{HL}		10	ns	
Input Setup Time	t_{ISU}	5		ns	
Input Hold Time	t_{IHD}	5		ns	
Output Delay	t_{ODLY}	0	20	ns	
Slave Select Setup Time	t_{SUSSN}	5		ns	
Slave Select Hold Time	t_{HDSSN}	5		ns	

7.2 UART Interface

The ATWINC1500-MR210PA has a Universal Asynchronous Receiver/Transmitter (UART) interface available on pins J14 and J19. It can be used for control or data transfer if the baud rate is sufficient for a given application. The UART is compatible with the RS-232 standard, where ATWINC1500-MR210PA operates as Data Terminal Equipment (DTE). It has a two-pin RXD/TXD interface.

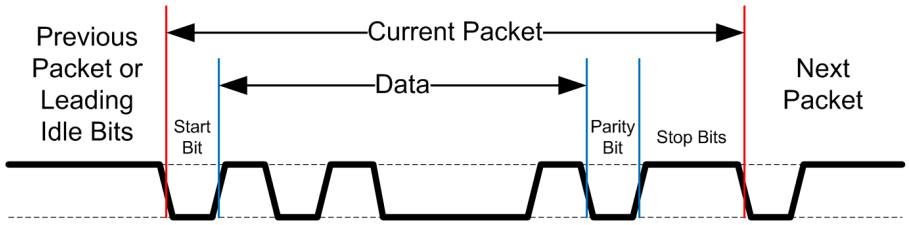
The UART features programmable baud rate generation with fractional clock division, which allows transmission and reception at a wide variety of standard and non-standard baud rates. The UART input clock is selectable between 10MHz, 5MHz, 2.5MHz, and 1.25MHz. The clock divider value is programmable as 13 integer bits and 3 fractional bits (with 8.0 being the smallest recommended value for normal operation). This results in the maximum supported baud rate of 10MHz/8.0 = 1.25MBd.

The UART can be configured for seven or eight bit operation, with or without parity, with four different parity types (odd, even, mark, or space), and with one or two stop bits. It also has Rx and Tx FIFOs, which ensure reliable high speed reception and low software overhead transmission. FIFO size is 4 x 8 for both Rx and Tx direction. The UART also has status registers showing the number of received characters available in the FIFO and various error conditions, as well the ability to generate interrupts based on these status bits.

An example of UART receiving or transmitting a single packet is shown in Figure 7-2. This example shows 7-bit data (0x45), odd parity, and two stop bits.

See the ATWINC1500-MR210PA Programming Guide for information on configuring the UART.

Figure 7-2. Example of UART Rx of Tx Packet



7.3 Wi-Fi/Bluetooth Coexistence

ATWILC1000A supports 2-wire and 3-wire Wi-Fi/Bluetooth Coexistence signaling conforming to the IEEE 802.15.2-2003 standard, Part 15.2. The type of coexistence interface used (2 or 3 wire) is chosen to be compatible with the specific Bluetooth device used in a given application. Table 7-3 shows a usage example of the 2-wire interface using the GPIO3 and GPIO4 pins; 3-wire interface using the GPIO3, GPIO4, and GPIO5 pins; for more specific instructions on configuring Coexistence refer to ATWILC1000A Programming Guide.

Table 7-3. Coexistence Pin Assignment Example

Pin Name	Function	Target	Pin #	2-wire	3-wire
GPIO3	BT_Req	BT is requesting to access the medium to transmit or receive. Goes high on TX or RX slot	28	Used	Used
GPIO4	BT_Pri	Priority of the BT packets in the requested slot. High to indicate high priority and low for normal.	29	Not Used	Used
GPIO5	WL_Act	Device response to the BT request. High - BT_req is denied and BT slot blocked.	30	Used	Used
GPIO6	Ant_SW	Direct control on Antenna (coex bypass)	31	Optional	Optional

8 Power Consumption

8.1 Description of Device States

ATWILC1000A has several Devices States:

- ON_Transmit – Device is actively transmitting an 802.11 signal
- ON_Receive – Device is actively receiving an 802.11 signal
- ON_Doze – Device is on but is neither transmitting nor receiving
- Power_Down – Device core supply off (Leakage)

8.2 Controlling the Device States

Table 8-1 shows how to switch between the device states using the following:

- CHIP_EN – Device pin (pin #23) used to enable DC/DC Converter
- VDDIO – I/O supply voltage from external supply

Table 8-1. Device States

Device State	CHIP_EN	VDDIO	Power Consumption[1]	
			I_{VBATT}	I_{VDDIO}
ON_Transmit	VDDIO	On	230mA @ 18dBm	29mA
ON_Receive	VDDIO	On	68mA	29mA
ON_Doze	VDDIO	On	850[2]µA	<10µA
Power_Down	GND	On	<0.5µA	<0.2µA

Notes: 1. Conditions: VBAT @ 3.6v, IO@1.8V.
2. 850µA Doze current is for ATWINC1500-MR210P module which uses an external DC-DC chip. Core ATWINC1500 Doze is 240µA.

8.3 Restrictions for Power States

When no power supplied to the device, i.e., the DC/DC Converter output and VDDIO are both off (at ground potential). In this case, a voltage cannot be applied to the device pins because each pin contains an ESD diode from the pin to supply. This diode will turn on when voltage higher than one diode-drop is supplied to the pin.

If a voltage must be applied to the signal pads while the chip is in a low power state, the VDDIO supply must be on, so the SLEEP or Power_Down state must be used.

Similarly, to prevent the pin-to-ground diode from turning on, do not apply a voltage that is more than one diode-drop below ground to any pin.

8.4 Power-Up/Down Sequence

The power-up/down sequence for ATWINC1500A is shown in Figure 8-1. The timing parameters are provided in Table 8-2.

Figure 8-1. Power Up/Down Sequence

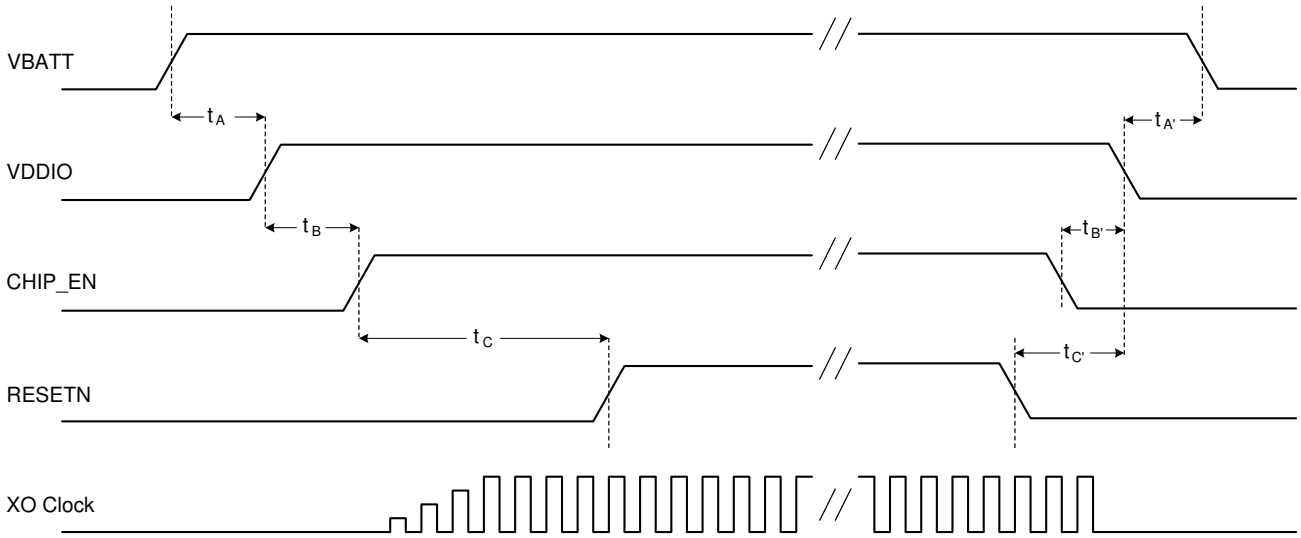


Table 8-2. Power-Up/Down Sequence Timing

Parameter	Min	Max	Units	Description	Notes
t_A	0		ms	VBATT rise to VDDIO rise	VBATT and VDDIO can rise simultaneously or can be tied together. VDDIO must not rise before VBATT.
t_B	0		ms	VDDIO rise to CHIP_EN rise	CHIP_EN must not rise before VDDIO. CHIP_EN must be driven high or low, not left floating.
t_C	5		ms	CHIP_EN rise to RESETN rise	This delay is needed because XO clock must stabilize before RESETN removal. RESETN must be driven high or low, not left floating.
$t_{A'}$	0		ms	VDDIO fall to VBATT fall	VBATT and VDDIO can fall simultaneously or can be tied together. VBATT must not fall before VDDIO.
$t_{B'}$	0		ms	CHIP_EN fall to VDDIO fall	VDDIO must not fall before CHIP_EN. CHIP_EN and RESETN can fall simultaneously.
$t_{C'}$	0		ms	RESETN fall to VDDIO fall	VDDIO must not fall before RESETN. RESETN and CHIP_EN can fall simultaneously.

8.5 Digital I/O Pin Behavior during Power-Up Sequences

Table 8-3 represents digital IO Pin states corresponding to device power modes.

Table 8-3. Digital I/O Pin Behavior in Different Device States

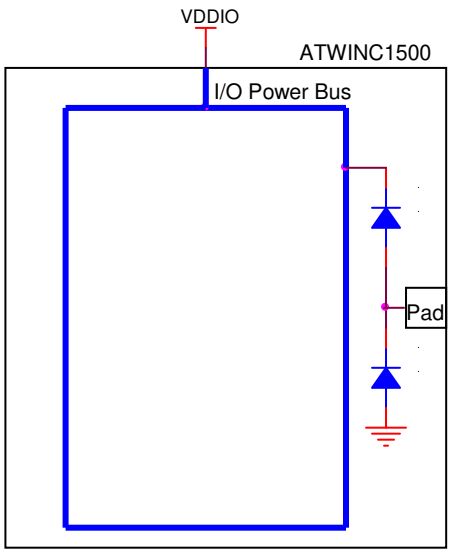
Device State	VDDIO	CHIP_EN	RESETN	Output Driver	Input Driver	Pull-Up/Down Resistor (96kΩ)
Power Down: core supply off	High	Low	Low	Disabled (Hi-Z)	Disabled	Disabled

Device State	VDDIO	CHIP_EN	RESETN	Output Driver	Input Driver	Pull-Up/Down Resistor (96kΩ)
Power-On Reset: core supply on, hard reset on	High	High	Low	Disabled (Hi-Z)	Disabled	Enabled
Power-On Default: core supply on, device out of reset but not programmed yet	High	High	High	Disabled (Hi-Z)	Enabled	Enabled
On Sleep/ On Transmit/ On Receive: core supply on, device programmed by firmware	High	High	High	Programmed by firmware for each pin: Enabled or Disabled	Opposite of Output Driver state	Programmed by firmware for each pin: Enabled or Disabled

9 VDDIO Load Switch

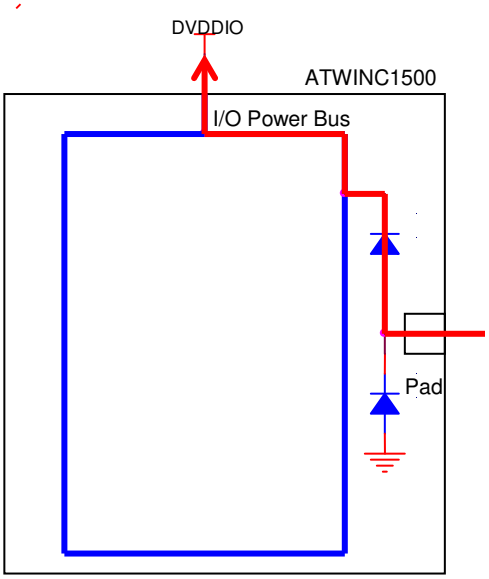
The ATWINC1500-MR210PA module is designed with a load switch in series with the VDDIO supply. The load switch is controlled by the Chip_En pin of the module (Module pin 22). When Chip_En is high, the load switch is turned on. When Chip_En is low the load switch is open and VDDIO is disconnected from the ATWINC1500-MR210P. When the VDDIO supply to the ATWINC1500-MR210PA is disconnected it is important that none of the pins to the ATWINC1500-MR210PA is in a high state. Figure 9-1 shows the ESD structure of the pins of the ATWINC1500 and Figure 9-2 shows the current path through the ESD diode from a pin that is being driven high to the VDDIO supply of the device. In effect, if VDDIO is disconnected from the external power supply and a high level is driven on to a pad of the device, the device will be powered up through the pad.

Figure 9-1. TWINC1500 Pad ESD Structure



This shows why it is important that any time Chip_En to the module is low, all pins interfacing to the module must not be driven or pulled high. They should either be set to a low level or high impedance state. This means that if any external pull-up resistors are attached to any pins they should be disconnected from the supply when Chip_En is low.

Figure 9-2. Current Path through ESD Diode



10 Notes On Interfacing to the ATWINC1500-MR210P

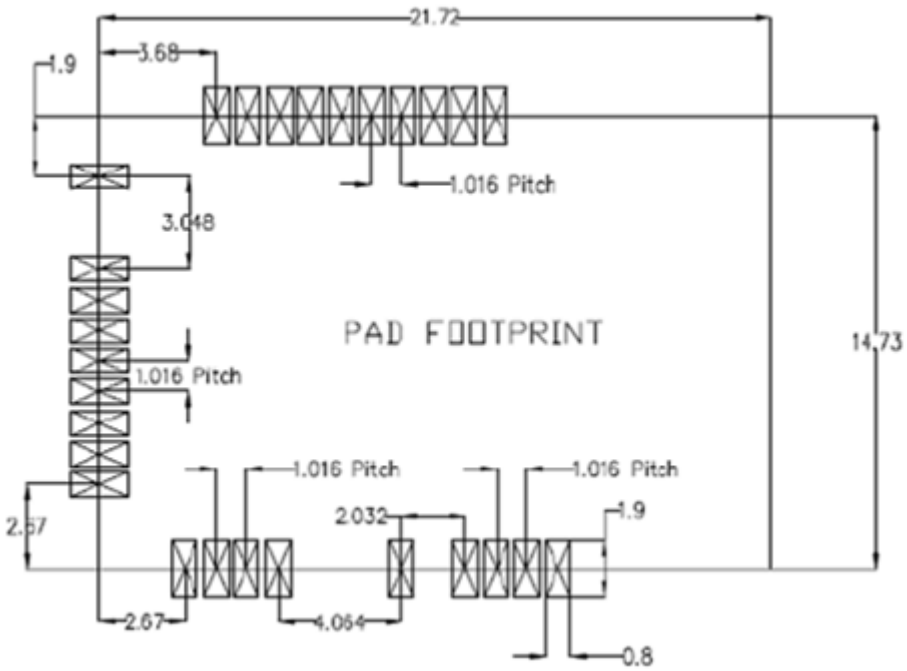
10.1 Programmable Pull Up Resistors

The ATWINC1500-MR210PA provides programmable pull-up resistors on various pins. The purpose of these resistors is to keep any unused input pins from floating which can cause excess current to flow through the input buffer from the VDDIO supply. Any unused module pin on the ATWINC1500-MR210PA should leave these pull-up resistors enabled so the pin will not float. The default state at power up is for the pull-up resistor to be enabled. However, any pin which is used should have the pull-up resistor disabled. The reason for this is that if any pins are driven to a low level while the ATWINC1500-MR210PA is in the low power sleep state, current will flow from the VDDIO supply through the pull-up resistors, increasing the current consumption of the module. Since the value of the pull-up resistor is approximately 100KΩ, the current through any pull-up resistor that is being driven low will be VDDIO/100K. For VDDIO = 3.3V, the current through each pull-up resistor that is driven low would be approximately 3.3V/100K = 33µA. Pins which are used and have had the programmable pull-up resistor disabled should always be actively driven to either a high or low level and not be allowed to float.

See the ATWINC1500-MR210PA Programming Guide for information on enabling/disabling the programmable pull up resistors.

11 Recommended Footprint (Unit: mm)

Figure 11-1. Footprint Drawing



12 RF Performance Placement Guidelines

It is critical to follow the recommendations listed below to achieve the best RF performance:

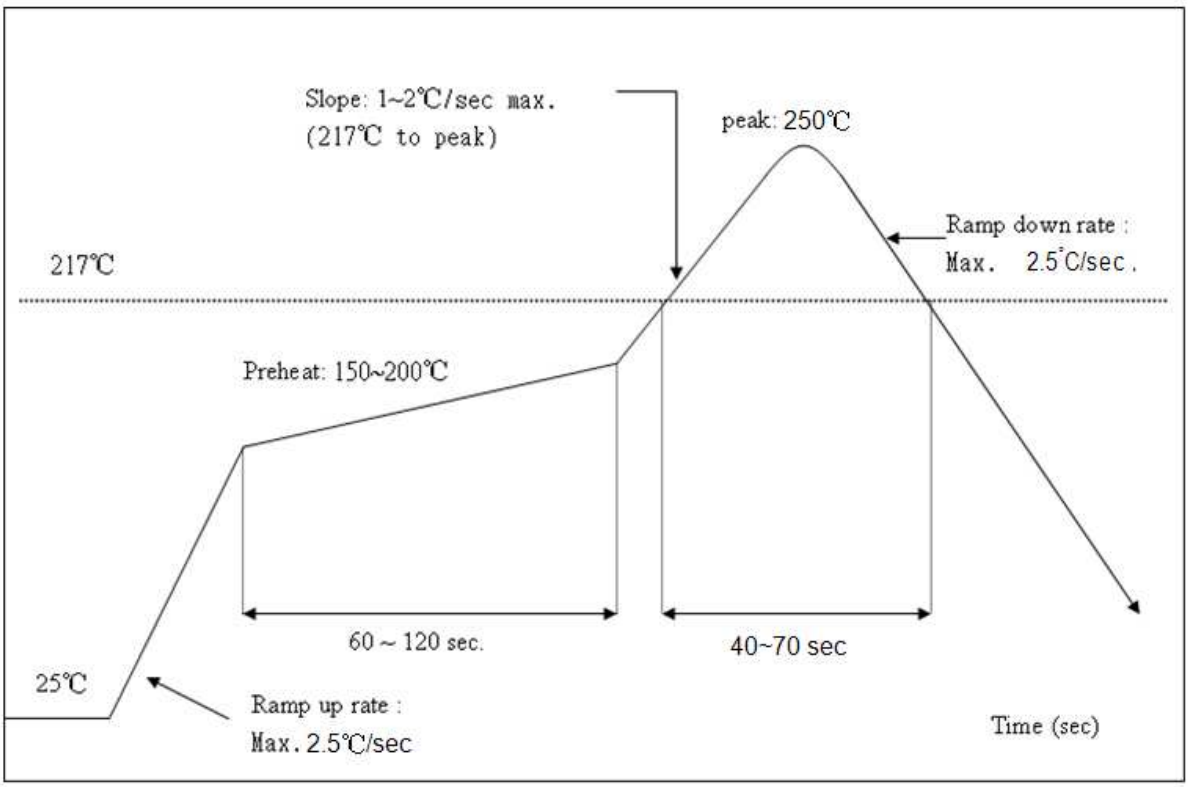
- Module must be placed on main board - printed antenna area must overlap with the carrier board. The portion of the module containing the antenna should not stick out over the edge of the main board. The antenna is de-signed to work properly when it is sitting directly on top of a 1.5mm thick printed circuit board.
- If the module is placed at the edge of the main board, a minimum 22mm by 5mm area directly under the antenna must be clear of all metal on all layers of the board. “In-land” placement is acceptable; however deepness of keep-out area must grove to: module edge to main board edge plus 5mm. DO NOT PLACE MODULE IN THE MIDDLE OF THE MAIN BOARD OR FAR AWAY FROM THE MAIN BOARD EDGE.
- Keep away from antenna, as far as possible, large metal objects to avoid electromagnetic field blocking.
- Do not enclose the antenna within a metal shield.
- Keep any components which may radiate noise or signals within the 2.4GHz – 2.5GHz frequency band far away from the antenna or better yet, shield those components. Any noise radiated from the main board in this frequency band will degrade the sensitivity of the module.
- Contact Atmel for assistance if any other placement is required.

13 Recommended Reflow Profile

Referred to IPC/JEDEC standard. Peak Temperature: <250°C.

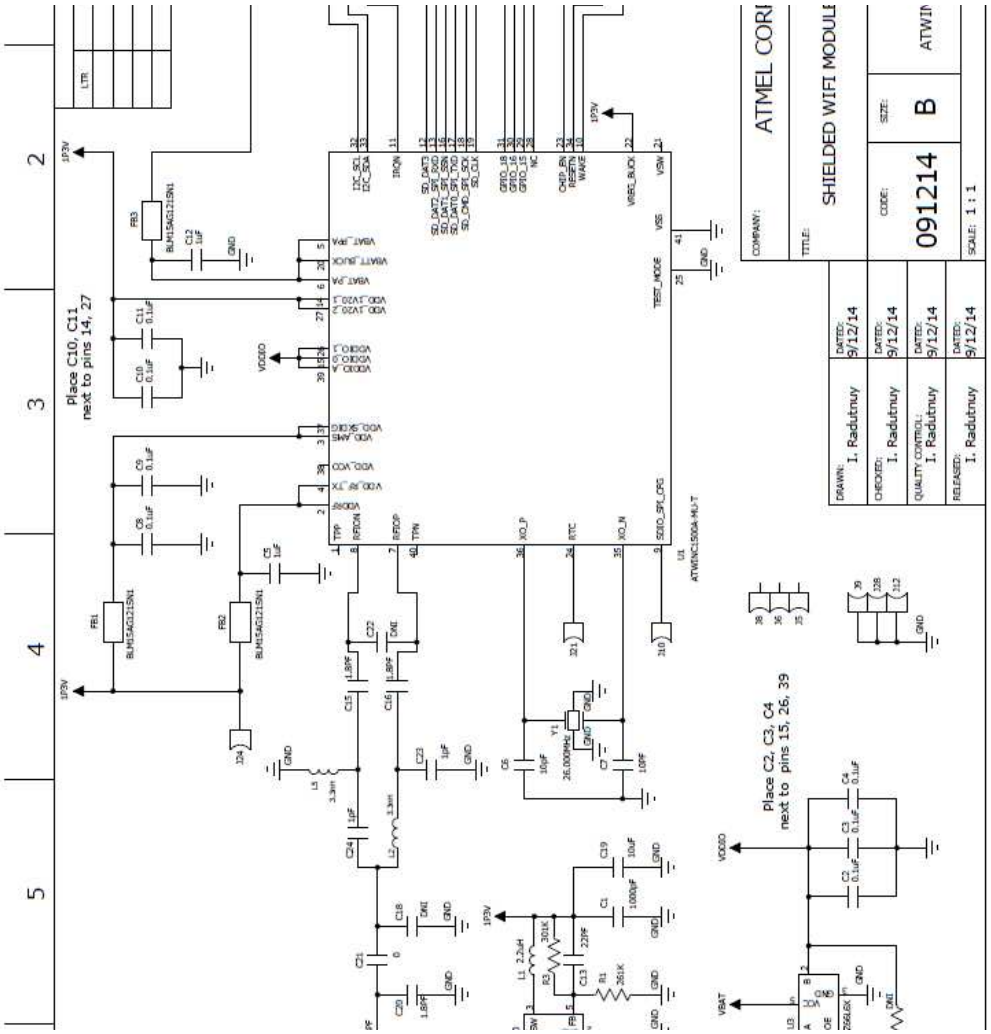
Number of Times: two times maximum.

Figure 13-1. Typical Reflow Profile



14 Module Schematic

Figure 14-1. ATWINC1500-MR210PA Schematic



15 Module Bill of Materials (BOM)

Table 15-1. ATWINC1500-MR210PA BOM

WiFi shielded module with DC/DC, discrete balun, load switch and printed antenna Revised: Friday, September 11, 2014

ATWINC1500-MR210P Revision: A

Item	Qty	Reference	Value	Description	Manufacturer	Part Number	Footprint
1	2	C5,C12	1.0uF	CAP,CER,1.0uF,20%,X5R,0402,6.3V	Panasonic	ECJ-0EB0J105M	CS0402
2	2	C1,C14	1000PF	CAP CER 1000PF 50V 10% X7R 0402	Murata	GRM155R71H102KA01D	CS0402
3	7	C2,C3,C4,C8,C9,C10, C11	0.1uF	CAP,CER,0.1uF,10%,X5R,0402,10V	AVX	0402ZD104KAT2A	CS0402
4	1	C13	22pF	CAP,CER,22pF,5%,NPO,0402,50V	Murata	GRM1555C1H220JZ01	CS0402
5	1	C17	4.7uF	CAP CER 4.7UF 4V 20% X5R 0402	Murata	GRM155R60G475ME47D	CS0402
6	2	C23,C24	1pF	CAP CER 1PF 50V NP0 0201	Murata	GRM0335C1H1R0CA01D	CS0201
7	2	C6,C7	10PF	CAP CER 10PF 50V 1% NP0 0402	Murata	GRM1555C1H100FA01D	CS0402
8	2	C15,C16	1.8PF	CAP CER 1.8PF 50V NP0 0201	Murata	GRM0335C1H1R8CA01D	CS0201
9	1	C19	10uF	CAP CER 10UF 4V 20% X5R 0402	Murata	GRM155R60G106ME44D	CS0402
10	1	C21	0	RES 0.0 OHM 1/20W JUMP 0201 SMD	Panasonic	ERJ-1GN0R00C	RS0201
11	1	C20	1.8PF	CAP CER 1.8PF 50V NP0 0201	Murata	GRM0335C1H1R8CA01D	CS0201
12		C18,C22	DNI				
13	3	FB1,FB2,FB3	BLM15AG121SN1	FERRITE,120 OHM @100MHz,0402	Murata	BLM15AG121SN1	FBS0402
14	1	L1	2.2uH	POWER INDUCTOR,2.2uH,20%,1250mA,0.22ohms,0603	Murata	LQM18PN2R2MFRL	LPS0603
15	2	L2,L5	3.3nH	INDUCTOR 3.3+/-0.2NH 750MA 0201	Murata	LQP03TN3N3C02D	LS0201
16	1	R1	261k	RES 261K OHM 1/10W 1% 0402 SMD	Panasonic	ERJ-2RKF2613X	RS0402
17	1	R2	6.8PF	CAP,CER,6.8pF,NPO,0402,50V	Murata	GRM1555C1H6R8CA01	CS0402
18	1	R3	301k	RES 301K OHM 1/10W 1% 0402 SMD	Panasonic	ERJ-2RKF3013X	RS0402
19		R4	DNI				
20	1	U1	ATWINC1500A-MU	IC, WiFi, 40QFN	Atmel	ATWINC1500A-MU	40QFN
21	1	U2	FT440Aa	1.5MHz, 600mA, Synchronous Step-Down Converter	FMD	FT440Aa	SOT23-5
22	1	U3	NC7SZ66L6X	IC BUS SWITCH SGL SPST 6MICROPAK	Fairchild	NC7SZ66L6X	6-UFDFN
23	1	Y1	26.000MHz	CRYSTAL 26MHZ 10PF SMD	Abracon	ABM10-26.000MHZ-D30-T3	4 SMD
24	1	PCB	-	ATWINC1500-MR210PA	Createk		
25	1	Shield	-	Metal Shield	Createk	NMI RF Shield rev1	

Revision A -Initial release to production.

16 Application Schematic

Table 16-1. Application Schematic