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ATWINC15x0-MR210xB

IEEE 802.11 b/g/n SmartConnect IoT Module

Description

The ATWINC15x0-MR210xB is a low-power consumption 802.11 b/g/n IoT (Internet of Things) module, which is specifically optimized for low-power IoT applications. The module integrates Power Amplifier, LNA, Switch, Power Management, and a choice of printed antenna or a micro co-ax (u.FL) connector for an external antenna resulting in a small form factor (21.7x14.7x2.1mm) design. With seamless roaming capabilities and advanced security, it could be interoperable with various vendors' 802.11 b/g/n access points in wireless LAN. The module provides SPI ports to interface with a host controller.

Note that all references to the ATWINC15x0-MR210xB module includes all the module devices listed below unless otherwise noted:

- ATWINC1500-MR210PB
- ATWINC1500-MR210UB
- ATWINC1510-MR210PB
- ATWINC1510-MR210UB

Features

- IEEE® 802.11 b/g/n 20MHz (1x1) solution
- Single spatial stream in 2.4GHz ISM band
- Integrated Transmit/Receive switch
- Integrated PCB antenna or u.FL micro co-ax connector for external antenna
- Superior Sensitivity and Range via advanced PHY signal processing
- Advanced Equalization and Channel Estimation
- Advanced Carrier and Timing Synchronization
- Wi-Fi Direct and Soft-AP support
- Supports IEEE 802.11 WEP, WPA, WPA2 Security
- Superior MAC throughput via hardware accelerated two-level A-MSDU/A-MPDU frame aggregation and block acknowledgment
- On-chip memory management engine to reduce host load
- SPI host interface
- Operating temperature range of -40°C to +85°C. RF performance guaranteed at room temperature of 25ºC with a 2-3db change at boundary conditions.
- I/O operating voltage of 2.7V to 3.6V
- Built in 26MHz Crystal
- Integrated Flash memory for system software
- Power Save Modes
  - 4µA Power Down mode typical at 3.3V I/O

  - 380µA Doze mode with chip settings preserved (used for beacon monitoring)[1]
  - On-chip low power sleep oscillator
  - Fast host wake-up from Doze mode by a pin or SPI transaction
- Fast Boot Options
  - On-chip Boot ROM (Firmware instant boot)
  - SPI flash boot (firmware patches and state variables)
  - Low-leakage on-chip memory for state variables
  - Fast AP Re-Association (150ms)
- On-Chip Network Stack to offload MCU
  - Integrated Network IP stack to minimize host CPU requirements
  - Network features TCP, UDP, DHCP, ARP, HTTP, TLS, and DNS
  - Hardware accelerators for Wi-Fi and TLS security to improve connection time
- Hardware accelerator for IP checksum
- Hardware accelerators for OTA security
- Small footprint host driver
- Wi-Fi Alliance® certifications for Connectivity and Optimizations
  - ID: WFA61069

Note: 1 See Power Consumption section 8 for module power modes.

Table of Contents

1. Ordering Information and Module Marking

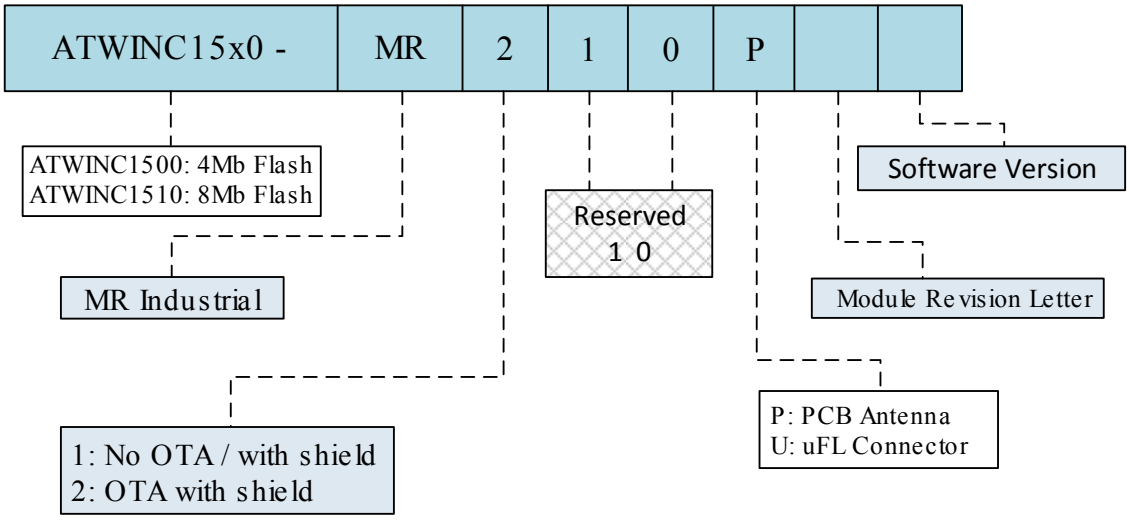
Following table describes the ordering details of the ATWINC15x0-MR210xB modules.

Table 1-1. Ordering Details

Model Number	Ordering Code	Package Dimension	No. of Pins	Description	Regulatory Certification
ATWINC1500-MR210PB	ATWINC1500-MR210PB1952	21.7x14.7x2.1mm	28	Certified Module with ATWINC1500B chip (4Mb Flash) and PCB printed antenna	FCC, IC, CE
ATWINC1500-MR210UB	ATWINC1500-MR210UB1952	21.7x14.7x2.1mm	28	Certified Module with ATWINC1500B chip (4Mb Flash) and u.FL connector	FCC, IC
ATWINC1510-MR210PB	ATWINC1510-MR210PB1952	21.7x14.7x2.1mm	28	Certified Module with ATWINC1510B chip (8Mb Flash) and PCB printed antenna	FCC, IC, CE
ATWINC1510-MR210UB	ATWINC1510-MR210UB1952	21.7x14.7x2.1mm	28	Certified Module with ATWINC1510B chip (8Mb Flash) and u.FL connector	Planned

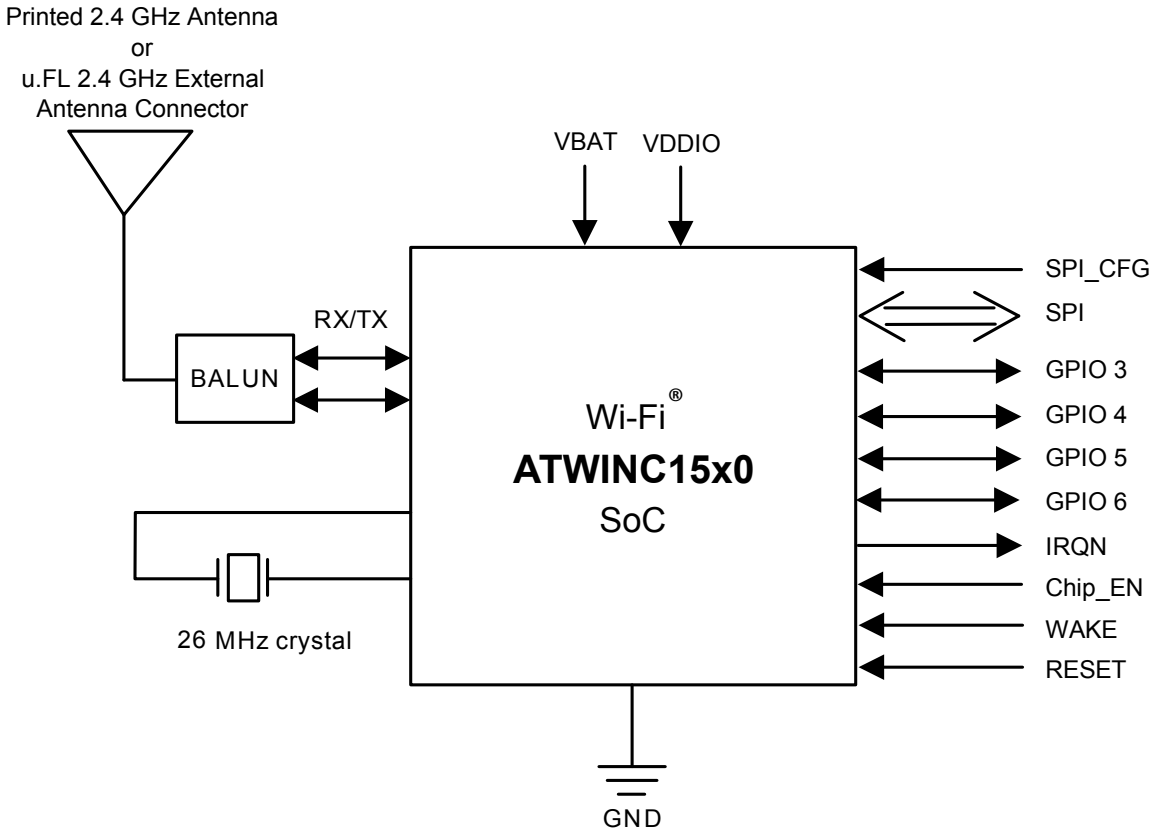
Following figure illustrates the ATWINC15x0-MR210xB modules marking information .

Figure 1-1. Marking Information



2. Block Diagram

Figure 2-1. ATWINC15x0-MR210xB Module Block Diagram



3. Pin Description

Figure 3-1. Pin Diagram

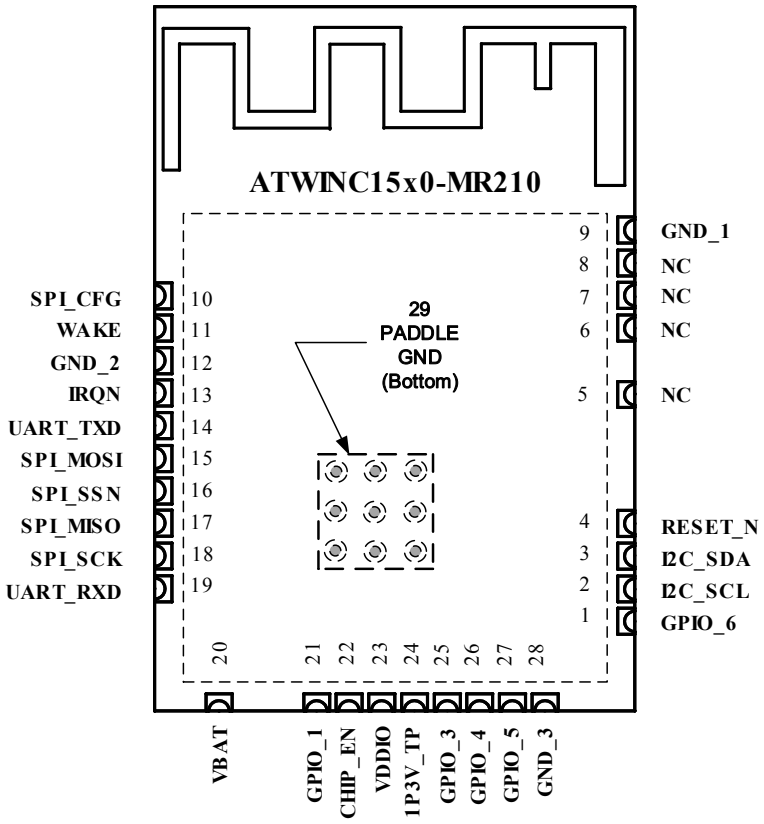


Table 3-1. ATWINC15x0-MR210xB Pin Description

Pin #	Name	Type	Description	Programmable pull-up resistor
1	GPIO_6	I/O	General purpose I/O.	Yes
2	I2C_SCL	I/O	I2C Slave Clock. Currently used only for development debug. Leave unconnected.	Yes
3	I2C_SDA	I/O	I2C Slave Data. Currently used only for development debug. Leave unconnected.	Yes
4	RESET_N	I	Active-Low Hard Reset. When this pin is asserted low, the module will be placed in the reset state. When this pin is asserted high, the module will be out of Reset and will function normally. Connect to a host output that defaults low at power up. If the host output is tri-stated, add a 1MΩ pull-down resistor to ensure a low level at power up.	No
5	NC	-	No connect.	
6	NC	-	No connect.	

Pin #	Name	Type	Description	Programmable pull-up resistor
7	NC	-	No connect.	
8	NC	-	No connect.	
9	GND_1	-	GND.	
10	SPI_CFG	I	Tie to VDDIO through a 1MΩ resistor to enable the SPI interface.	No
11	WAKE	I	Host Wake control. Can be used to wake up the module from Doze mode. Connect to a host GPIO.	Yes
12	GND_2	-	GND.	
13	IRQN	O	ATWINC15x0-MR210xB Device Interrupt output. Connect to host interrupt input pin.	Yes
14	UART_TXD	O	UART Transmit Output from ATWINC15x0-MR210xB Added debug.	Yes
15	SPI_RXD	I	SPI MOSI (Master Out Slave In) pin.	Yes
16	SPI_SSN	I	SPI Slave Select. Active low.	Yes
17	SPI_TXD	O	SPI MISO (Master In Slave Out) pin.	Yes
18	SPI_SCK	I	SPI Clock.	Yes
19	UART_RXD	I	UART Receive input to ATWINC15x0-MR210xB. Added debug.	Yes
20	VBATT	-	Battery power supply.	
21	GPIO_1/RTC	I	General Purpose I/O / RTC.	Yes
22	CHIP_EN	I	Module enable. High level enables the module; low-level places module in Power Down mode. Connect to a host Output that defaults low at power up. If the host output is tri-stated, add a 1MΩ pull-down resistor to ensure a low level at power up.	No
23	VDDIO	-	I/O Power Supply. Must match host I/O voltage.	
24	1P3V_TP	-	1.3V VDD Core Test Point. Decouple with 10µF, and 0.01µF to GND.	
25	GPIO_3	I/O	General purpose I/O.	
26	GPIO_4	I/O	General purpose I/O.	Yes
27	GPIO_5	I/O	General purpose I/O.	Yes
28	GND_3	-	GND.	
29	PADDLE GND	-	GND.	

4. Electrical Specification Recommended Operating Conditions

4.1 Absolute Maximum Ratings

Absolute maximum ratings for the ATWINC15x0-MR210xB modules are listed below.

Table 4-1. Conditions

Symbol	Description	Min.	Max.	Unit
VBATT	Input supply voltage	-0.3	5.0	V
VDDIO	I/O voltage	-0.3	4.2	V
Operating Temperature		-40	+85	ºC

Caution: Stresses listed under "**Absolute Maximum Ratings**" may cause permanent damage to the device. This is a stress rating only. The functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect the device reliability.

4.2 Recommended Operating Conditions

Table 4-2. Recommended Operating Conditions

Symbol	Min.	Typ.	Max.	Unit
VBATT	3.0	3.3	4.2	V
VDDIO	2.7	3.3	3.6	V

Note: 1. Test Conditions: -40ºC - +85ºC

5. CPU and Memory Subsystems

5.1 Processor

The ATWINC15x0-MR210xB modules have a Cortus APS3 32-bit processor. This processor performs many of the MAC functions, including but not limited to the association, authentication, power management, security key management, and MSDU aggregation/de-aggregation. In addition, the processor provides flexibility for various modes of operation, such as STA and AP modes.

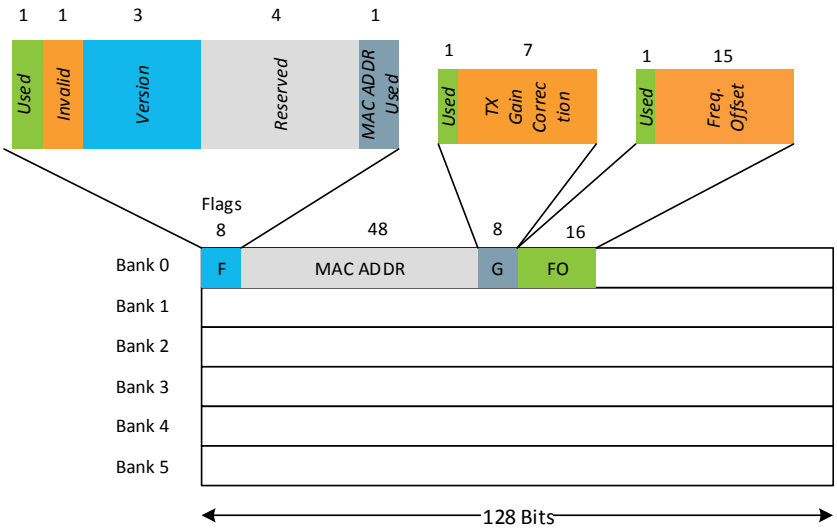
5.2 Memory Subsystem

The APS3 core uses a 128KB instruction/boot ROM along with a 160KB instruction RAM and a 64KB data RAM. The ATWINC15x0-MR210xB modules come populated with either 4Mb or 8Mb of flash memory depending on the module model that is ordered. This memory can be used for system software. See Table 1-1 for more information. In addition, the device uses a 128KB shared RAM, accessible by the processor and MAC, which allows the APS3 core to perform various data management tasks on the TX and RX data packets.

5.3 Non-volatile Memory (eFuse)

The ATWINC15x0-MR210xB modules have 768 bits of non-volatile eFuse memory that can be read by the CPU after device reset. This non-volatile one-time-programmable (OTP) memory can be used to store customer-specific parameters, such as MAC address; various calibration information, such as TX power, crystal frequency offset, etc.; and other software-specific configuration parameters. The eFuse is partitioned into six 128-bit banks. Each bank has the same bitmap (see following figure). The purpose of the first 80 bits in each bank is fixed, and the remaining 48 bits are general-purpose software dependent bits, or reserved for future use. Since each bank can be programmed independently, this allows for several updates of the device parameters following the initial programming; for example, updating the MAC address.

Figure 5-1. eFuse Bitmap



6. WLAN Subsystem

The WLAN subsystem is composed of the Media Access Controller (MAC) and the Physical Layer (PHY). The following two subsections describe the MAC and PHY in detail.

6.1 MAC

6.1.1 Description

The ATWINC15x0-MR210xB MAC is designed to operate at low power while providing high data throughput. The IEEE 802.11 MAC functions are implemented with a combination of dedicated datapath engines, hardwired control logic, and a low-power, high-efficiency microprocessor. The combination of dedicated logic with a programmable processor provides optimal power efficiency and real-time response while providing the flexibility to accommodate evolving standards and future feature enhancements.

Dedicated datapath engines are used to implement datapath functions with heavy computational requirements. For example, an FCS engine checks the CRC of the transmitting and receiving packets, and a cipher engine performs all the required encryption and decryption operations for the WEP, WPA-TKIP, and WPA2 CCMP-AES.

Control functions which have real-time requirements are implemented using hardwired control logic modules. These logic modules offer real-time response while maintaining configurability via the processor. Examples of hardwired control logic modules are the channel access control module (implements EDCA/HCCA, Beacon TX control, interframe spacing, etc.), protocol timer module (responsible for the Network Access Vector, back-off timing, timing synchronization function, and slot management), MPDU handling module, aggregation/de-aggregation module, block ACK controller (implements the protocol requirements for burst block communication), and TX/RX control FSMs (coordinate data movement between PHY-MAC interface, cipher engine, and the DMA interface to the TX/RX FIFOs).

The MAC functions implemented solely in software on the microprocessor have the following characteristics:

- Functions with high memory requirements or complex data structures. Examples are association table management and power save queuing.
- Functions with low computational load or without critical real-time requirements. Examples are authentication and association.
- Functions which need flexibility and upgradeability. Examples are beacon frame processing and QoS scheduling.

6.1.2 Features

The ATWINC15x0-MR210xB IEEE802.11 MAC supports the following functions:

- IEEE 802.11b/g/n
- IEEE 802.11e WMM QoS EDCA/PCF multiple access categories traffic scheduling
- Advanced IEEE 802.11n features:
  - Transmission and reception of aggregated MPDUs (A-MPDU)
  - Transmission and reception of aggregated MSDUs (A-MSDU)
  - Immediate Block Acknowledgment
  - Reduced Interframe Spacing (RIFS)
- Support for IEEE802.11i and WFA security with key management:

  - WEP 64/128
  - WPA-TKIP
  - 128-bit WPA2 CCMP (AES)
- Advanced power management:
  - Standard 802.11 Power Save Mode
  - Wi-Fi Alliance WMM-PS (U-APSD)
- RTS-CTS and CTS-self support
- Supports either STA or AP mode in the infrastructure basic service set mode
- Supports Independent Basic Service Set (IBSS)

6.2 PHY

6.2.1 Description

The ATWINC1500B WLAN PHY is designed to achieve reliable and power-efficient physical layer communication specified by IEEE 802.11 b/g/n in single stream mode with 20MHz bandwidth. Advanced algorithms have been employed to achieve maximum throughput in a real world communication environment with impairments and interference. The PHY implements all the required functions that include FFT, filtering, FEC (Viterbi decoder), frequency, timing acquisition and tracking, channel estimation and equalization, carrier sensing, clear channel assessment, and automatic gain control.

6.2.2 Features

The ATWINC1500B IEEE802.11 PHY supports the following functions:

- Single antenna 1x1 stream in 20MHz channels
- Supports IEEE 802.11b DSSS-CCK modulation: 1, 2, 5.5, 11Mbps
- Supports IEEE 802.11g OFDM modulation: 6, 9, 12,18, 24, 36, 48, 54Mbps
- Supports IEEE 802.11n HT modulations MCS0-7, 20MHz, 800 and 400ns guard interval: 6.5, 7.2, 13.0, 14.4, 19.5, 21.7, 26.0, 28.9, 39.0, 43.3, 52.0, 57.8, 58.5, 65.0, 72.2Mbps
- IEEE 802.11n mixed mode operation
- Per packet TX power control
- Advanced channel estimation/equalization, automatic gain control, CCA, carrier/symbol recovery, and frame detection

6.3 Radio

This section presents information describing the properties and characteristics of the ATWINC15x0-MR210xB and Wi-Fi radio transmit and receive performance capabilities of the device.

The performance measurements are taken at the RF pin assuming 50Ω impedance; the RF performance is guaranteed for room temperature of 25ºC with a derating of 2-3dB at boundary conditions.

Measurements were taken under typical conditions: VBATT=3.3V; VDDIO=3.3V; temperature: +25ºC

Table 6-1. Features and Properties

Feature	Description
Part Number	ATWINC15x0-MR210xB
WLAN Standard	IEEE 802.11 b/g/n, Wi-Fi compliant

Feature	Description
Host Interface	SPI
Dimension	21.7x14.7x2.1mm
Frequency Range	2.412GHz ~ 2.472GHz (2.4GHz ISM Band)
Number of Channels	11 for North America, and 13 for Europe
Modulation	802.11b: DQPSK, DBPSK, CCK 802.11g/n: OFDM /64-QAM,16-QAM, QPSK, BPSK
Data Rate	802.11b: 1, 2, 5.5, 11Mbps
	802.11g: 6, 9, 12, 18, 24, 36, 48, 54Mbps
Data Rate (20MHz, normal GI, 800ns)	802.11n: 6.5, 13, 19.5, 26, 39, 52, 58.5, 65Mbps
Data Rate (20MHz, short GI, 400ns)	802.11n: 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65,72.2Mbps
Operating temperature	-40 to +85ºC
Storage temperature	-40 to +125 ºC
Humidity	Operating Humidity 10% to 95% Non-Condensing Storage Humidity 5% to 95% Non-Condensing

6.3.1 Receiver Performance

Table 6-2. Receiver Performance

Parameter	Description	Minimum	Typical	Maximum	Unit
Frequency		2,412		2,472	MHz
Sensitivity 802.11b	1Mbps DSS		-95		dBm
	2Mbps DSS		-90		
	5.5Mbps DSS		-92		
	11Mbps DSS		-86		
Sensitivity 802.11g	6Mbps OFDM		-90		
	9Mbps OFDM		-89		
	12Mbps OFDM		-88		
	18Mbps OFDM		-85		
	24Mbps OFDM		-83		
	36Mbps OFDM		-80		
	48Mbps OFDM		-76		
	54Mbps OFDM		-74		
Sensitivity 802.11n (BW=20MHz)	MCS 0		-89		
	MCS 1		-87		
	MCS 2		-85		
	MCS 3		-82		
	MCS 4		-77		
	MCS 5		-74		
	MCS 6		-72		
	MCS 7		-70.5		
Maximum Receive Signal Level	1-11Mbps DSS		0		
	6-54Mbps OFDM		0		
	MCS 0 – 7		0		
Adjacent Channel Rejection	1Mbps DSS (30MHz offset)		50		dB
	11Mbps DSS (25MHz offset)		43		
	6Mbps OFDM (25MHz offset)		40		
	54Mbps OFDM (25MHz offset)		25		
	MCS 0 – 20MHz BW (25MHz offset)		40		
	MCS 7 – 20MHz BW (25MHz offset)		20		

Parameter	Description	Minimum	Typical	Maximum	Unit
Cellular Blocker Immunity	776-794MHz CDMA		-14		dBm
	824-849MHz GSM		-10		
	880-915MHz GSM		-10		
	1710-1785MHz GSM		-15		
	1850-1910MHz GSM		-15		
	1850-1910MHz WCDMA		-24		
	1920-1980MHz WCDMA		-24		

6.3.2 Transmitter Performance

Table 6-3. Transmitter Performance

Parameter	Description	Minimum	Typical	Maximum	Unit
Frequency	—	2,412	—	2,472	MHz
Output Power[1-2] ON_Transmit	802.11b 1Mbps	—	17.5	—	dBm
	802.11b 11Mbps	—	18.5	—	
	802.11g 6Mbps	—	17.5	—	
	802.11g 54Mbps	—	16	—	
	802.11n MCS 0	—	17.0	—	
	802.11n MCS 7	—	14.5	—	
TX Power Accuracy	—	—	±1.5 [2]	—	dB
Carrier Suppression	—	—	30.0	—	dBc
Harmonic Output Power	2nd	—		-41	dBm/MHz
	3rd	—	—	-41	

Note:

1. Measured at 802.11 spec compliant EVM/Spectral Mask.
2. Measured after RF matching network.
3. Operating temperature range is -40°C to +85°C. RF performance guaranteed at room temperature of 25°C with a 2-3dB change at boundary conditions.
4. With respect to TX power, different (higher/lower) RF output power settings may be used for specific antennas and/or enclosures, in which case recertification may be required.
5. The availability of some specific channels and/or operational frequency bands are country dependent and should be programmed at the Host product factory to match the intended destination. Regulatory bodies prohibit exposing the settings to the end user. This requirement needs to be taken care of via Host implementation.

7. External Interfaces

7.1 Interfacing with the Host Microcontroller

This section describes the ATWINC15x0-MR210xB to host microcontroller interface. The interface comprises of a slave SPI and additional control signals, as shown in the figure. For more information on SPI interface specification and timing, refer to Section 7.2: SPI Interface. Additional control signals are connected to the GPIO/IRQ interface of the microcontroller.

Figure 7-1. Interfacing with Host Microcontroller

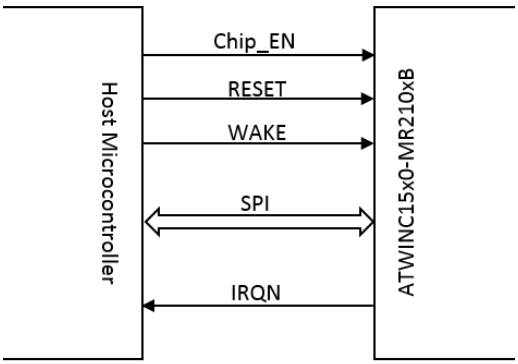


Table 7-1. Host Microcontroller Interface Pins

Module Pin	Function
4	RESET_N
11	WAKE
13	IRQ_N
22	CHIP_EN
16	SPI_SSN
15	SPI_MOSI
17	SPI_MISO
18	SPI_SCK

7.2 SPI Interface

7.2.1 Overview

The ATWINC15x0-MR210xB has a Serial Peripheral Interface (SPI) that operates as an SPI slave. The SPI interface can be used for control and for serial I/O of 802.11 data. The SPI pins are mapped as shown in the following Table. The SPI is a full-duplex slave-synchronous serial interface that is available immediately following reset when pin 10 (SPI_CFG) is tied to VDDIO.

Table 7-2. SPI Interface Pin Mapping

Pin #	SPI function
10	CFG: Must be tied to VDDIO
16	SSN: Active Low Slave Select
15	MOSI(RXD): Serial Data Receive
18	SCK: Serial Clock
17	MISO(TXD): Serial Data Transmit

When the SPI is not selected, i.e., when SSN is high, the SPI interface will not interfere with data transfers between the serial-master and other serial-slave devices. When the serial slave is not selected, its transmitted data output is buffered, resulting in a high impedance drive onto the MISO line.

The SPI interface responds to a protocol that allows an external host to read or write any register in the chip as well as initiate DMA transfers.

The SPI SSN, MOSI, MISO, and SCK pins of the ATWINC15x0-MR210xB have internal programmable pull-up resistors (see Section 9.1: Programmable Pull-up Resistors). These resistors should be programmed to be disabled. Otherwise, if any of the SPI pins are driven to a low level while the ATWINC15x0-MR210xB is in the low-power sleep state, the current will flow from the VDDIO supply through the pull-up resistors, increasing the current consumption of the module.

7.2.2 SPI Timing

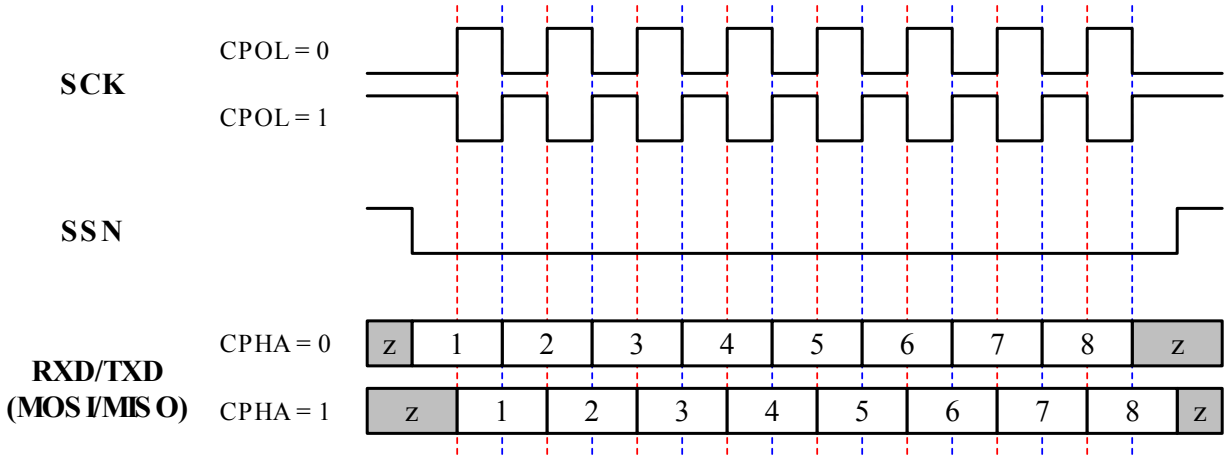
The SPI Slave interface supports four standard modes as determined by the Clock Polarity (CPOL) and Clock Phase (CPHA) settings. These modes are illustrated in the following table and figure.

Table 7-3. SPI Slave Modes

Mode	CPOL	CPHA
0	0	0
1	0	1
2	1	0
3	1	1

The red lines in the following figure correspond to Clock Phase = 0 and the blue lines correspond to Clock Phase = 1.

Figure 7-2. SPI Slave Clock Polarity and Clock Phase Timing



The SPI timing is provided in the following figure and table.

Figure 7-3. SPI Timing Diagram (SPI Mode CPOL=0, CPHA=0)

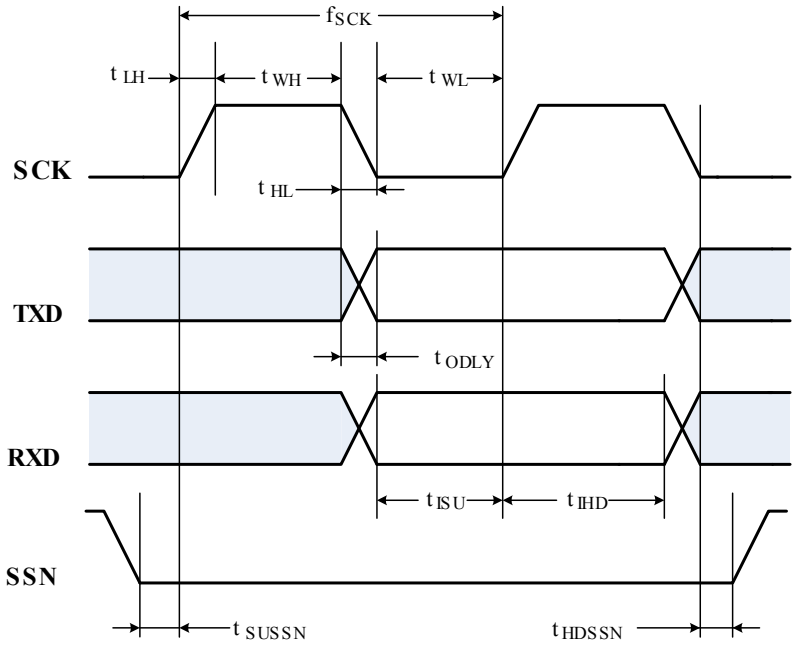


Table 7-4. SPI Slave Timing Parameters[1]

Parameter	Symbol	Min.	Max.	Units
Clock Input Frequency[2]	f_{SCK}	—	48	MHz
Clock Low Pulse Width	t_{WL}	4	—	ns
Clock High Pulse Width	t_{WH}	5	—	
Clock Rise Time	t_{LH}	0	7	
Clock Fall Time	t_{HL}	0	7	
TXD Output Delay[3]	t_{ODLY}	4	9 from SCK fall 12.5 from SCK rise	
RXD Input Setup Time	t_{ISU}	1	—	
RXD Input Hold Time	t_{IHD}	5	—	
SSN Input Setup Time	t_{SUSSN}	3	—	
SSN Input Hold Time	t_{HDSSN}	5.5	—	

Note:

1. Timing is applicable to all SPI modes
2. Maximum clock frequency specified is limited by the SPI Slave interface internal design, actual maximum clock frequency can be lower and depends on the specific PCB layout
3. Timing based on 15pF output loading

7.3 UART Interface

The ATWINC15x0-MR210xB supports the Universal Asynchronous Receiver/Transmitter (UART) interface. This interface should be used for debug purposes only. The UART is available on pins 14 and 19. The UART is compatible with the RS-232 standard, and the ATWINC15x0-MR210xB operates as Data Terminal Equipment (DTE). It has a two-pin RXD/TXD interface.

The default configuration for accessing the UART interface of ATWINC15x0-MR210xB is mentioned below:

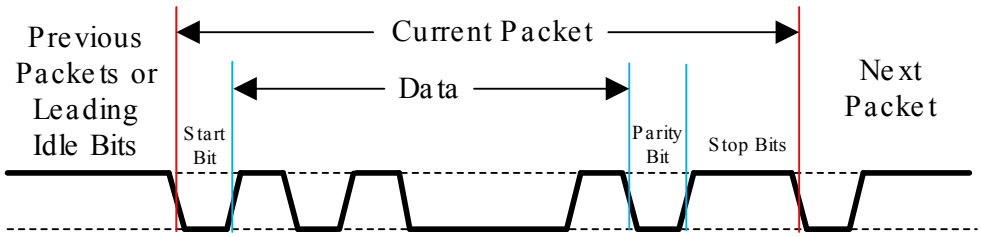
- Baud rate: 115200
- Data: 8 bit
- Parity: None
- Stop bit: 1 bit
- Flow control: None

It also has RX and TX FIFOs, which ensure reliable high-speed reception and low software overhead transmission. FIFO size is 4 x 8 for both RX and TX direction. The UART also has status registers showing the number of received characters available in the FIFO and various error conditions, as well the ability to generate interrupts based on these status bits.

An example of the UART receiving or transmitting a single packet is shown in the following figure. This example shows 7-bit data (0x45), odd parity, and two stop bits.

Important: UART2 supports RTS and CTS flow control. The UART RTS and UART CTS MUST be connected to the host MCU UART and enabled for the UART interface to be functional.

Figure 7-4. Example of UART RX of TX Packet



8. Power Consumption

8.1 Description of Device States

The ATWINC15x0-MR210xB has several device states:

- ON_Transmit – Device is actively transmitting an 802.11 signal. Highest output power and nominal current consumption.
- ON_Receive – Device is actively receiving an 802.11 signal. Lowest sensitivity and nominal current consumption.
- ON_Doze – Device is ON but is neither transmitting nor receiving
- Power_Down – Device core supply off (Leakage)
- IDLE connect – Device is connected with 1 DTIM beacon interval

The following pins are used to switch between the ON and Power_Down states:

- CHIP_EN – Device pin (pin #22) used to enable DC/DC Converter
- VDDIO – I/O supply voltage from external supply
  In the ON states, VDDIO is on and CHIP_EN is high (at VDDIO voltage level). To switch between the ON states and Power_Down state CHIP_EN has to change between high and low (GND) voltage. When VDDIO is off and CHIP_EN is low, the chip is powered off with no leakage (also see Section 8.3: Restrictions for Power States).

8.2 Current Consumption in Various Device States

Table 8-1. Current Consumption

Device State	Code Rate	Output power, dBm	Current Consumption [1]	
			IVBATT	IVDDIO
ON_Transmit	802.11b 1Mbps	17.5	268mA	22mA
	802.11b 11Mbps	18.5	264mA	22mA
	802.11g 6Mbps	17.5	269mA	22mA
	802.11g 54Mbps	16.0	266mA	22mA
	802.11n MCS 0	17.0	268mA	22mA
	802.11n MCS 7	14.5	265mA	22mA
ON_Receive	802.11b 1Mbps	N/A	61mA	22mA
	802.11b 11Mbps	N/A	61mA	22mA
	802.11g 6Mbps	N/A	61mA	22mA
	802.11g 54Mbps	N/A	61mA	22mA
	802.11n MCS 0	N/A	61mA	22mA
	802.11n MCS 7	N/A	61mA	22mA

Device State	Code Rate	Output power, dBm	Current Consumption [1]	
			IVBATT	IVDDIO
ON_Doze	N/A	N/A	380µA	<10µA
Power_Down	N/A	N/A	<0.5µA	<3.5µA

Note:

1. Measured conditions: VBATT @ 3.6V, VDDIO@ 3.3V, temp. 25°C.

8.3 Restrictions for Power States

When no power is supplied to the device, for example, the DC/DC Converter output and VDDIO are both off (at ground potential), a voltage cannot be applied to the device pins because each pin contains an ESD diode from the pin to supply. This diode will turn on when a voltage higher than one diode drop is supplied to the pin.

If a voltage must be applied to the signal pads while the chip is in a low-power state, the VDDIO supply must be on, so the SLEEP or Power_Down state must be used.

Similarly, to prevent the pin-to-ground diode from turning on, do not apply a voltage that is more than one diode drop below ground to any pin.

8.4 Power-up/down Sequence

The power-up/down sequence for ATWINC15x0-MR210xB is shown in the Following Figure. The timing parameters are provided in following the table.

Figure 8-1. Power Up/Down Sequence

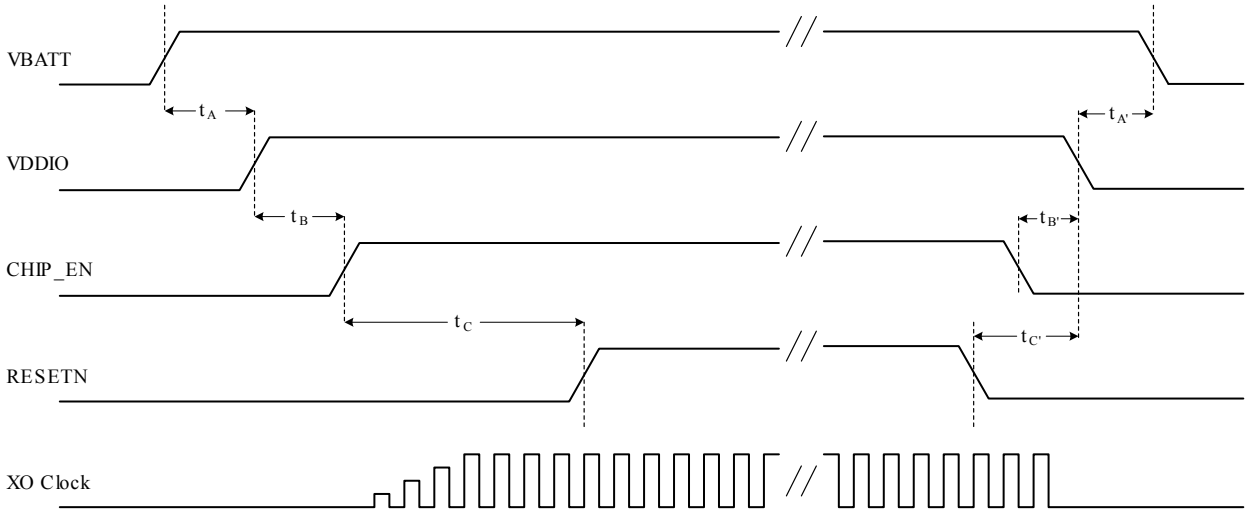


Table 8-2. Power-up/down Sequence Timing

Parameter	Min.	Max.	Units	Description	Notes
t_A	0		ms	VBATT rise to VDDIO rise	VBATT and VDDIO can rise simultaneously or can be tied together. VDDIO must not rise before VBATT.
t_B	0		ms	VDDIO rise to CHIP_EN rise	CHIP_EN must not rise before VDDIO. CHIP_EN must be driven high or low, not left floating.
t_C	5		ms	CHIP_EN rise to RESETN rise	This delay is needed because the XO clock must stabilize before RESETN removal. RESETN must be driven high or low, not left floating.
$t_{A'}$	0		ms	VDDIO fall to VBATT fall	VBATT and VDDIO can fall simultaneously or can be tied together. VBATT must not fall before VDDIO.
$t_{B'}$	0		ms	CHIP_EN fall to VDDIO fall	VDDIO must not fall before CHIP_EN. CHIP_EN and RESETN can fall simultaneously.
$t_{C'}$	0		ms	RESETN fall to VDDIO fall	VDDIO must not fall before RESETN. RESETN and CHIP_EN can fall simultaneously.

8.5 Digital I/O Pin Behavior During Power-up Sequences

Following Table represents digital I/O Pin states corresponding to device power modes.

Table 8-3. Digital I/O Pin Behavior in Different Device States

Device state	VDDIO	CHIP_EN	RESETN	Output driver	Input driver	Pull-up/down resistor (96kΩ)
Power Down: core supply off	High	Low	Low	Disabled (Hi-Z)	Disabled	Disabled
Power-On Reset: core supply on, hard reset on	High	High	Low	Disabled (Hi-Z)	Disabled	Enabled

Device state	VDDIO	CHIP_EN	RESETN	Output driver	Input driver	Pull-up/down resistor (96kΩ)
Power-On Default: core supply on, the device is out of reset but not programmed yet	High	High	High	Disabled (Hi-Z)	Enabled	Enabled
On Sleep/ On Transmit/ On Receive: core supply on, device programmed by firmware	High	High	High	Programmed by firmware for each pin: Enabled or Disabled	Opposite of Output Driver state	Programmed by firmware for each pin: Enabled or Disabled

8.6 Module Reset

If a module reset is performed, the RESETN pin must be pulsed low for a minimum of 1µ second.

9. Notes On Interfacing to the ATWINC15x0-MR210xB

9.1 Programmable Pull-up Resistors

The ATWINC15x0-MR210xB provides programmable pull-up resistors on various pins. The purpose of these resistors is to keep any unused input pins from floating, which can cause excess current to flow through the input buffer from the VDDIO supply. Any unused module pin on the ATWINC15x0-MR210xB should leave these pull-up resistors enabled so the pin will not float. The default state at power up is for the pull-up resistor to be enabled. However, any pin that is used should have the pull-up resistor disabled. The reason for this is that if any pins are driven to a low level while the ATWINC15x0-MR210xB is in the low power sleep state, current will flow from the VDDIO supply through the pull-up resistors, increasing the current consumption of the module. Since the value of the pull-up resistor is approximately 100KΩ, the current through any pull-up resistor that is being driven low will be VDDIO/100K. For VDDIO = 3.3V, the current through each pull-up resistor that is driven low would be approximately 3.3V/100K = 33µA. Pins which are used and have had the programmable pull-up resistor disabled should always be actively driven to either a high or low level and not be allowed to float.