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ATWINC3400-MR210CA

IEEE® 802.11 b/g/n Network Controller with Integrated Bluetooth® Low Energy Module

Introduction

The ATWINC3400-MR210CA is an IEEE 802.11 b/g/n RF/Baseband/Medium Access Control (MAC) network controller with Bluetooth Low Energy module. The ATWINC3400-MR210CA modules are Bluetooth 5.0 certified. This module is optimized for low power and high performance mobile applications. This module features small form factor with integrated Power Amplifier (PA), Low-Noise Amplifier (LNA), Transmit/Receive (T/R) switch (for Wi-Fi® and Bluetooth), Power Management Unit (PMU), and Chip Antenna. The ATWINC3400-MR210CA module requires a 32.768 kHz clock for Sleep operation.

The ATWINC3400-MR210CA module utilizes highly optimized IEEE 802.11 Bluetooth coexistence protocols, and provides Serial Peripheral Interface (SPI) to interface with the host controller.

Features

Wi-Fi features:

- IEEE 802.11 b/g/n RF/PHY/MAC
- IEEE 802.11 b/g/n (1x1) with Single Spatial Stream, up to 72 Mbps PHY Rate in 2.4 GHz ISM Band
- Integrated Chip Antenna
- Superior Sensitivity and Range via Advanced PHY Signal Processing
- Advanced Equalization and Channel Estimation
- Advanced Carrier and Timing Synchronization
- Supports Soft-AP
- Supports IEEE 802.11 WEP, WPA, and WPA2
- Superior MAC Throughput through Hardware Accelerated Two-Level A-MSDU/A-MPDU Frame Aggregation and Block Acknowledgment
- On-Chip Memory Management Engine to Reduce the Host Load
- Operating Temperature Range from -40°C to +85°C
- Wi-Fi Alliance® Certified for Connectivity and Optimizations
  - ID: WFA62065
- Integrated On-Chip Microcontroller
- SPI Host Interface
- Integrated Flash Memory for Wi-Fi and Bluetooth System Software
- Low Leakage On-Chip Memory for State Variables
- Fast AP Re-Association (150 ms)
- On-Chip Network Stack to Offload MCU
  - Integrated network IP slack to minimize the host CPU requirements

- Network Features: Firmware Version 1:2:x
  - TCP, UDP, DHCP, ARP, HTTP, SSL, DNS, and SNTP

Bluetooth features:

- ATWINC3400-MR210CA Bluetooth Low Energy Certification (end product) QD ID 112092
- Adaptive Frequency Hopping (AFH)
- Superior Sensitivity and Range

Table of Contents

1. Ordering Information and Module Marking

The following table provides the ordering details for the ATWINC3400-MR210CA module.

Table 1-1. Ordering Details

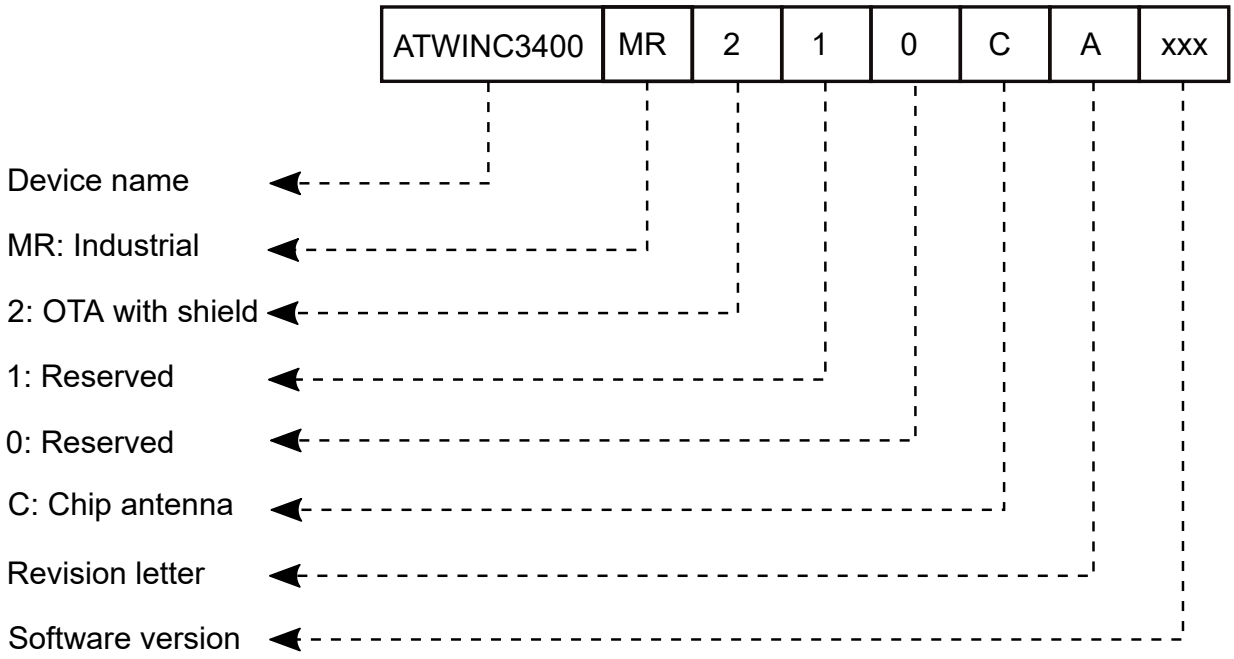
Model Number	Ordering Code	Package	Description	Regulatory Information
ATWINC3400-MR210CA	ATWINC3400-MR210CAxxx [1]	22.43 x 14.73 x 2.0 mm	Certified module with chip antenna	FCC, IC, CE

Note:

1. 'xxx' in the preceding table and following figure denotes the software version. For example, at the time of publish the software is v1.22, so its equivalent order code is ATWINC3400-MR210CA122. The order code changes as per the software version. For more information on ordering code, refer to the ATWINC3400 product page.

The following figure illustrates the ATWINC3400-MR210CA module marking information.

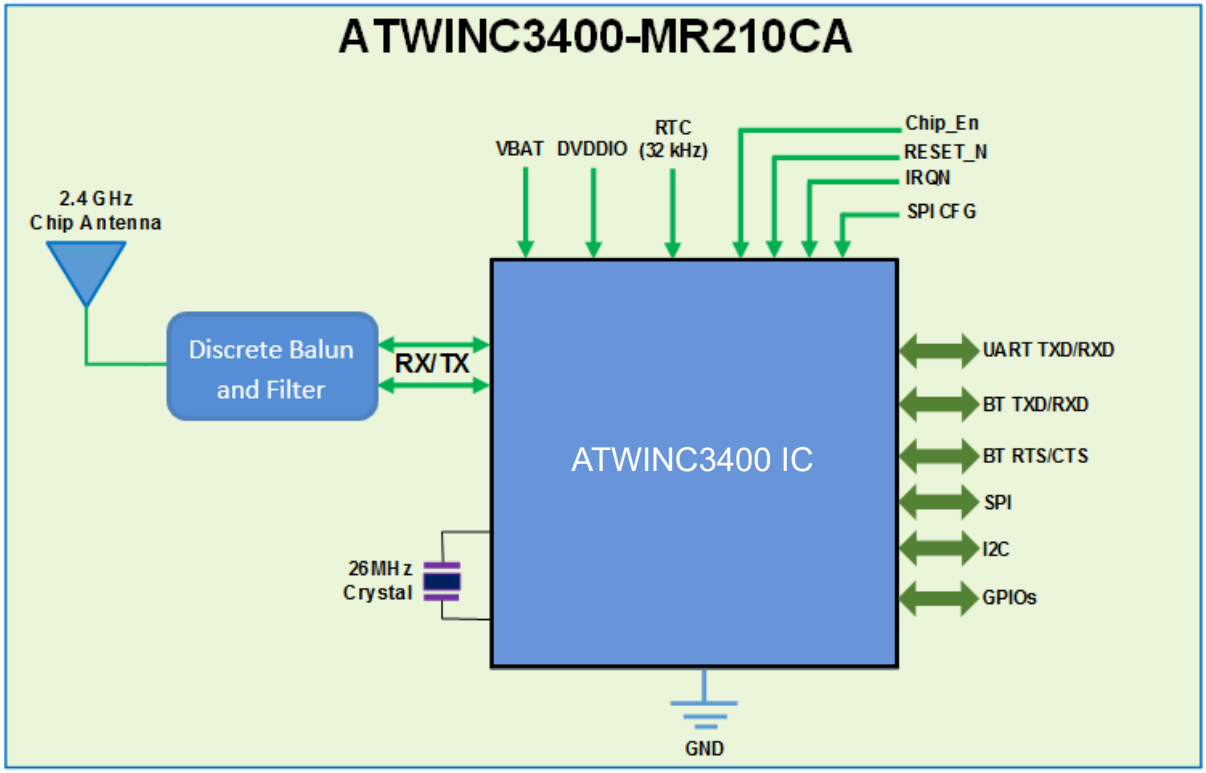
Figure 1-1. Marking Information



2. Block Diagram

The following figure shows the block diagram of the ATWINC3400-MR210CA module.

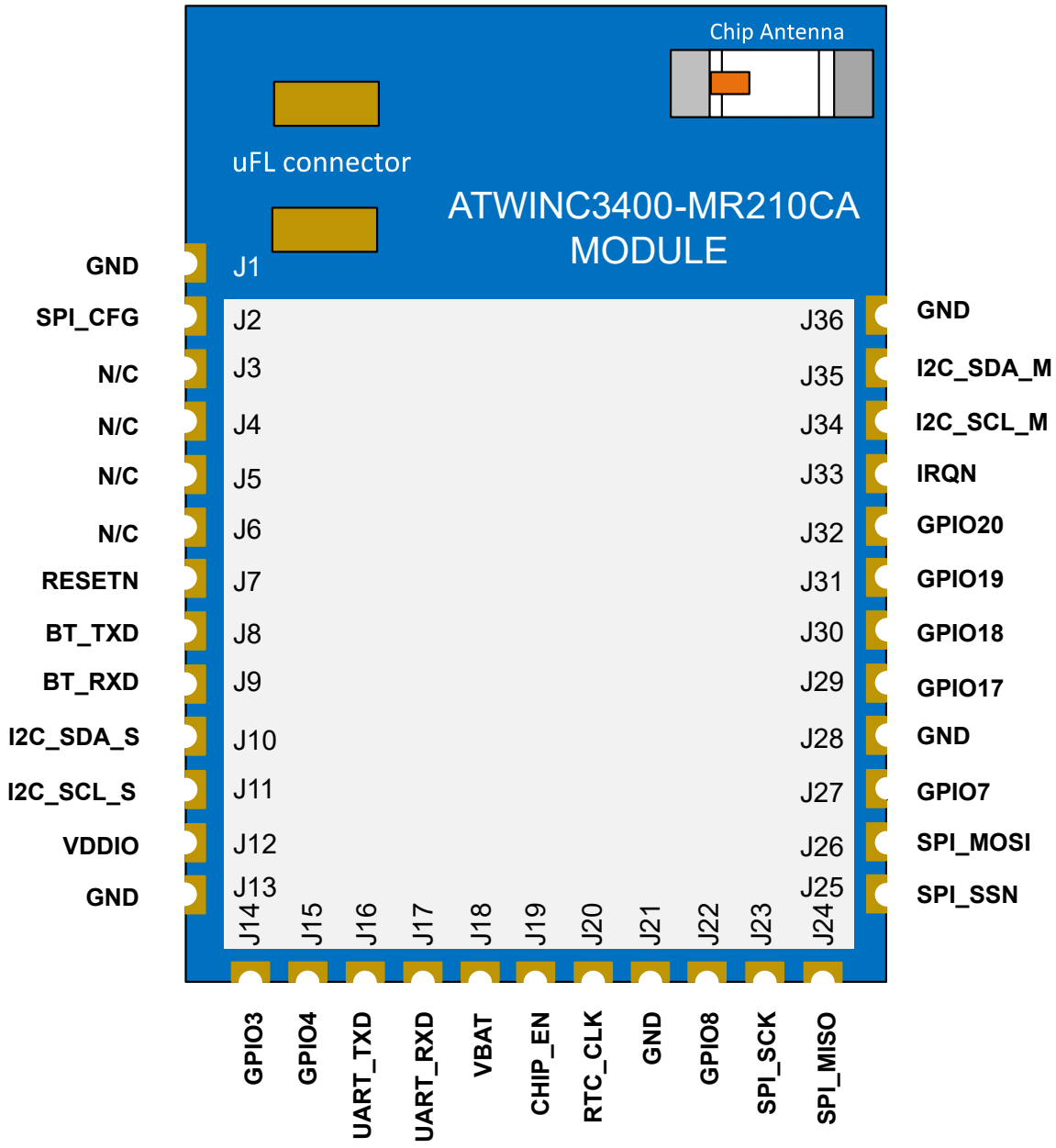
Figure 2-1. ATWINC3400-MR210CA Module Block Diagram



3. Pinout and Package Information

This package contains an exposed paddle that must be connected to the system board ground. The ATWINC3400-MR210CA module pin assignment is shown in following figure.

Figure 3-1. ATWINC3400-MR210CA Module Pin Assignment



The following table provides the ATWINC3400-MR210CA module pin description.

Table 3-1. ATWINC3400-MR210CA Module Pin Description

Pin #	Pin Name	Pin Type	Description
1	GND	GND	Ground pin.

Pin #	Pin Name	Pin Type	Description
2	SPI_CFG	Digital Input	Serial Peripheral Interface pin, which must be tied to VDDIO.
3	NC	-	No connection.
4	NC	-	No connection.
5	NC	-	No connection.
6	NC	-	No connection.
7	RESETN	Digital Input	• Active-low hard Reset pin. • When the Reset pin is asserted low, the module is in the Reset state. When the Reset pin is asserted high, the module functions normally. • This pin must connect to a host output that is low by default on power-up. If the host output is tri-stated, add a 1 MOhm pull down resistor to ensure a low level at power-up.
8	BT_TXD	Digital I/O, Programmable pull up	Bluetooth UART transmit data output pin.
9	BT_RXD	Digital I/O, Programmable pull up	Bluetooth UART receive data input pin.
10	I2C_SDA_S	Digital I/O, Programmable pull up	• I2C Slave data pin. • Used only for test purposes. It is recommended to add a test point for this pin.
11	I2C_SCL_S	Digital I/O, Programmable pull up	• I2C Slave clock pin. • Used only for test purposes. It is recommended to add a test point for this pin.
12	VDDIO	Power	Digital I/O power supply.
13	GND	GND	Ground pin.
14	GPIO3	Digital I/O, Programmable pull up	General Purpose Input/Output pin.
15	GPIO4	Digital I/O, Programmable pull up	General Purpose Input/Output pin.
16	UART_TXD	Digital I/O, Programmable pull up	• Wi-Fi UART TxD output pin. • Used only for debug development purposes. It is recommended to add a test point for this pin.

Pin #	Pin Name	Pin Type	Description
17	UART_RXD	Digital I/O, Programmable pull up	• Wi-Fi UART RxD input pin. • Used only for debug development purposes. It is recommended to add a test point for this pin.
18	VBAT	Power	Power supply pin for DC/DC converter and PA.
19	CHIP_EN	Digital Input	• PMU enable pin. • When the CHIP_EN pin is asserted high, the module is enbled. When the CHIP_EN pin is asserted low, the module is disabled or put into Power-Down mode. • Connect to a host output that is low by default at power-up. If the host output is tri-stated, add a 1 MOhm pull down resistor if necessary to ensure a low level at power-up.
20	RTC_CLK	Digital I/O, Programmable pull up	• RTC Clock input pin. • This pin must connect to a 32.768 kHz clock source.
21	GND	GND	Ground pin.
22	GPIO8	Digital I/O, Programmable pull up	General Purpose Input/Output pin.
23	SPI_SCK	Digital I/O, Programmable pull up	SPI clock pin.
24	SPI_MISO	Digital I/O, Programmable pull up	SPI MISO (Master In Slave Out) pin.
25	SPI_SSN	Digital I/O, Programmable pull up	Active-low SPI SSN (Slave Select) pin.
26	SPI_MOSI	Digital I/O, Programmable pull up	SPI MOSI (Master Out Slave In) pin.
27	GPIO7	Digital I/O, Programmable pull up	General Purpose Input/Output pin.
28	GND	GND	Ground pin.
29	GPIO17	Digital I/O, Programmable pull up	General Purpose Input/Output pin.
30	GPIO18	Digital I/O, Programmable pull up	General Purpose Input/Output pin.
31	GPIO19	Digital I/O, Programmable pull up	General Purpose Input/Output pin.

Pin #	Pin Name	Pin Type	Description
32	GPIO20	Digital I/O, Programmable pull up	General Purpose Input/Output pin.
33	IRQN	Digital output, Programmable pull up	• ATWINC3400-MR210CA module host interrupt request output pin. • This pin must connect to a host interrupt pin.
34	I2C_SCL_M	Digital I/O, Programmable pull up	I2C Master clock pin.
35	I2C_SDA_M	Digital I/O, Programmable pull up	I2C Master data pin.
36	GND	GND	Ground pin.
37	PADDLE VSS	Power	Connect to system board ground.

3.1 Package Description

The following table provides the ATWINC3400-MR210CA module package dimensions.

Table 3-2. ATWINC3400-MR210CA Module Package Information

Parameter	Value	Unit
Pad count	36	-
Package size	22.43 x 14.73	mm
Total thickness	2.09	
Pad pitch	1.20	
Pad width	0.81	
Exposed pad size	4.4 x 4.4	

4. Electrical Characteristics

This chapter provides an overview of the electrical characteristics of the ATWINC3400-MR210CA module.

4.1 Absolute Maximum Ratings

The following table provides the absolute maximum ratings for the ATWINC3400-MR210CA module.

Table 4-1. ATWINC3400-MR210CA Module Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
VDDIO	I/O supply voltage	-0.3	5.0	V
VBAT	Battery supply voltage	-0.3	5.0	
V_{IN}	Digital input voltage	-0.3	VDDIO	
V_{AIN}	Analog input voltage	-0.3	1.5	
V_{ESDHBM}	Electrostatic discharge Human Body Model (HBM)	-1000, -2000 (see notes below)	+1000, +2000 (see notes below)	
T_A	Storage temperature	-65	150	ºC
-	Junction temperature	-	125	
-	RF input power	-	23	dBm

1. V_{IN} corresponds to all the digital pins.
2. For V_{ESDHBM}, each pin is classified as Class 1, or Class 2, or both:
   - 2.1. The Class 1 pins include all the pins (both analog and digital).
   - 2.2. The Class 2 pins include all digital pins only.
   - 2.3. V_{ESDHBM} is ±1 kV for Class 1 pins. V_{ESDHBM} is ± 2 kV for Class 2 pins.

⚠ CAUTION Stresses beyond those listed under “Absolute Maximum Ratings” cause permanent damage to the device. This is a stress rating only. The functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods affects the device reliability.

4.2 Recommended Operating Conditions

The following table provides the recommended operating conditions for the ATWINC3400-MR210CA module.

Table 4-2. ATWINC3400-MR210CA Module Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
VDDIO	I/O supply voltage (1)	2.7	3.3	3.6	V
VBAT	Battery supply voltage(2)(3)	3.0	3.6	4.2	V
-	Operating temperature	-40	-	85	°C

Note:

1. I/O supply voltage is applied to the VDDIO pin.
2. Battery supply voltage is applied to the VBAT pin.
3. The ATWINC3400-MR210CA module is functional across this range of voltages; however, optimal RF performance is guaranteed for VBAT in the range ≥ 3.0V VBAT ≤ 4.2V.

4.3 DC Characteristics

The following table provides the DC characteristics for the ATWINC3400-MR210CA module digital pads.

Table 4-3. DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage	-0.30	-	0.60	V
V_{IH}	Input High Voltage	VDDIO-0.60	-	VDDIO+0.30	
V_{OL}	Output Low Voltage	-	-	0.45	
V_{OH}	Output High Voltage	VDDIO-0.50	-	-	
-	Output Load Capacitance	-	-	20	pF
-	Digital Input Load Capacitance	-	-	6	

4.4 IEEE 802.11 b/g/n Radio Performance

4.4.1 Receiver Performance

The receiver performance is tested under following conditions:

- VBAT = 3.3V
- VDDIO = 3.3V
- Temp = 25°C
- Measured after RF matching network

The following table provides the receiver performance characteristics for the ATWINC3400-MR210CA module.

Table 4-4. IEEE 802.11 Receiver Performance Characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency	-	2,412	-	2,472	MHz
Sensitivity 802.11b	1 Mbps DSSS	-	-95.0	-	dBm
	2 Mbps DSSS	-	-94.0	-	
	5.5 Mbps DSSS	-	-90.0	-	
	11 Mbps DSSS	-	-86.0	-	
Sensitivity 802.11g	6 Mbps OFDM	-	-90.0	-	dBm
	9 Mbps OFDM	-	-89.0	-	
	12 Mbps OFDM	-	-87.0	-	
	18 Mbps OFDM	-	-85.0	-	
	24 Mbps OFDM	-	-82.0	-	
	36 Mbps OFDM	-	-79.0	-	
	48 Mbps OFDM	-	-75.0	-	
	54 Mbps OFDM	-	-73.0	-	
Sensitivity 802.11n (BW=20 MHz, 800ns GI)	MCS 0	-	-89.0	-	dBm
	MCS 1	-	-87.0	-	
	MCS 2	-	-84.0	-	
	MCS 3	-	-82.0	-	
	MCS 4	-	-78.0	-	
	MCS 5	-	-75.0	-	
	MCS 6	-	-73.0	-	
	MCS 7	-	-71.0	-	
Maximum receive signal level	1-11 Mbps DSSS	-	0	-	dBm
	6-54 Mbps OFDM	-	0	-	
	MCS 0 - 7 (800ns GI)	-	0	-	
Adjacent channel rejection	1 Mbps DSSS (30 MHz offset)	-	50	-	dB
	11 Mbps DSSS (25 MHz offset)	-	43	-	
	6 Mbps OFDM (25 MHz offset)	-	40	-	
	54 Mbps OFDM (25 MHz offset)	-	25	-	
	MCS 0 – 20 MHz BW (25 MHz offset)	-	40	-	
	MCS 7 – 20 MHz BW (25 MHz offset)	-	20	-	

4.4.2 Transmitter Performance

The transmitter performance is tested under following conditions:

- VBAT = 3.3V
- VDDIO = 3.3V
- Temp = 25°C

The following table provides the transmitter performance characteristics for the ATWINC3400-MR210CA module.

Table 4-5. IEEE 802.11 Transmitter Performance Characteristics

Parameter	Description	Minimum	Typical	Max.	Unit
Frequency	-	2,412	-	2,472	MHz
Output power	802.11b 1 Mbps	-	16.7(1)	-	dBm
	802.11b 11 Mbps	-	17.5(1)	-	
	802.11g OFDM 6 Mbps	-	18.3(1)	-	
	802.11g OFDM 54 Mbps	-	13.0(1)	-	
	802.11n HT20 MCS 0 (800ns GI)	-	17.5(1)	-	
	802.11n HT20 MCS 7 (800ns GI)	-	12.5 (1)(2)	-	
Tx power accuracy	-	-	±1.5(3)	-	dB
Carrier suppression	-	-	30.0	-	dBc
Harmonic output power (Radiated, Regulatory mode)	2nd	-	-	-41	dBm/MHz
	3rd	-	-	-41	

Note:

1. Measured at IEEE 802.11 specification compliant EVM/Spectral mask.
2. Typical output power shall be 10 dBm only for channel-10 (2.457 GHz). Values mentioned in the preceding table are applicable for all the other channels.
3. Measured after RF matching network.
4. Operating temperature range is -40°C to +85°C. RF performance guaranteed at room temperature of 25°C with a 2-3dB change at boundary conditions.
5. With respect to Tx power, different (higher/lower) RF output power settings may be used for specific antennas and/or enclosures, in which case re-certification may be required.
6. The availability of some specific channels and/or operational frequency bands are country-dependent and should be programmed at the host product factory to match the intended destination. Regulatory bodies prohibit exposing the settings to the end user. This requirement needs to be taken care of via host implementation.

4.5 Bluetooth Radio Performance

4.5.1 Receiver Performance

The receiver performance is tested under following conditions:

- VBAT = 3.3V
- VDDIO = 3.3V
- Temp: 25°C
- Measured after RF matching network

The following table provides the Bluetooth receiver performance characteristics for the ATWINC3400-MR210CA module.

Table 4-6. Bluetooth Receiver Performance Characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency	-	2,402	-	2,480	MHz
Sensitivity (ideal Tx)	Bluetooth Low Energy (GFSK)	-	-92.5	-	dBm
Maximum receive signal level	Bluetooth Low Energy (GFSK)	-	-2	-	
Interference performance (Bluetooth Low Energy)	Co-channel	-	9		dB
	adjacent + 1 MHz	-	-4	-	
	adjacent - 1 MHz	-	-2	-	
	adjacent + 2 MHz(image frequency)	-	-24	-	
	adjacent - 2 MHz	-	-25	-	
	adjacent + 3 MHz (adjacent to image)	-	-27	-	
	adjacent - 3 MHz	-	-27	-	
	adjacent + 4 MHz	-	-28	-	
	adjacent - 4 MHz	-	-27	-	
	adjacent +5 MHz	-	-27	-	
	adjacent - 5 MHz	-	-27	-	

4.5.2 Transmitter Performance

The transmitter performance is tested under following conditions:

- VBAT = 3.3V
- VDDIO = 3.3V
- Temp: 25°C
- Measured after RF matching network.

The following table provides the Bluetooth transmitter performance characteristics for the ATWINC3400-MR210CA module.

Table 4-7. Bluetooth Transmitter Performance Characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency	-	2,402	-	2,480	MHz
Output power	Bluetooth Low Energy (GFSK)	-	3.3	3.8	dBm
In-band spurious emission (Bluetooth Low Energy)	N+2 (Image frequency)	-	-33	-	
	N + 3 (Adjacent to image frequency)	-	-32	-	
	N-2	-	-48	-	
	N-3	-	-47	-	

5. Power Management

5.1 Device States

The ATWINC3400-MR210CA module has multiple device states, based on the state of the IEEE 802.11 and Bluetooth subsystems. It is possible for both subsystems to be active at the same time. To simplify the device power consumption breakdown, the following basic states are defined. One subsystem can be active at a time:

- WiFi_ON_Transmit – Device actively transmits IEEE 802.11 signal
- WiFi_ON_Receive – Device actively receives IEEE 802.11 signal
- BT_ON_Transmit – Device actively transmits Bluetooth signal
- BT_ON_Receive – Device actively receives Bluetooth signal
- Doze – Device is powered on but it does not actively transmit or receive data
- Power_Down – Device core supply is powered off

5.2 Controlling Device States

The following table shows different device states and their power consumption for the ATWINC3400-MR210CA . The device states can be switched using the following:

- CHIP_EN – Module pin (pin 19) enables or disables the DC/DC converter
- VDDIO – I/O supply voltage from external supply

In the ON states, VDDIO is ON and CHIP_EN is high (at VDDIO voltage level). To change from the ON states to Power_Down state, connect the RESETN and CHIP_EN pin to logic low (GND) by following the power-down sequence mentioned in Figure 5-1. When VDDIO is OFF and CHIP_EN is low, the chip is powered off with no leakage.

Table 5-1. Device States Current Consumption

Device State	Code Rate	Output Power (dBm)	Current Consumption(1)	
			I_{VBAT}	I_{VDDIO}
ON_WiFi_Transmit	802.11b 1 Mbps	16.7	271 mA	24 mA
	802.11b 11 Mbps	17.5	265 mA	24 mA
	802.11g 6 Mbps	18.3	275 mA	24 mA
	802.11g 54 Mbps	13.0	235 mA	24 mA
	802.11n MCS 0	17.5	272 mA	24 mA
	802.11n MCS 7	12.5	232 mA	24 mA

Device State	Code Rate	Output Power (dBm)	Current Consumption(1)	
			I_{VBAT}	I_{VDDIO}
ON_WiFi_Receive	802.11b 1 Mbps	N/A	63.9 mA	23.7 mA
	802.11b 11 Mbps	N/A	63.9 mA	23.7 mA
	802.11g 6 Mbps	N/A	63.9 mA	23.7 mA
	802.11g 54 Mbps	N/A	63.9 mA	23.7 mA
	802.11n MCS 0	N/A	63.9 mA	23.7 mA
	802.11n MCS 7	N/A	63.9 mA	23.7 mA
ON_BT_Transmit	BLE 1 Mbps	3.3	79.37 mA	23.68 mA
ON_BT_Receive	BLE 1 Mbps	N/A	51.36 mA	23.68 mA
Doze (Bluetooth Low Energy Idle)	N/A	N/A	53 mA (2)	
Doze (Bluetooth Low Energy Low Power)	N/A	N/A	1 mA (2)	
Power_Down	N/A	N/A	10.5 uA(2)	

Note:

1. Conditions: VBAT = 3.3V, VDDIO = 3.3V, at 25°C.
2. Current consumption mentioned for these states is the sum of current consumed in VDDIO and VBAT voltage rails.

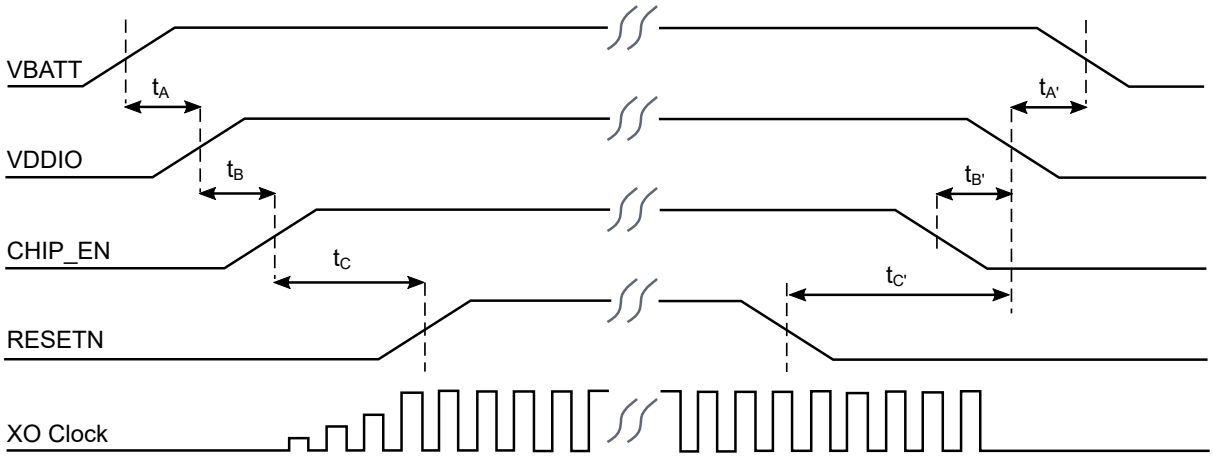
When power is not supplied to the device (DC/DC converter output and VDDIO are OFF, at ground potential), voltage cannot be applied to the ATWINC3400-MR210CA module pins because each pin contains an ESD diode from the pin to supply. This diode turns on when voltage higher than one diode-drop is supplied to the pin.

If voltage must be applied to the signal pads when the chip is in a low-power state, the VDDIO supply must be ON, so the Power_Down state must be used. Similarly, to prevent the pin-to-ground diode from turning ON, do not apply voltage that is more than one diode-drop below the ground to any pin.

5.3 Power-Up/Down Sequence

The following figure illustrates the power-up/down sequence for the ATWINC3400-MR210CA module.

Figure 5-1. Power-Up/Down Sequence



The following table provides power-up/down sequence timing parameters.

Table 5-2. Power-Up/Down Sequence Timing

Parameter	Min.	Max.	Units	Description	Notes
t_A	0	-	ms	VBAT rise to VDDIO rise	VBAT and VDDIO can rise simultaneously or connected together. VDDIO must not rise before VBAT.
t_B	0	-	ms	VDDIO rise to CHIP_EN rise	CHIP_EN must not rise before VDDIO. CHIP_EN must be driven high or low and must not be left floating.
t_C	5	-	ms	CHIP_EN rise to RESETN rise	This delay is required to stabilize the XO clock before RESETN removal. RESETN must be driven high or low and must not be left floating.
$t_{A'}$	0	-	ms	VDDIO fall to VBAT fall	VBAT and VDDIO fall simultaneously or connected together. VBAT must not fall before VDDIO.
$t_{B'}$	0	-	ms	CHIP_EN fall to VDDIO fall	VDDIO must not fall before CHIP_EN. CHIP_EN and RESETN must fall simultaneously.
$t_{C'}$	0	-	ms	RESETN fall to VDDIO fall	VDDIO must not fall before RESETN. RESETN and CHIP_EN fall simultaneously.

5.4 Digital I/O Pin Behavior During Power-Up Sequences

The following table represents the digital I/O pin states corresponding to the device power modes.

Table 5-3. Digital I/O Pin Behavior in Different Device States

Device State	VDDIO	CHIP_EN	RESETN	Output Driver	Input Driver	Pull Up/Down Resistor (96 kOhm)
Power_Down: core supply OFF	High	Low	Low	Disabled (Hi-Z)	Disabled	Disabled
Power-On Reset: core supply and hard reset ON	High	High	Low	Disabled (Hi-Z)	Disabled	Enabled
Power-On Default: core supply ON, device out of reset and not programmed	High	High	High	Disabled (Hi-Z)	Enabled	Enabled
On_Doze/ On_Transmit/ On_Receive: core supply ON, device programmed by firmware	High	High	High	Programmed by firmware for each pin: enabled or disabled	Opposite of Output Driver state	Programmed by firmware for each pin: enabled or disabled

6. Clocking

6.1 Low-Power Clock

The ATWINC3400-MR210CA module requires an external 32.768 kHz clock to be supplied at the module pin 20. This clock is used during the sleep operation. The frequency accuracy of this external clock must be within ±200 ppm.

7. CPU and Memory Subsystem

7.1 Processor

The ATWINC3400-MR210CA module has two Cortus APS3 32-bit processors, one is used for Wi-Fi and the other is used for Bluetooth. In IEEE 802.11 mode, the processor performs many of the MAC functions, including but not limited to: association, authentication, power management, security key management, and MSDU aggregation/de-aggregation. In addition, the processor provides flexibility for various modes of operation, such as Station (STA) and Access Point (AP) modes. In Bluetooth mode, the processor handles multiple tasks of the Bluetooth protocol stack.

7.2 Memory Subsystem

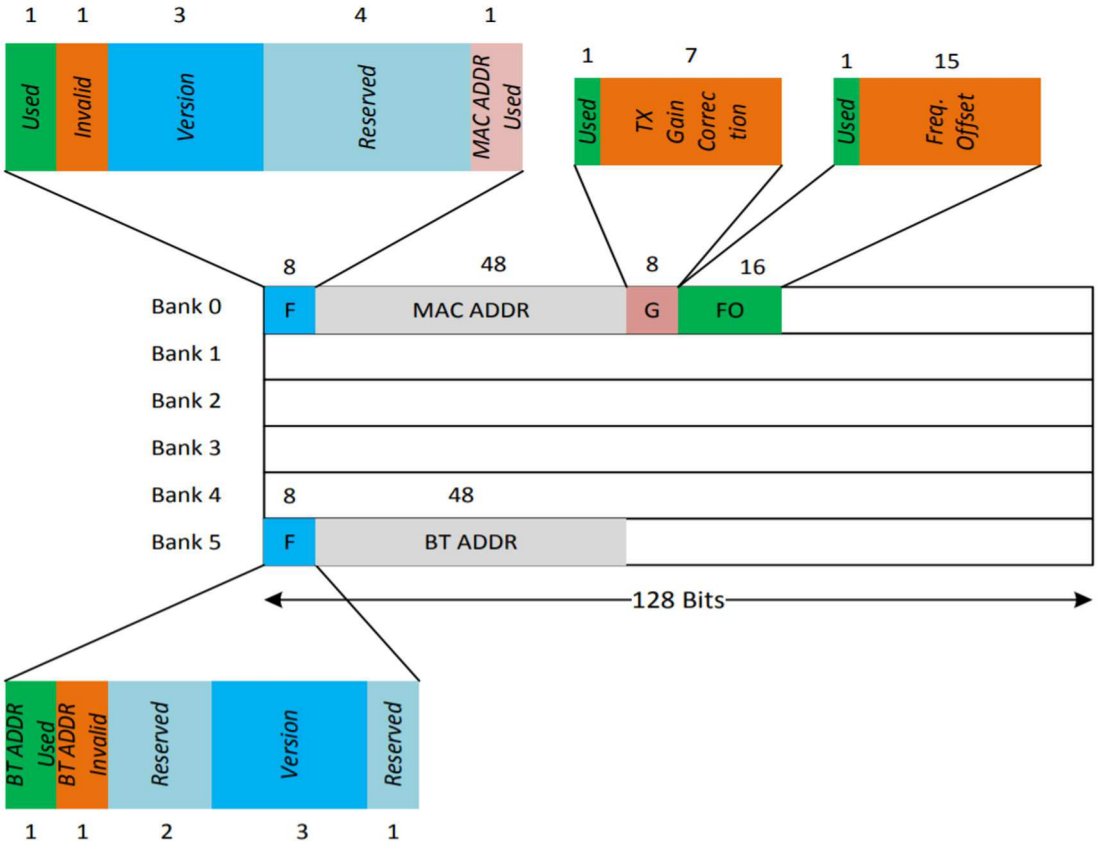
The APS3 core uses a 256 KB instruction/boot ROM (160 KB for IEEE 802.11 and 96 KB for Bluetooth) along with a 420 KB instruction RAM (128 KB for IEEE 802.11 and 292 KB for Bluetooth), and a 128 KB data RAM (64 KB for IEEE 802.11 and 64 KB for Bluetooth). In addition, the device uses a 160 KB shared/exchange RAM (128 KB for IEEE 802.11 and 32 KB for Bluetooth), accessible by the processor and MAC, which allows the processor to perform various data management tasks on the Tx and Rx data packets.

7.3 Nonvolatile Memory

The ATWINC3400-MR210CA module has 768 bits of nonvolatile eFuse memory that can be read by the CPU after device reset. This nonvolatile One-Time-Programmable (OTP) memory can be used to store customer-specific parameters, such as the 802.11 MAC address and Bluetooth address; and various calibration information such as Tx power, crystal frequency offset, and other software-specific configuration parameters. The eFuse is partitioned into six 128-bit banks. The bit map of the first and last banks is shown in the following figure. The purpose of the first 80 bits in bank 0 and the first 56 bits in bank 5 is fixed, and the remaining bits are general-purpose software dependent bits, reserved for future use. Currently, the Bluetooth address is derived from the Wi-Fi MAC address (BT_ADDR=MAC_ADDR +1). This eliminates the need to program the first 56 bits in bank 5. Since each bank and each bit can be programmed independently, this allows for several updates of the device parameters following the initial programming. For example, if the MAC address has to be changed, Bank 1 has to be programmed with the new MAC address along with the values of Tx gain correction and frequency offset if they are used and programmed in the Bank 0. The contents of Bank 0 have to be invalidated in this case by programming the Invalid bit in the Bank 0. This will allow the firmware to use the MAC address from Bank 1.

By default, ATWINC3400-MR210CA modules are programmed with the MAC address and the frequency offset bits of Bank 0.

Figure 7-1. ATWINC3400-MR210CA eFuse Bit Map



8. WLAN Subsystem

The WLAN subsystem is composed of the Media Access Controller (MAC), Physical Layer (PHY), and the radio.

8.1 MAC

The ATWINC3400-MR210CA module is designed to operate at low power, while providing high data throughput. The IEEE 802.11 MAC functions are implemented with a combination of dedicated datapath engines, hardwired control logic, and a low power, high-efficiency microprocessor. The combination of dedicated logic with a programmable processor provides optimal power efficiency and real time response while providing the flexibility to accommodate evolving standards and future feature enhancements.

The dedicated datapath engines are used to implement datapath functions with heavy computational requirements. For example, a Frame Check Sequence (FCS) engine checks the Cyclic Redundancy Check (CRC) of the transmitting and receiving packets, and a cipher engine performs all the required encryption and decryption operations for the WEP, WPA-TKIP, and WPA2 CCMP-AES security requirements.

Control functions, which have real time requirements, are implemented using hardwired control logic modules. These logic modules offer real time response while maintaining configurability through the processor. Examples of hardwired control logic modules are the channel access control module (implements EDCA/HCCA, Beacon Tx control, interframe spacing, and so on), protocol timer module (responsible for the Network Access vector, back-off timing, timing synchronization function, and slot management), MAC Protocol Data Unit (MPDU) handling module, aggregation/deaggregation module, block ACK controller (implements the protocol requirements for burst block communication), and Tx/Rx control Finite State Machine (FSM) (coordinates data movement between PHY and MAC interface, cipher engine, and the Direct Memory Access (DMA) interface to the Tx/Rx FIFOs).

The following are the characteristics of MAC functions implemented solely in software on the microprocessor:

- Functions with high memory requirements or complex data structures. Examples include association table management and power save queuing.
- Functions with low computational load or without critical real time requirements. Examples include authentication and association.
- Functions that require flexibility and upgradeability. Examples include beacon frame processing and QoS scheduling.

Features

The ATWINC3400-MR210CA MAC supports the following functions:

- IEEE 802.11b/g/n
- IEEE 802.11e WMM QoS EDCA/HCCA/PCF multiple access categories traffic scheduling
- Advanced IEEE 802.11n features:
  - Transmission and reception of aggregated MPDUs (A-MPDU)
  - Transmission and reception of aggregated MSDUs (A-MSDU)
  - Immediate block acknowledgment
  - Reduced Interframe Spacing (RIFS)
- IEEE 802.11i and WFA security with key management:

  - WEP 64/128
  - WPA-TKIP
  - 128-bit WPA2 CCMP (AES)
- Advanced power management:
  - Standard IEEE 802.11 power save mode
- RTS-CTS and CTS-self support
- Either STA or AP mode in the infrastructure basic service set mode

8.2 PHY

The ATWINC3400-MR210CA module WLAN PHY is designed to achieve reliable and power-efficient physical layer communication specified by IEEE 802.11 b/g/n in single stream mode with 20 MHz bandwidth. The advanced algorithms are used to achieve maximum throughput in a real world communication environment with impairments and interference. The PHY implements all the required functions such as Fast Fourier Transform (FFT), filtering, Forward Error Correction (FEC) that is a Viterbi decoder, frequency, timing acquisition and tracking, channel estimation and equalization, carrier sensing, clear channel assessment and automatic gain control.

Features

The IEEE 802.11 PHY supports the following functions:

- Single antenna 1x1 stream in 20 MHz channels
- Supports IEEE 802.11b DSSS-CCK modulation: 1, 2, 5.5, and 11 Mbps
- Supports IEEE 802.11g OFDM modulation: 6, 9, 12,18, 24, 36, 48, and 54 Mbps
- Supports IEEE 802.11n HT modulations MCS0-7, 20 MHz, 800 and 400ns guard interval: 6.5, 7.2, 13.0, 14.4, 19.5, 21.7, 26.0, 28.9, 39.0, 43.3, 52.0, 57.8, 58.5, 65.0, and 72.2 Mbps
- IEEE 802.11n mixed mode operation
- Per packet Tx power control
- Advanced channel estimation/equalization, automatic gain control, CCA, carrier/symbol recovery and frame detection

8.3 Radio

This section presents information describing the properties and characteristics of the ATWINC3400-MR210CA and Wi-Fi radio transmit and receive performance capabilities of the device.

The performance measurements are taken at the RF pin assuming 50Ω impedance; the RF performance is guaranteed for room temperature of 25ºC with a derating of 2-3 dB at boundary conditions.

Measurements were taken under typical conditions: VBATT=3.3V; VDDIO=3.3V; temperature: +25ºC

Table 8-1. Features and Properties

Feature	Description
Part Number	ATWINC3400-MR210CA
WLAN Standard	IEEE 802.11 b/g/n, Wi-Fi compliant
Host Interface	SPI