Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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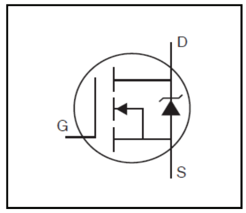
HEXFET® Power MOSFET

Features

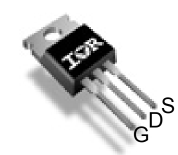
- Advanced Planar Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified *



V_{DSS}	75V
$R_{DS(on)}$ max.	4.5mΩ
I_D (Silicon Limited)	170A
I_D (Package Limited)	75A

Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating . These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications



TO-220AB
AUIRF2907Z

G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRF2907Z	TO-220	Tube	50	AUIRF2907Z

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	170	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	120	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Package Limited)	75	
I_{DM}	Pulsed Drain Current ①	600	
P_D @T_C = 25°C	Maximum Power Dissipation	300	W
	Linear Derating Factor	2.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy (Thermally Limited) ②	270	mJ
E_{AS} (Tested)	Single Pulse Avalanche Energy Tested Value ⑦	690	
I_{AR}	Avalanche Current ①	See Fig.15,16, 12a, 12b	A
E_{AR}	Repetitive Avalanche Energy ⑥		mJ
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧	——	0.50⑨	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface ⑦	0.50	——	
$R_{\theta JA}$	Junction-to-Ambient ⑦	——	62	

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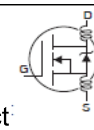
*Qualification standards can be found at www.infineon.com

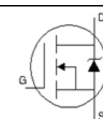
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	75	——	——	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.069	——	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	3.5	4.5	mΩ	V_{GS} = 10V, I_D = 75A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
gfs	Forward Trans conductance	180	——	——	S	V_{DS} = 10V, I_D = 75A
I_{DSS}	Drain-to-Source Leakage Current	——	——	20	µA	V_{DS} = 75V, V_{GS} = 0V
		——	——	250		V_{DS} =75V,V_{GS} = 0V,T_J =125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-200		V_{GS} = -20V

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge	——	180	270	nC	I_D = 75A
Q_{gs}	Gate-to-Source Charge	——	46	——		V_{DS} = 60V
Q_{gd}	Gate-to-Drain Charge	——	65			V_{GS} = 10V ④
$t_{d(on)}$	Turn-On Delay Time	——	19	——	ns	V_{DD} = 38V
t_r	Rise Time	——	140	——		I_D = 75A
$t_{d(off)}$	Turn-Off Delay Time	——	97	——		R_G= 2.5Ω
t_f	Fall Time	——	100	——		V_{GS} = 10V ④
L_D	Internal Drain Inductance	——	5.0	——	nH	Between lead, 6mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	——	13	——		
C_{iss}	Input Capacitance	——	7500	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	970	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	510	——		ƒ = 1.0MHz, See Fig. 5
C_{oss}	Output Capacitance	——	3640	——		V_{GS} = 0V, V_{DS} = 1.0V ƒ = 1.0MHz
C_{oss}	Output Capacitance	——	650	——		V_{GS} = 0V, V_{DS} = 60V ƒ = 1.0MHz
$C_{oss\ eff.}$	Effective Output Capacitance	——	1020	——		V_{GS} = 0V, V_{DS} = 0V to 60V

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	75	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	680		
V_{SD}	Diode Forward Voltage	——	——	1.3	V	T_J = 25°C,I_S = 75A ,V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	41	61	ns	T_J = 25°C ,I_F = 75A ,V_{DD} = 38V
Q_{rr}	Reverse Recovery Charge	——	59	89	nC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.095mH, R_G = 25Ω, I_{AS} = 75A, V_{GS} =10V. Part not recommended for use above this value.
③ I_{SD} ≤ 75A, di/dt ≤ 340A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C.
④ Pulse width ≤ 1.0ms; duty cycle ≤ 2%.
⑤ Coss eff. is a fixed capacitance that gives the same charging time as Coss while V_{DS} is rising from 0 to 80% V_{DSS}.
⑥ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
⑦ This value determined from sample failure population, starting T_J = 25°C, L = 0.095mH, R_G = 25Ω, I_{AS} = 75A, V_{GS} =10V.
⑧ R_θ is measured at T_J of approximately 90°C.
⑨ TO-220 device will have an Rth of 0.45°C/W.

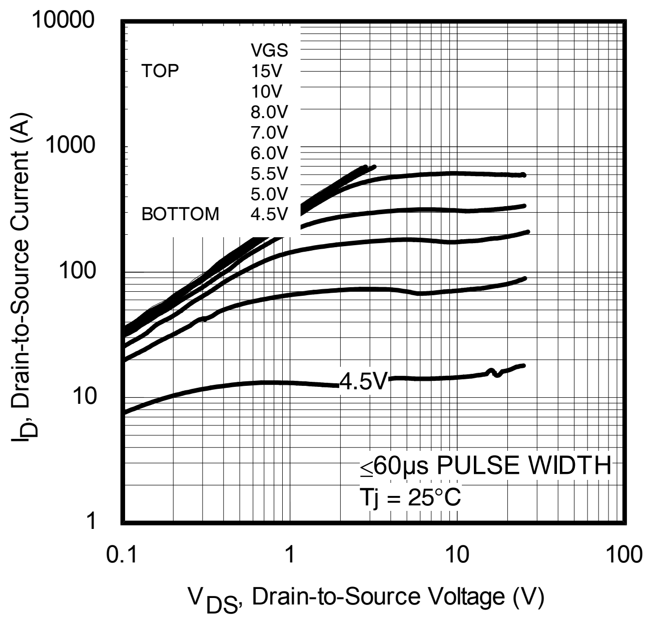


Fig. 1 Typical Output Characteristics

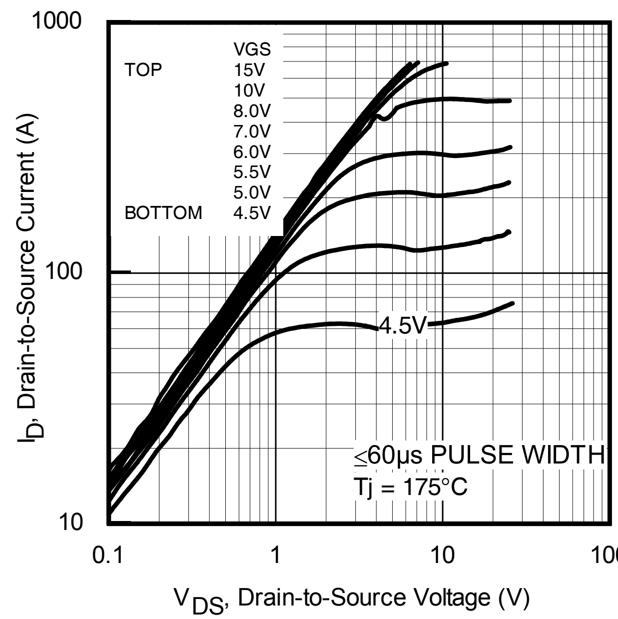


Fig. 2 Typical Output Characteristics

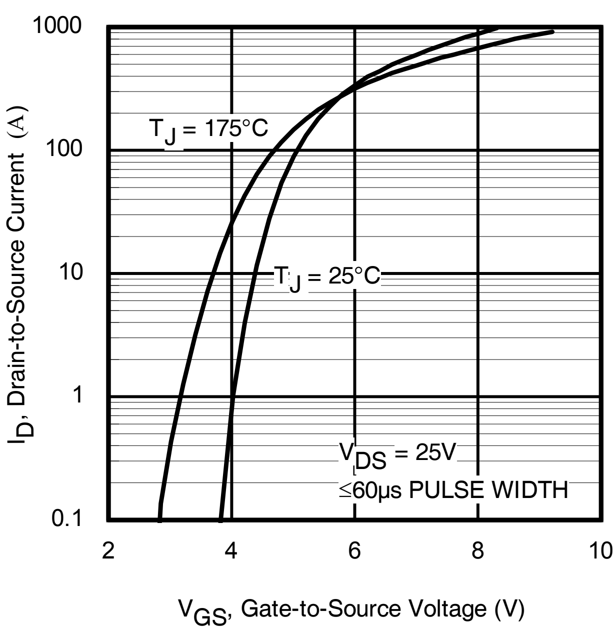


Fig. 3 Typical Transfer Characteristics

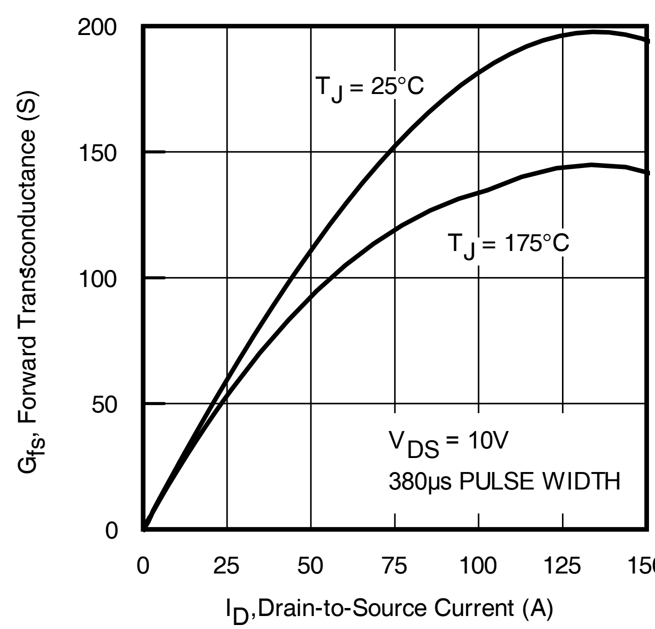


Fig. 4 Typical Forward Transconductance Vs. Drain Current

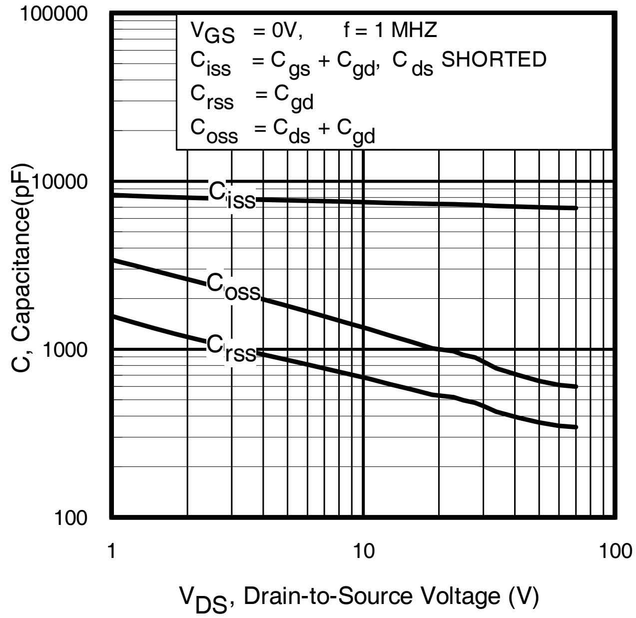


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

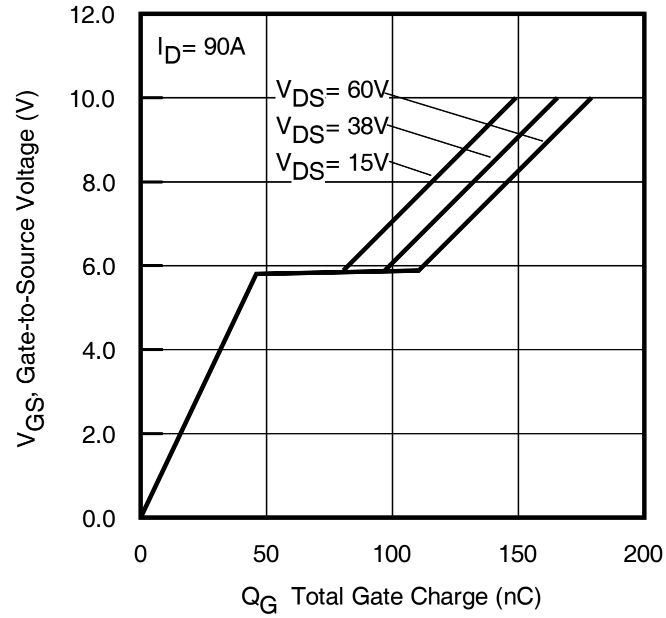


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

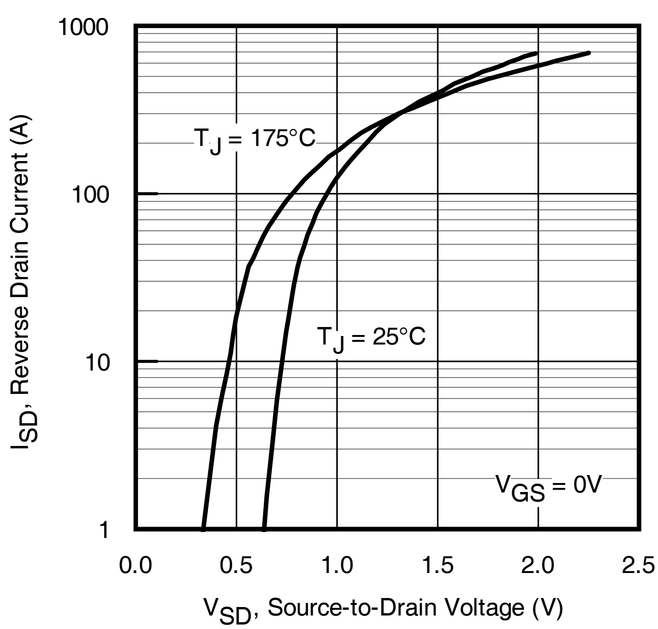


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

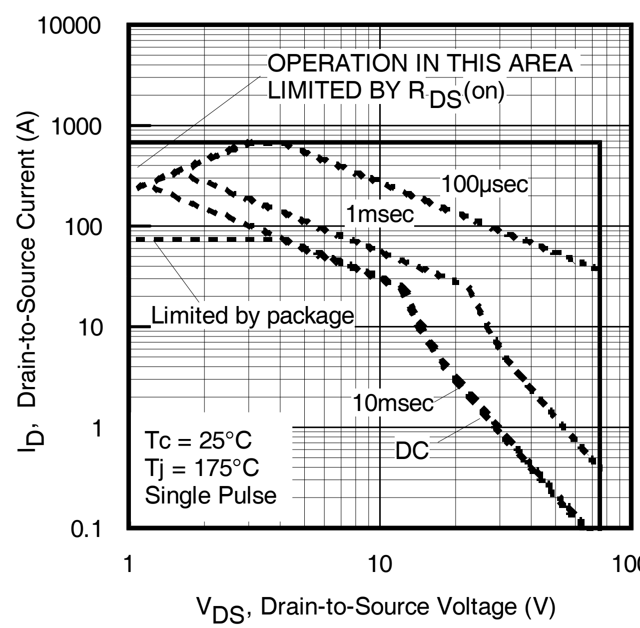


Fig 8. Maximum Safe Operating Area

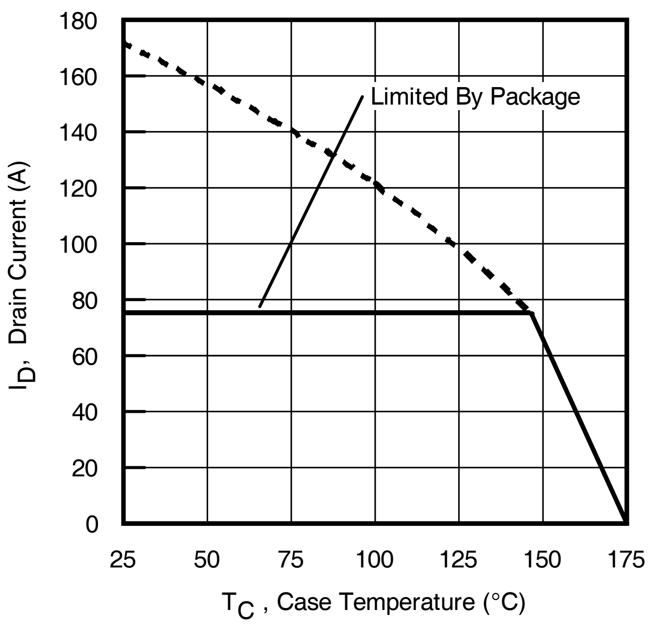


Fig 9. Maximum Drain Current vs. Case Temperature

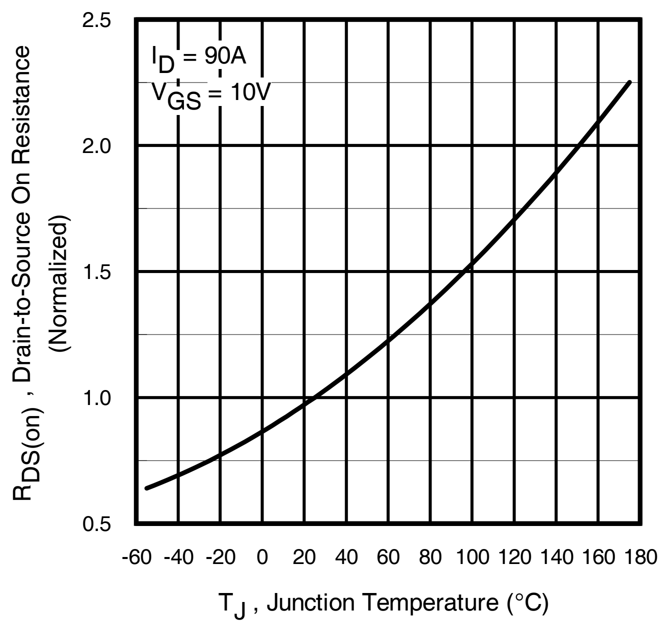


Fig 10. Normalized On-Resistance
Vs. Temperature

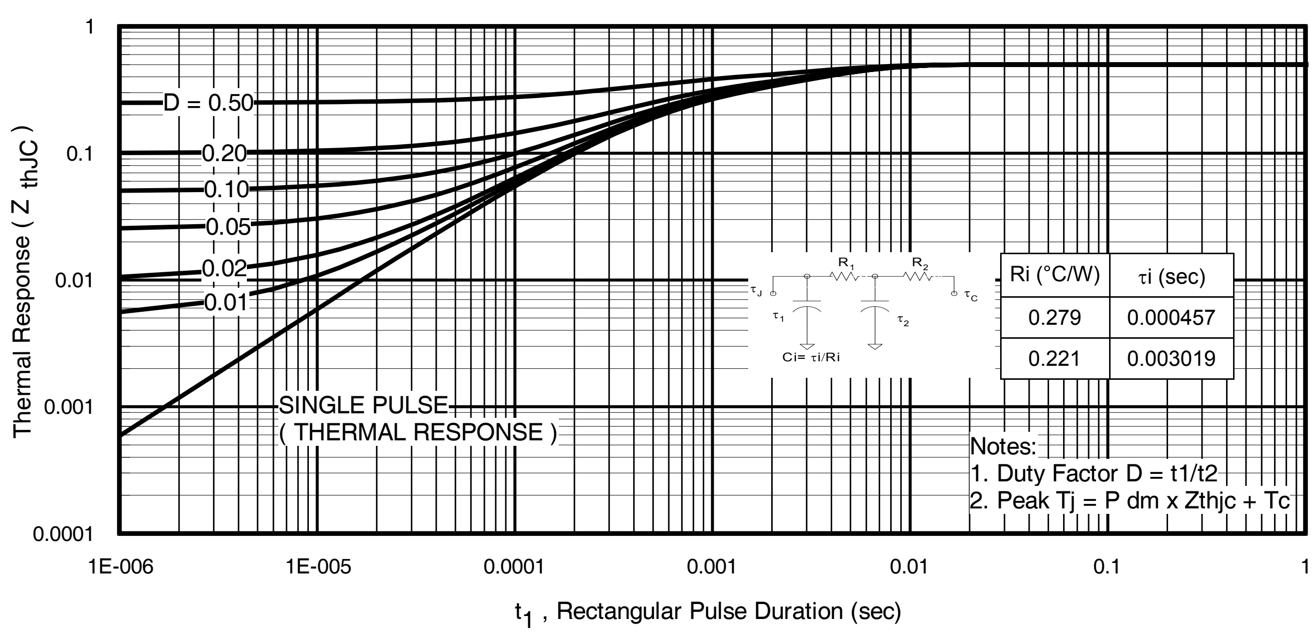


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

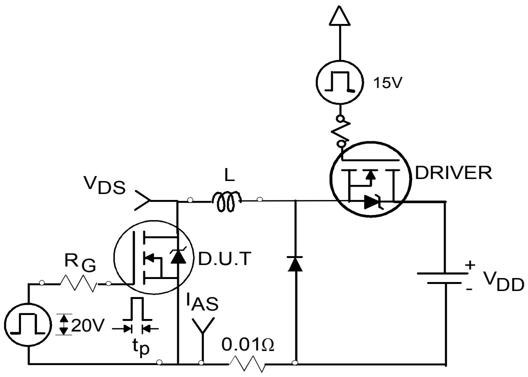


Fig 12a. Unclamped Inductive Test Circuit

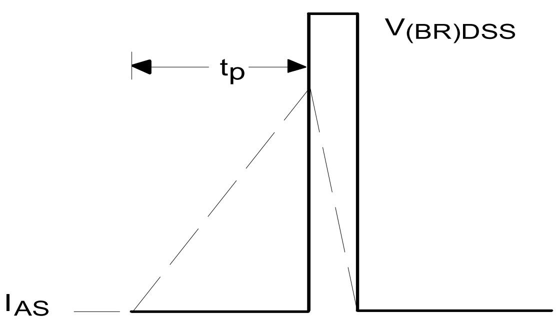


Fig 12b. Unclamped Inductive Waveforms

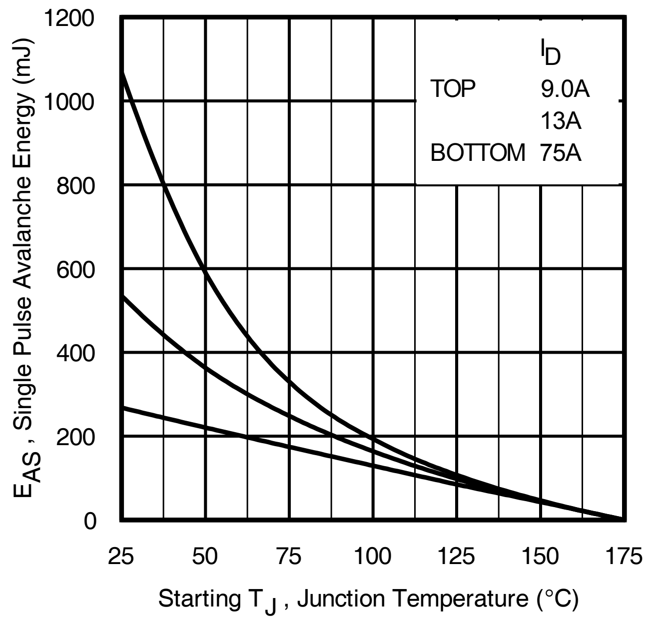


Fig 12c. Maximum Avalanche Energy vs. Drain Current

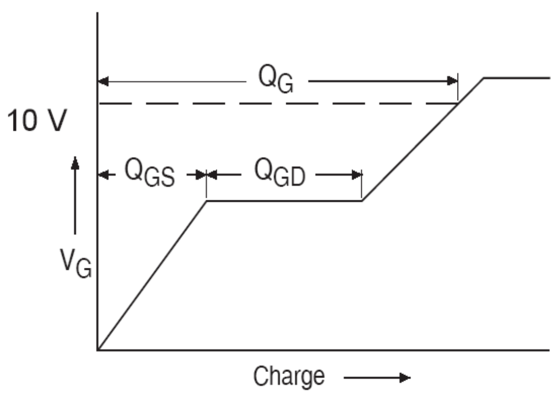


Fig 13a. Gate Charge Waveform

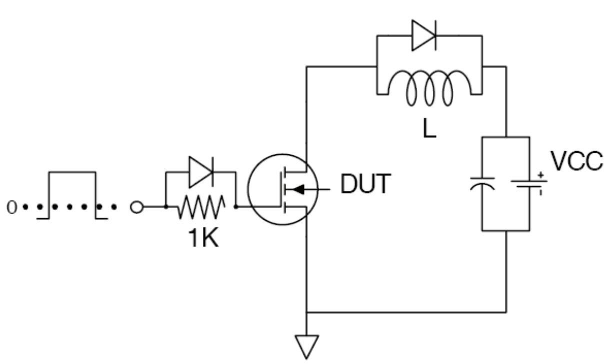


Fig 13b. Gate Charge Test Circuit

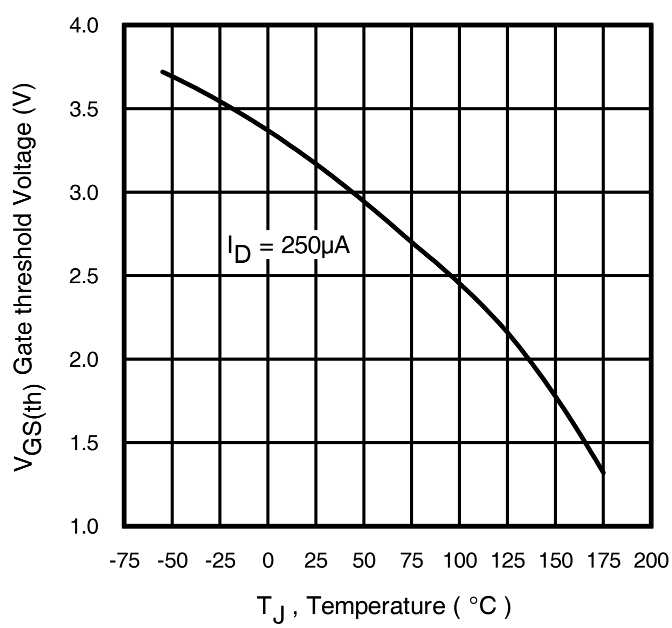


Fig 14. Threshold Voltage vs. Temperature

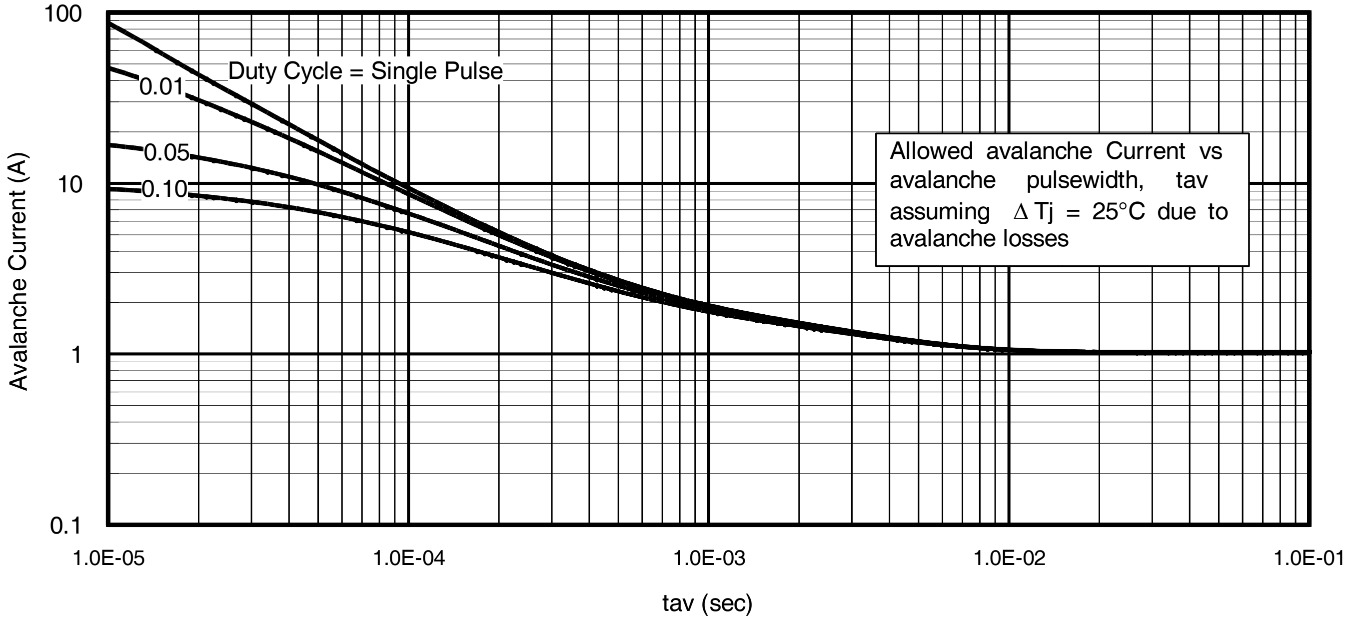


Fig 15. Typical Avalanche Current vs. Pulse width

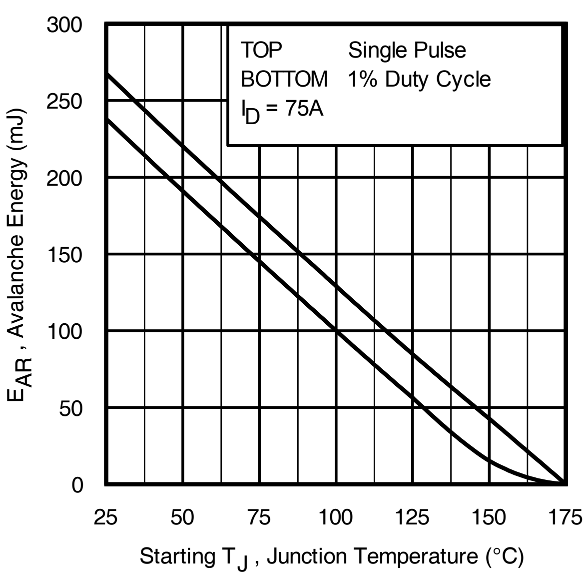


Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.infineon.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 11)

$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

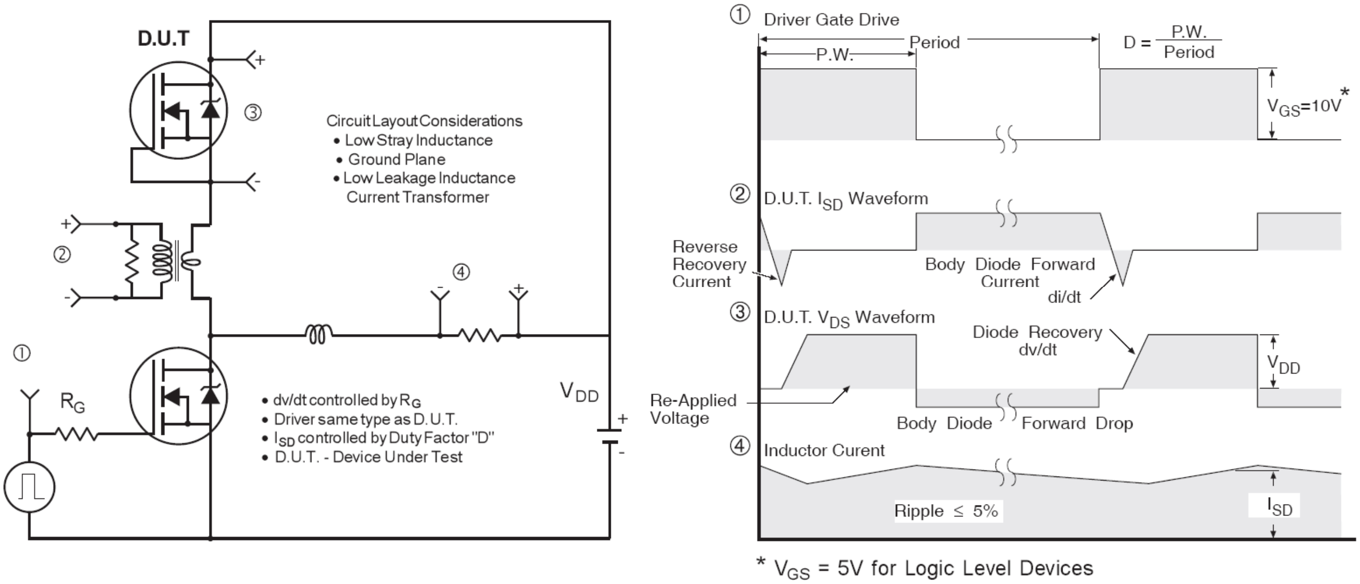


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

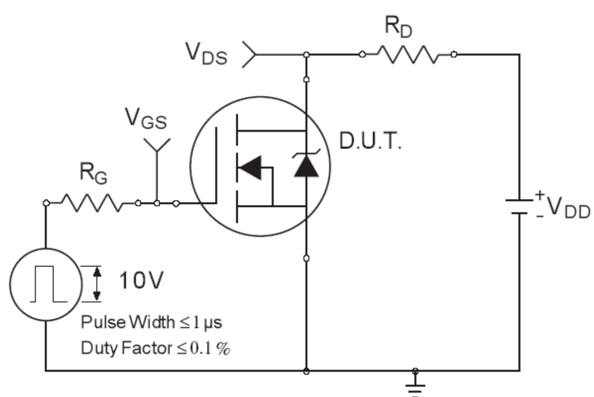


Fig 18a. Switching Time Test Circuit

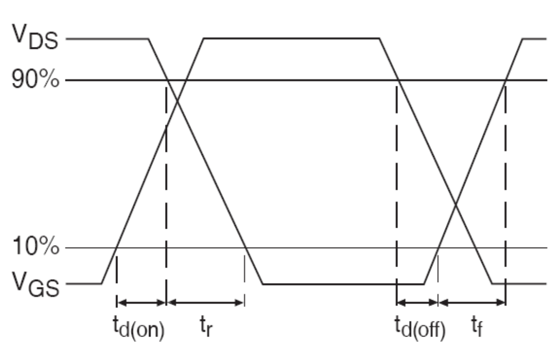
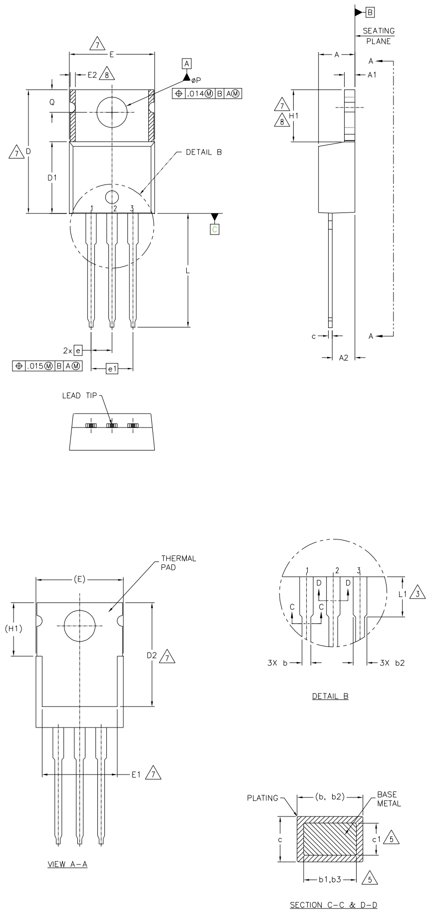


Fig 18b. Switching Time Waveforms

TO-220AB Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

1.– DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M– 1994.
2.– DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
3.– LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
4.– DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5.– DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
6.– CONTROLLING DIMENSION : INCHES.
7.– THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
8.– DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
9.– OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	1.14	1.40	.045	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	–	0.76	–	.030	8
e	2.54 BSC		.100 BSC		
e1	5.08 BSC		.200 BSC		
H1	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	3
øP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

LEAD ASSIGNMENTS

HEXFET

1.– GATE
2.– DRAIN
3.– SOURCE

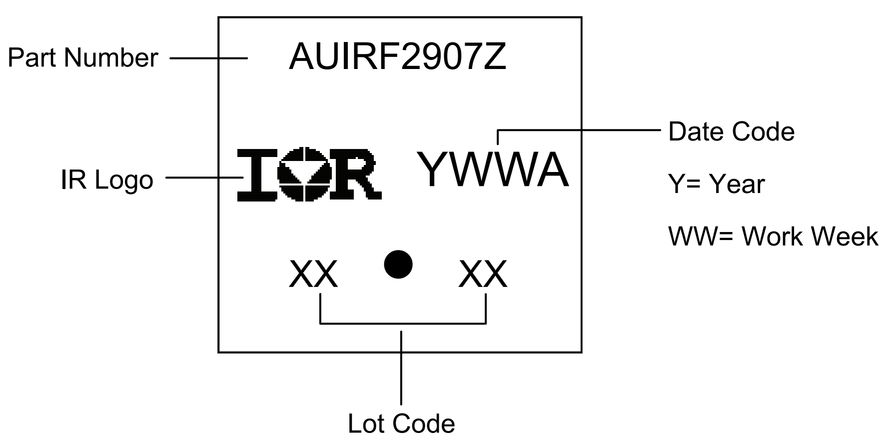
IGBTs, CoPACK

1.– GATE
2.– COLLECTOR
3.– EMITTER

DIODES

1.– ANODE
2.– CATHODE
3.– ANODE

TO-220AB Part Marking Information



TO-220AB package is not recommended for Surface Mount Application.

Qualification Information

<table>
<tr><td rowspan="2">Qualification Level</td><td colspan="3">Automotive
(per AEC-Q101)</td></tr>
<tr><td colspan="3">Comments: This part number(s) passed Automotive qualification. Infineon’s Industrial and Consumer qualification level is granted by extension of the higher Automotive level.</td></tr>
<tr><td colspan="2">Moisture Sensitivity Level</td><td>TO-220AB</td><td>N/A</td></tr>
<tr><td rowspan="3">ESD</td><td>Machine Model</td><td colspan="2">Class M4 (+/- 425V)†
AEC-Q101-002</td></tr>
<tr><td>Human Body Model</td><td colspan="2">Class H2 (+/- 4000V)†
AEC-Q101-001</td></tr>
<tr><td>Charged Device Model</td><td colspan="2">Class C4 (+/- 1000V)†
AEC-Q101-005</td></tr>
<tr><td colspan="2">RoHS Compliant</td><td colspan="2">Yes</td></tr>
</table>

† Highest passing voltage.

Revision History

Date	Comments
9/21/2017	• Updated datasheet with corporate template. • Corrected typo error on package outline and part marking on page 9.

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