Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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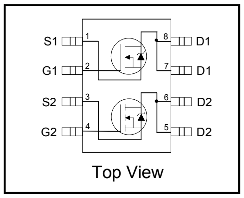
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



V_{DSS}	**50V**
$R_{DS(on)}$ max.	**130mΩ**
I_D	**3.0A**

SO-8
AUIRF7103Q

G	D	S
Gate	Drain	Source

Features

- Advanced Planar Technology
- Dual N Channel MOSFET
- Low On-Resistance
- Logic Level Gate Drive
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified *

Description

Specifically designed for Automotive applications, this cellular design of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve low on-resistance per silicon area. This benefit combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in Automotive and a wide variety of other applications.

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRF7103Q	SO-8	Tape and Reel	4000	AUIRF7103QTR

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 4.5V	3.0	A
I_D @ T_A = 70°C	Continuous Drain Current, V_{GS} @ 4.5V	2.5	
I_{DM}	Pulsed Drain Current ①	25	
P_D @T_A = 25°C	Maximum Power Dissipation ③	2.4	W
	Linear Derating Factor	16	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy (Thermally Limited) ④	22	mJ
I_{AR}	Avalanche Current ①	See Fig.19,20, 16b, 16c	A
E_{AR}	Repetitive Avalanche Energy ⑥		mJ
dv/dt	Peak Diode Recovery dv/dt ⑤	12	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JL}$	Junction-to-Drain Lead	——	20	°C/W
$R_{\theta JA}$	Junction-to-Ambient ④⑤	——	62.5	

HEXFET® is a registered trademark of Infineon.
*Qualification standards can be found at www.infineon.com

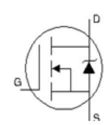
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	50	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.057	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	130	mΩ	V_{GS} = 10V, I_D = 3.0A ②
		—	—	200		V_{GS} = 4.5V, I_D = 1.5A ②
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	3.0	V	V_{DS} = V_{GS}, I_D = 250µA
gfs	Forward Trans conductance	3.4	—	—	S	V_{DS} = 15V, I_D = 3.0A
I_{DSS}	Drain-to-Source Leakage Current	—	—	2.0	µA	V_{DS} =40V, V_{GS} = 0V
		—	—	25		V_{DS} = 40V,V_{GS} = 0V,T_J =55°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Q_g	Total Gate Charge	—	10	15	nC	I_D = 2.0A
Q_{gs}	Gate-to-Source Charge	—	1.2	—		V_{DS} = 40V
Q_{gd}	Gate-to-Drain Charge	—	2.8	—		V_{GS} = 10V
$t_{d(on)}$	Turn-On Delay Time	—	5.1	—	ns	V_{DD} = 25V
t_r	Rise Time	—	1.7	—		I_D = 1.0A
$t_{d(off)}$	Turn-Off Delay Time	—	15	—		R_G = 6.0Ω
t_f	Fall Time	—	2.3	—		R_D = 25Ω ②
C_{iss}	Input Capacitance	—	255	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	69	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	29	—		f = 1.0MHz

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	3.0	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	12		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	T_J = 25°C,I_S = 1.5A,V_{GS} = 0V ②
t_{rr}	Reverse Recovery Time	—	35	53	ns	T_J = 25°C ,I_F = 1.5A,
Q_{rr}	Reverse Recovery Charge	—	45	67	nC	di/dt = 100A/µs ②
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.
② Pulse width ≤ 400µs; duty cycle ≤ 2%.
③ Surface mounted on 1" in square Cu board.
④ Starting T_J = 25°C, L = 4.9mH, R_G = 25Ω, I_{AS} = 3.0A. (See Fig. 12)
⑤ I_{SD} ≤ 2.0A, di/dt ≤ 155A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C.
⑥ Limited by T_{Jmax} , see Fig.16b, 16c, 19, 20 for typical repetitive avalanche performance.

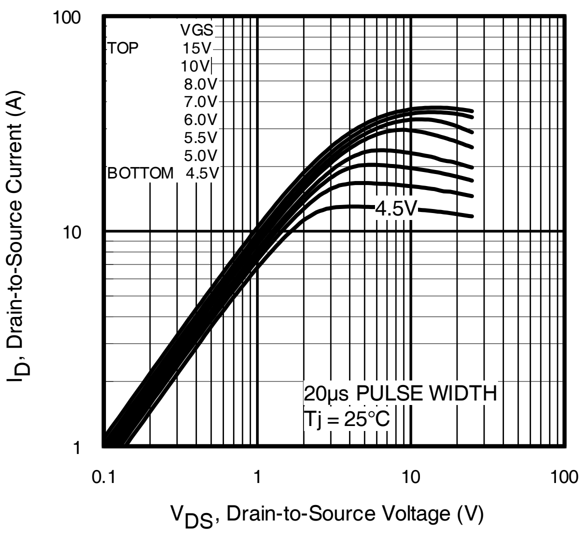


Fig. 1 Typical Output Characteristics

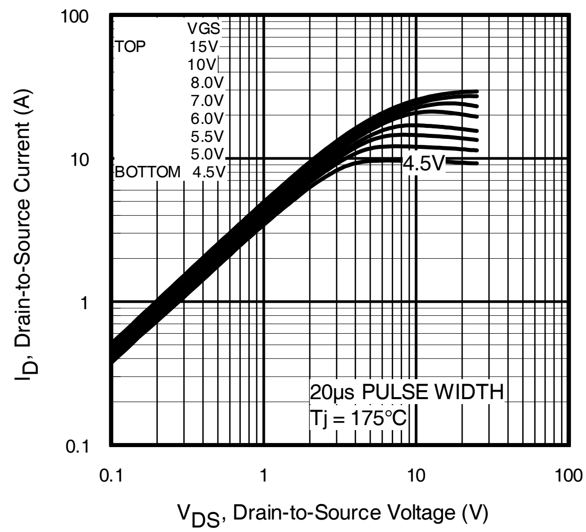


Fig. 2 Typical Output Characteristics

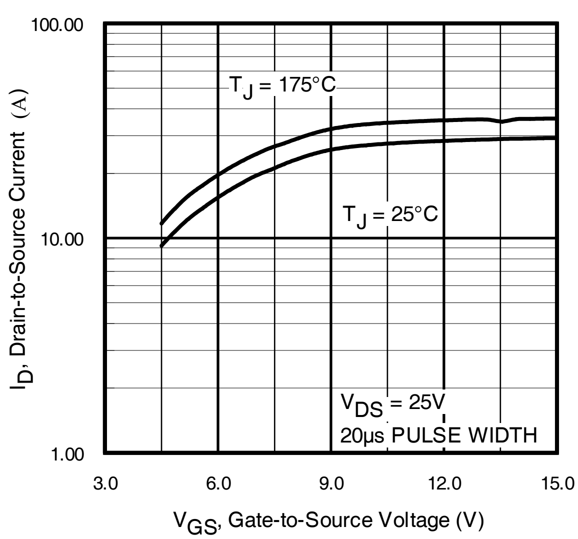


Fig. 3 Typical Transfer Characteristics

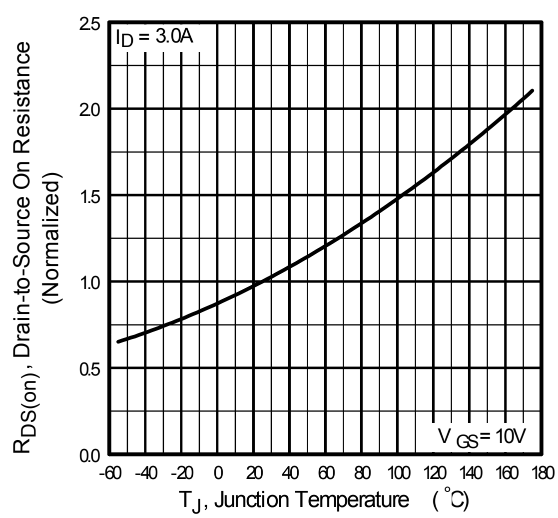


Fig. 4 Normalized On-Resistance vs. Temperature

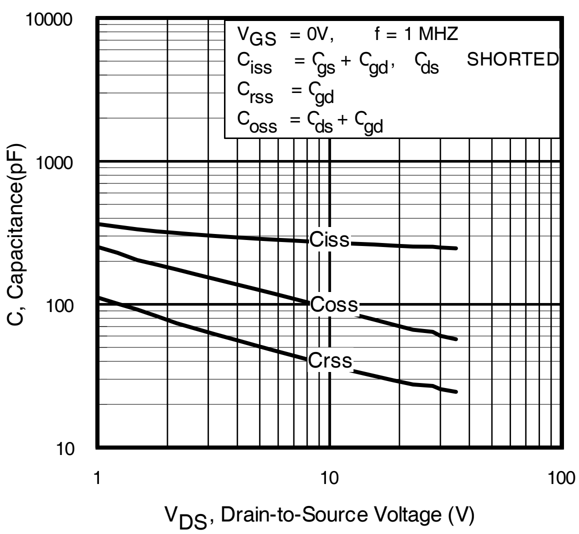


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

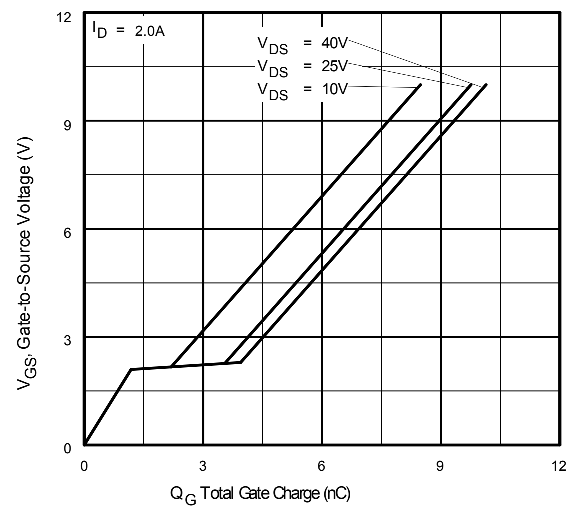


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

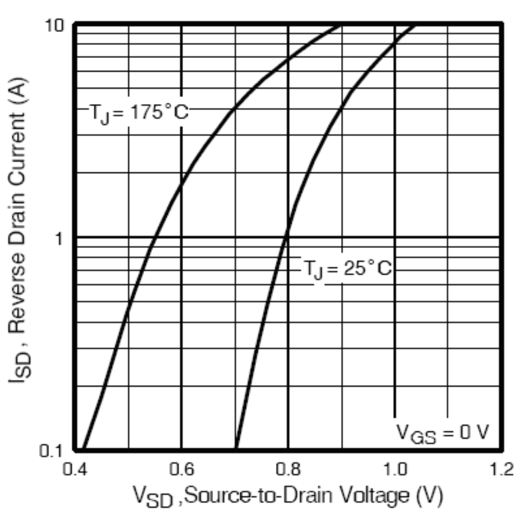


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

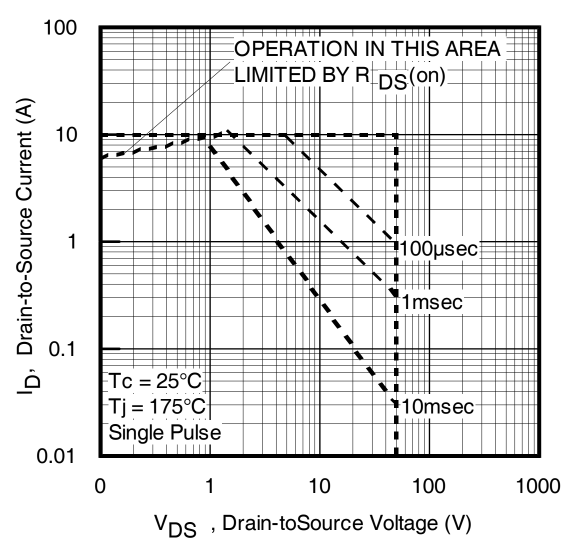


Fig 8. Maximum Safe Operating Area

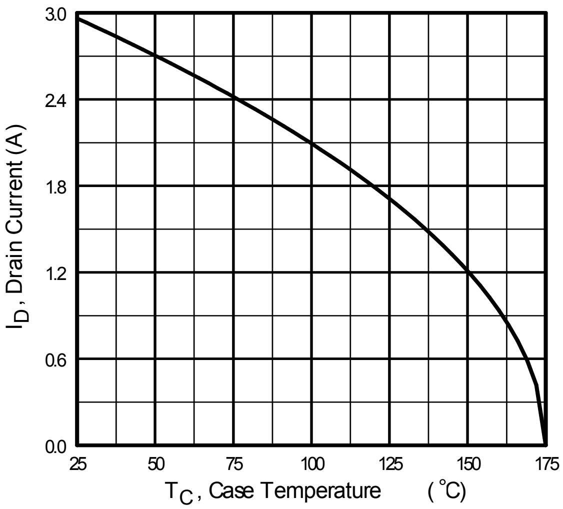


Fig 9. Maximum Drain Current vs. Case Temperature

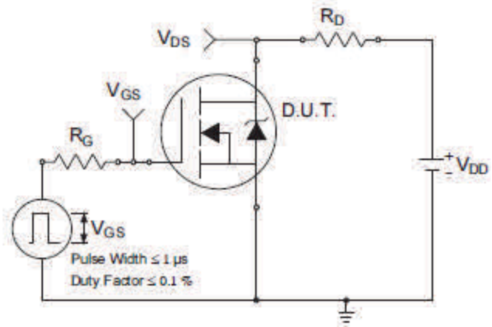


Fig 10a. Switching Time Test Circuit

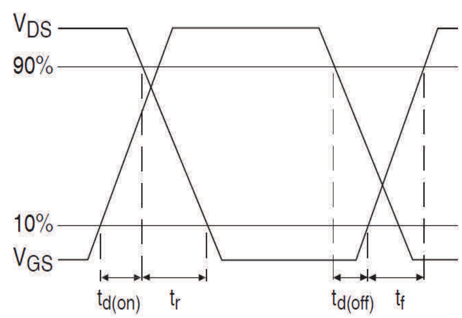


Fig 10b. Switching Time Waveforms

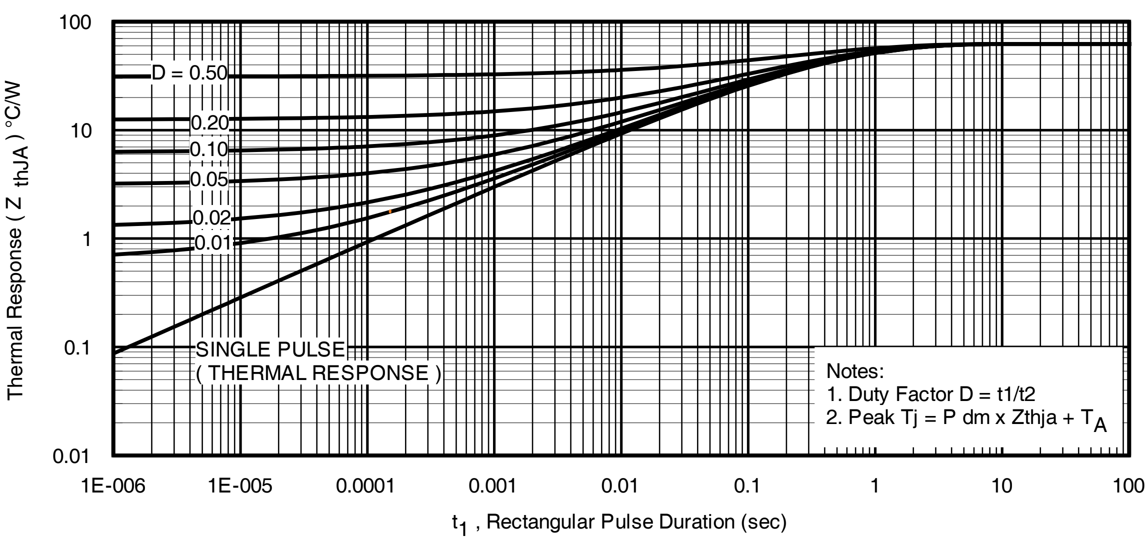


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

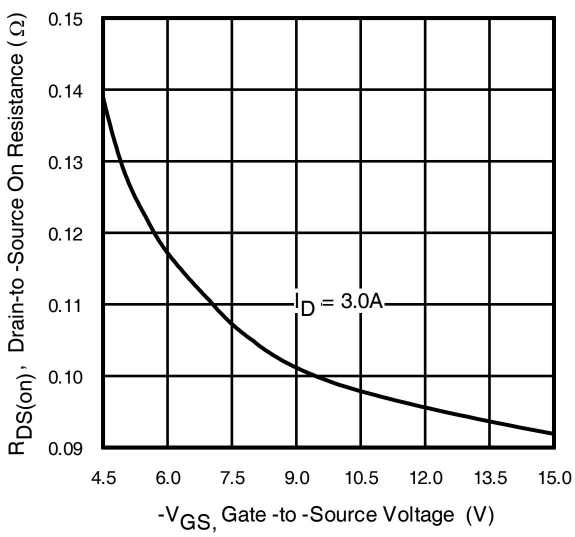


Fig 12. Typical On-Resistance Vs. Gate Voltage

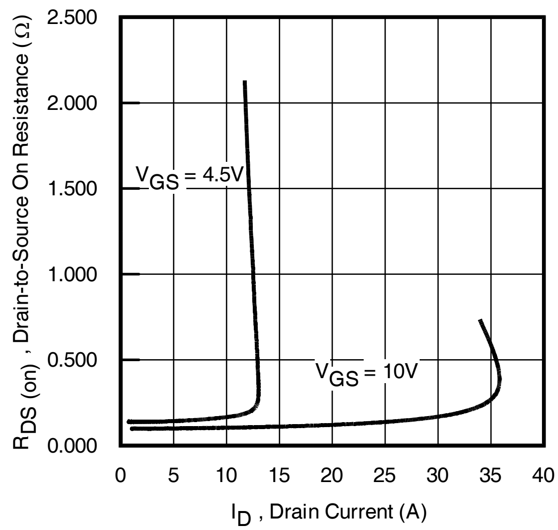


Fig 13. Typical On-Resistance Vs. Drain Current

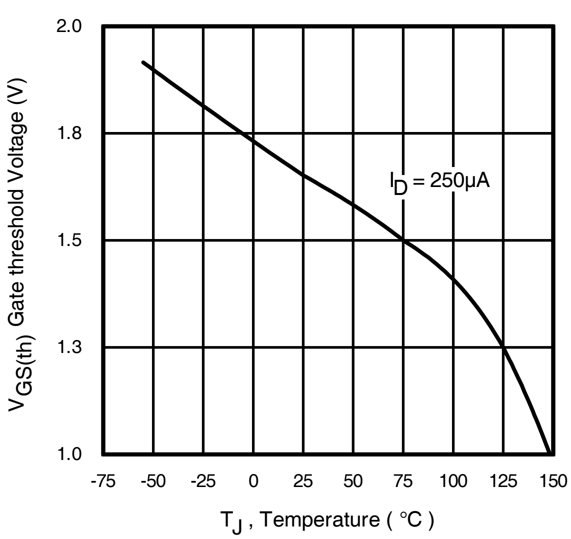


Fig. 14. Typical Threshold Voltage Vs. Junction Temperature

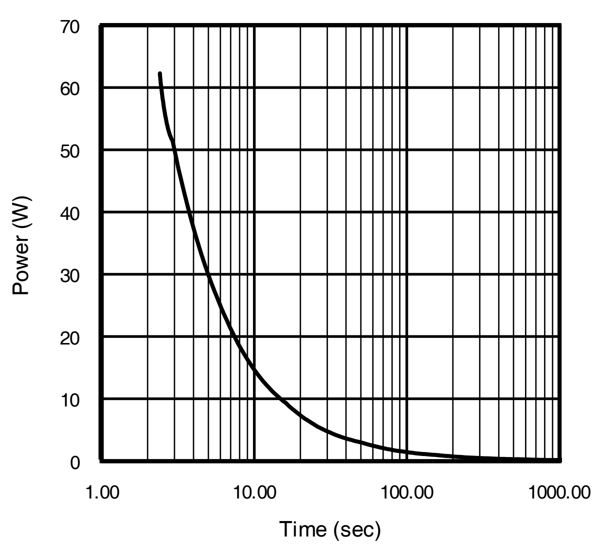


Fig 15. Typical Power Vs. Time

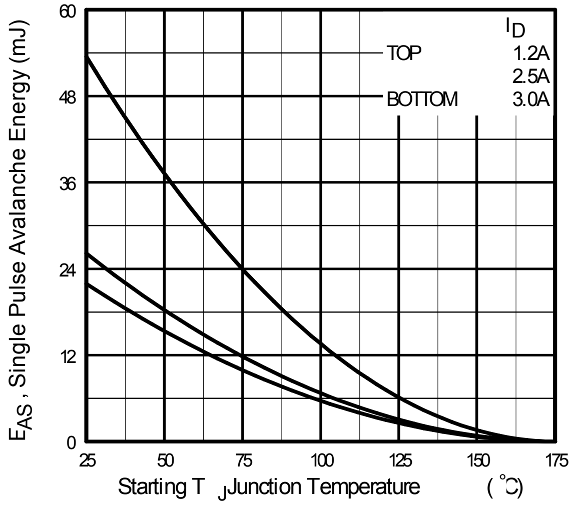


Fig 16a. Maximum Avalanche Energy vs. Drain Current

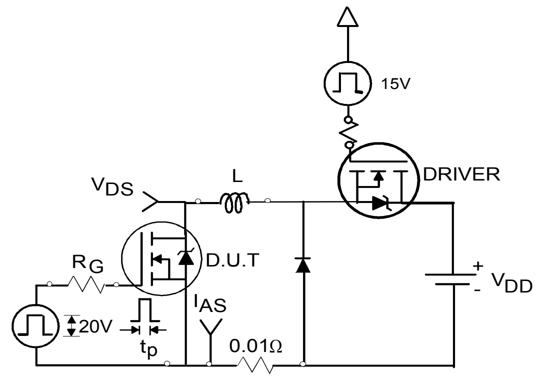


Fig 16b. Unclamped Inductive Test Circuit

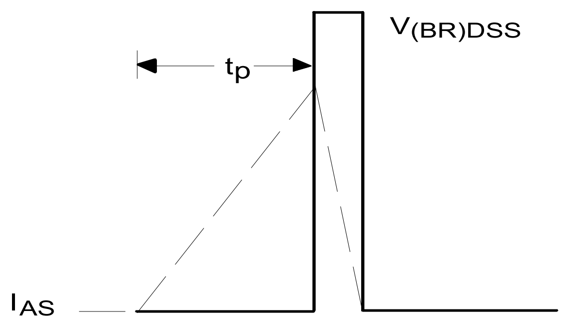


Fig 16c. Unclamped Inductive Waveforms

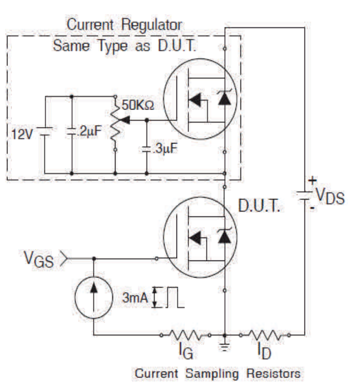


Fig 17. Gate Charge Test Circuit

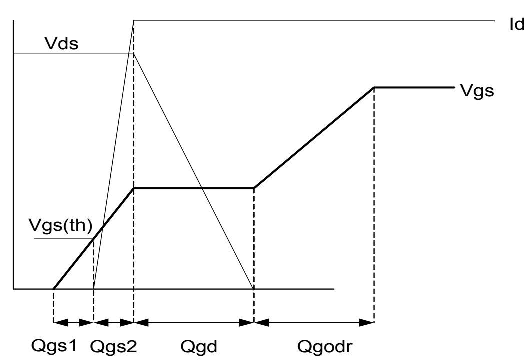


Fig 18. Basic Gate Charge Waveform

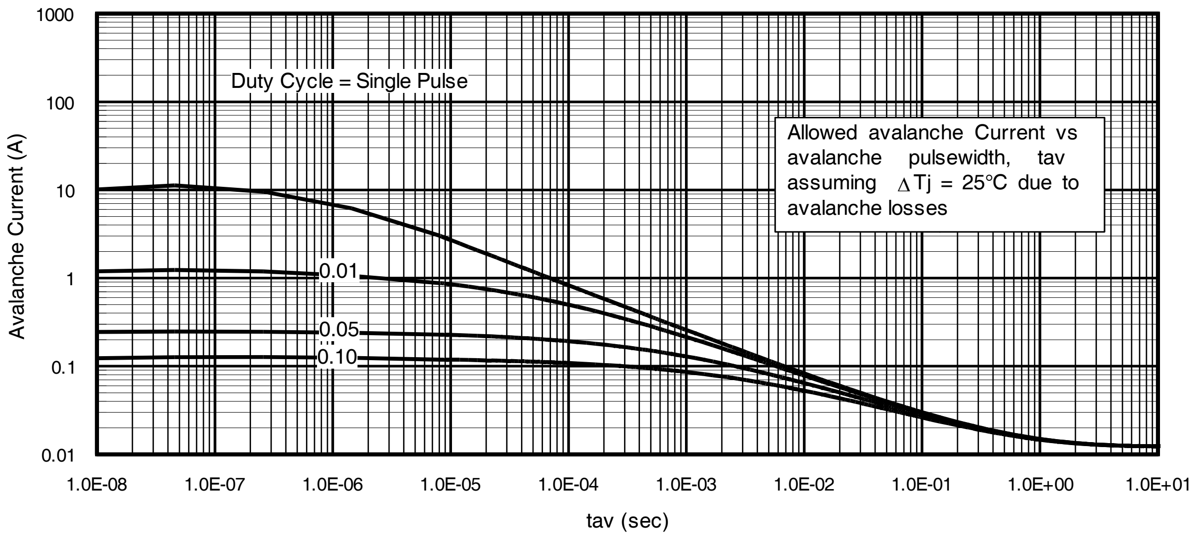


Fig 19. Typical Avalanche Current vs. Pulse width

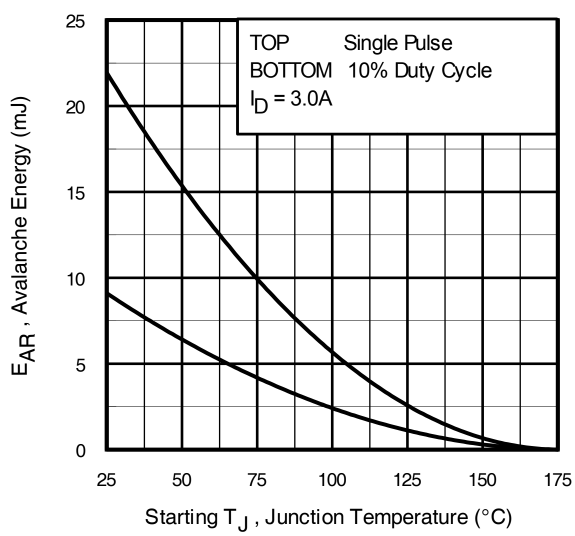


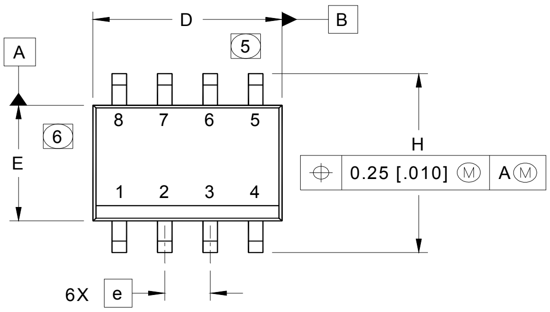
Fig 20. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 19, 20:
(For further info, see AN-1005 at www.infineon.com)

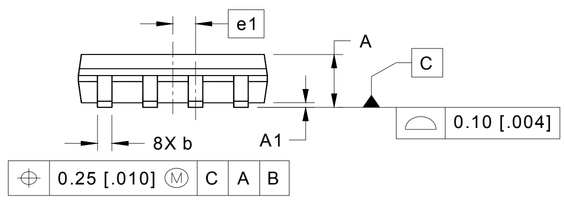
1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16b, 16c.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 11, 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 11)

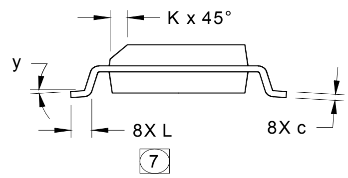
$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

SO-8 Package Outline (Dimensions are shown in millimeters (inches))

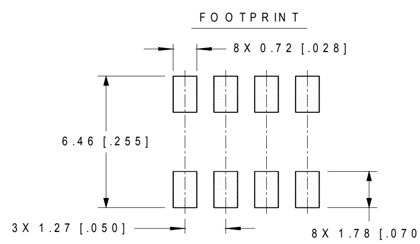


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

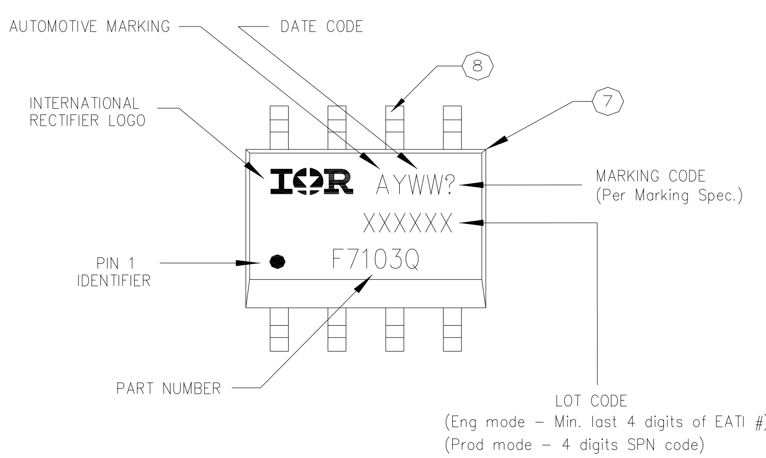




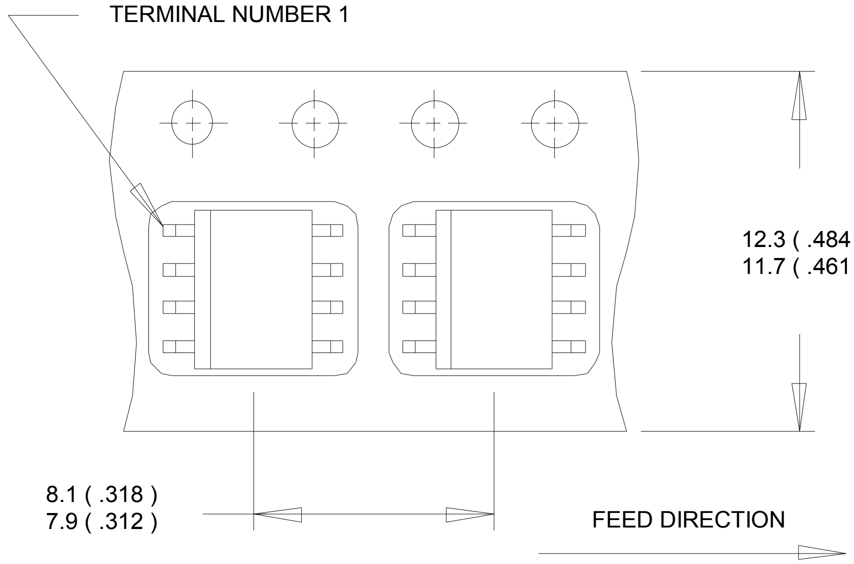
NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.



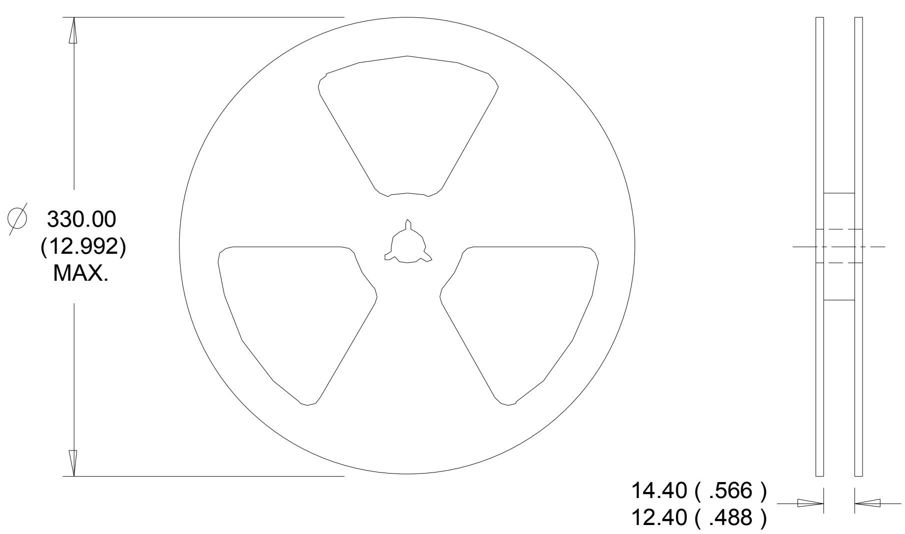
SO-8 Part Marking Information



SO-8 Tape and Reel (Dimensions are shown in millimeters (inches)



NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Qualification Information

Qualification Level		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		SO-8	MSL1
ESD	Machine Model	Class M1A (+/- 50V)† AEC-Q101-002	
	Human Body Model	Class H0 (+/- 250V)† AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 1125V)† AEC-Q101-005	
RoHS Compliant		Yes	

† Highest passing voltage.

Revision History

Date	Comments
4/3/2014	• Added "Logic Level Gate Drive" bullet in the features section on page 1 • Updated data sheet with new IR corporate template
9/30/2015	• Updated datasheet with corporate template • Corrected ordering table on page 1.

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