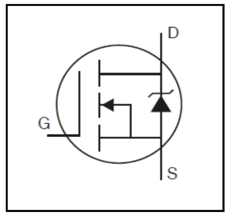
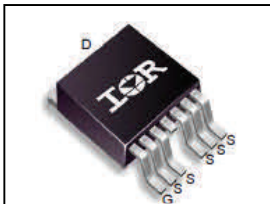
HEXFET® Power MOSFET

Features

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dV/dT Rating
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified *



V_{DSS}		150V
$R_{DS(on)}$	typ.	10mΩ
	max.	11.8mΩ
I_D		105A



D2Pak 7 Pin

G	D	S
Gate	Drain	Source

Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating . These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRFS4115-7P	D^2Pak 7 Pin	Tube	50	AUIRFS4115-7P
		Tape and Reel Left	800	AUIRFS4115-7TRL

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	105	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	74	
I_{DM}	Pulsed Drain Current ①	420	
P_D @T_C = 25°C	Maximum Power Dissipation	380	W
	Linear Derating Factor	2.5	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy (Thermally Limited) ②	230	mJ
I_{AR}	Avalanche Current ①	See Fig.14,15, 22a, 22b	A
E_{AR}	Repetitive Avalanche Energy ①		mJ
dv/dt	Peak Diode Recovery ③	32	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧⑨	——	0.40	°C/W
$R_{\theta JA}$	Junction-to-Ambient ⑦	——	40	

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*Qualification standards can be found at www.infineon.com

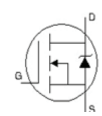
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	150	—	—	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.18	—	V/°C	Reference to 25°C, I_D = 3.5mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	10	11.8	mΩ	V_{GS} = 10V, I_D = 63A ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	V_{DS} = V_{GS}, I_D = 250μA
gfs	Forward Trans conductance	93	—	—	S	V_{DS} = 50V, I_D = 63A
R_G	Gate Resistance	—	2.1	—	Ω	
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V_{DS} = 150V, V_{GS} = 0V
		—	—	250		V_{DS} = 150V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge	—	73	110	nC	I_D = 63A
Q_{gs}	Gate-to-Source Charge	—	28	—		V_{DS} = 75V
Q_{gd}	Gate-to-Drain Charge	—	28	—		V_{GS} = 10V④
Q_{sync}	Total Gate Charge Sync. (Q_g - Q_{gd})	—	45	—		
$t_{d(on)}$	Turn-On Delay Time	—	18	—	ns	V_{DD} = 98V
t_r	Rise Time	—	50	—		I_D = 63A
$t_{d(off)}$	Turn-Off Delay Time	—	37	—		R_G= 2.1Ω
t_f	Fall Time	—	23	—		V_{GS} = 10V④
C_{iss}	Input Capacitance	—	5320	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	490	—		V_{DS} = 50V
C_{rss}	Reverse Transfer Capacitance	—	110	—		f = 1.0MHz
$C_{oss\ eff.(ER)}$	Effective Output Capacitance (Energy Related)	—	450	—		V_{GS} = 0V, V_{DS} = 0V to 120V⑥
$C_{oss\ eff.(TR)}$	Effective Output Capacitance (Time Related)	—	520	—		V_{GS} = 0V, V_{DS} = 0V to 120V⑤

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	104	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	420		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 63A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	82	—	ns	T_J = 25°C V_{DD} = 130V
		—	99	—		T_J = 125°C I_F = 63A,
Q_{rr}	Reverse Recovery Charge	—	271	—	nC	T_J = 25°C di/dt = 100A/μs ④
		—	385	—		T_J = 125°C
I_{RRM}	Reverse Recovery Current	—	6.0	—	A	T_J = 25°C
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.
② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.115mH, R_G = 25Ω, I_{AS} = 63A, V_{GS} =10V. Part not recommended for use above this value.
③ $I_{SD} \leq$ 63A, di/dt $\leq$ 2510A/μs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 175°C.
④ Pulse width $\leq$ 400μs; duty cycle $\leq$ 2%.
⑤ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
⑥ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994
⑧ R_θ is measured at T_J approximately 90°C.

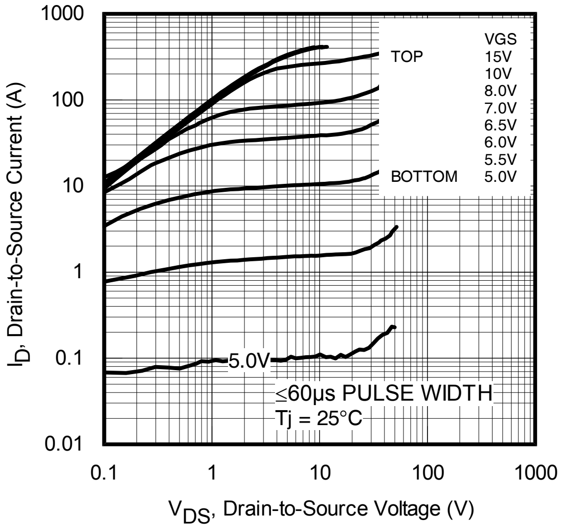


Fig. 1 Typical Output Characteristics

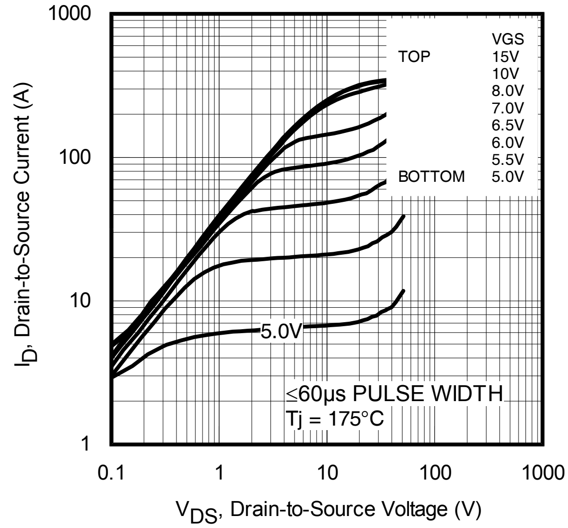


Fig. 2 Typical Output Characteristics

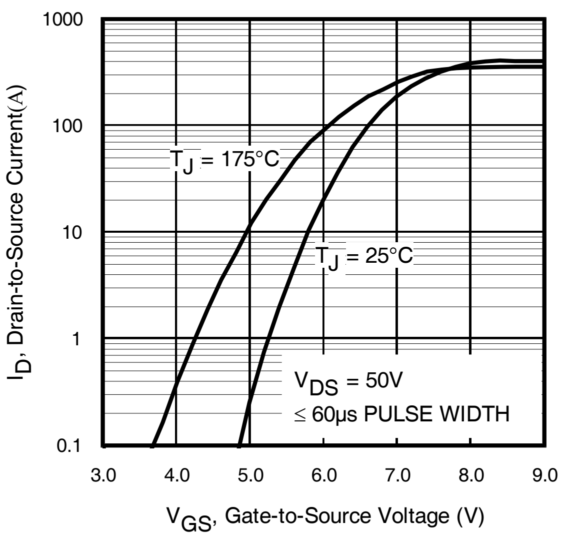


Fig. 3 Typical Transfer Characteristics

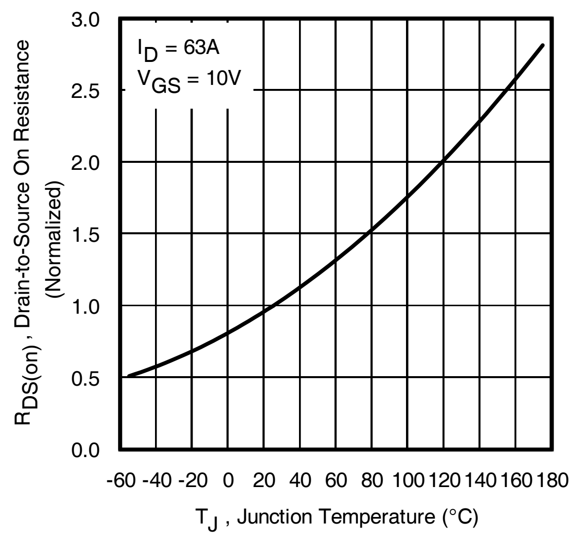


Fig. 4 Normalized On-Resistance vs. Temperature

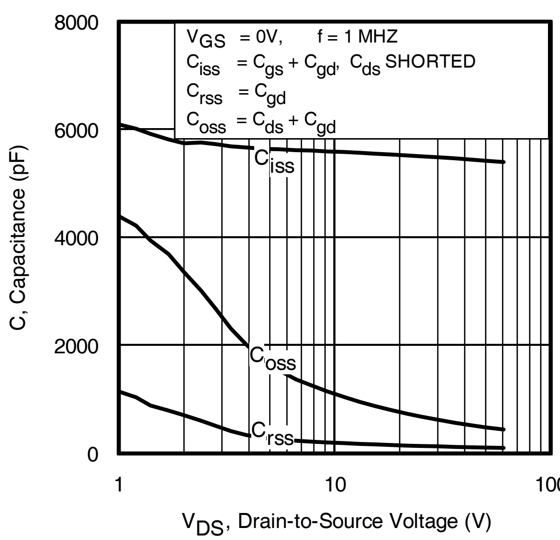


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

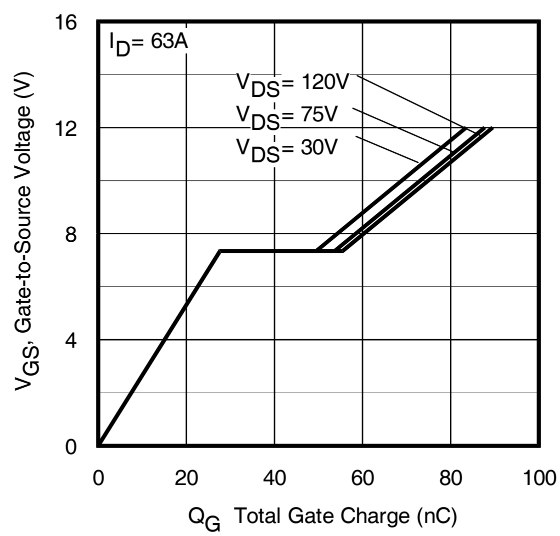


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

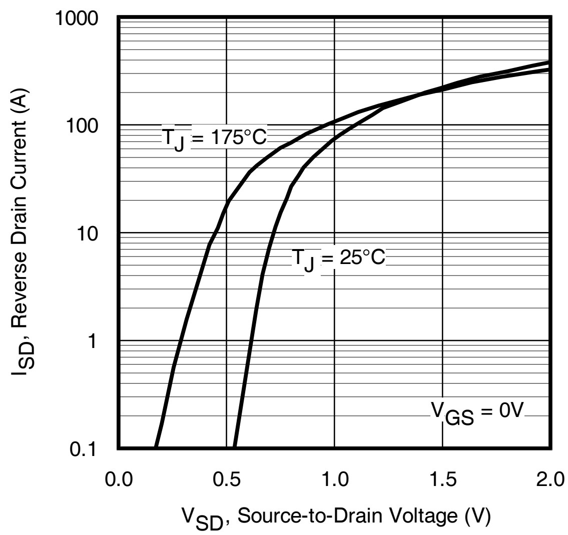


Fig. 7 Typical Source-to-Drain Diode

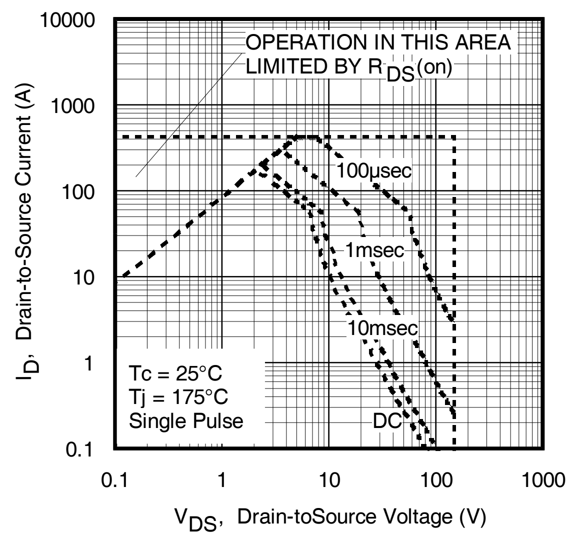


Fig 8. Maximum Safe Operating Area

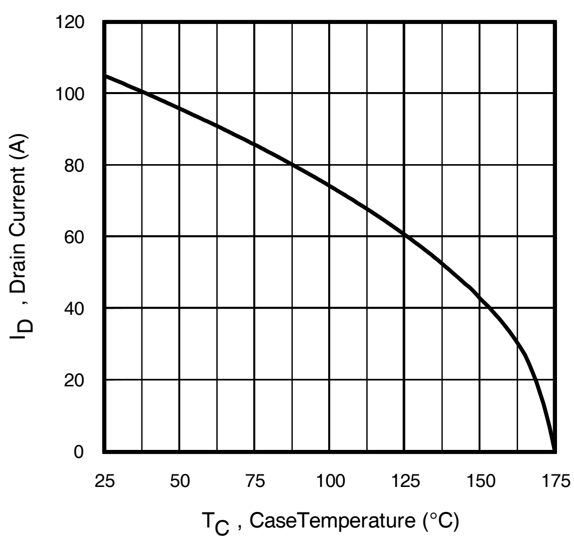


Fig 9. Maximum Drain Current vs. Case Temperature

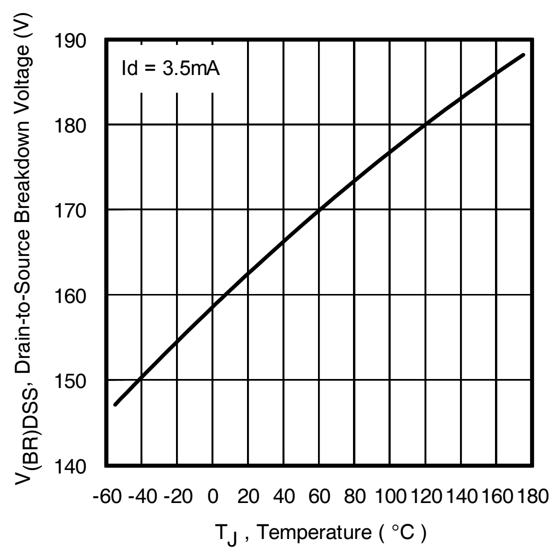


Fig 10. Drain-to-Source Breakdown Voltage

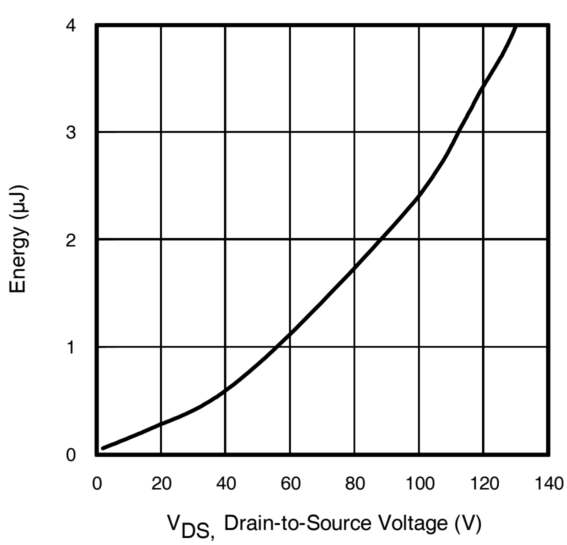


Fig 11. Typical Coss Stored Energy

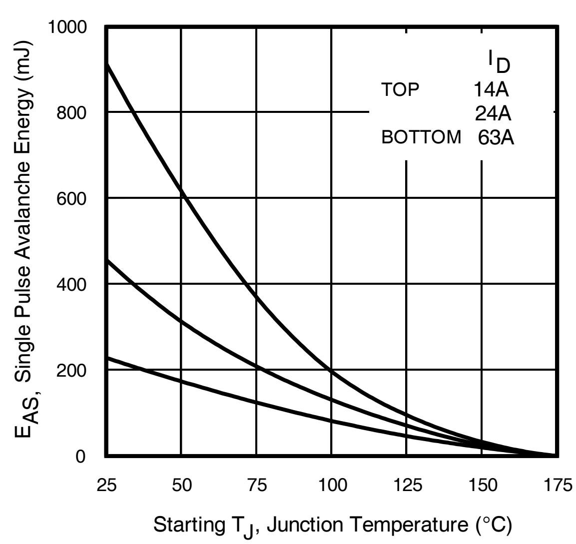


Fig 12. Maximum Avalanche Energy vs. Drain Current

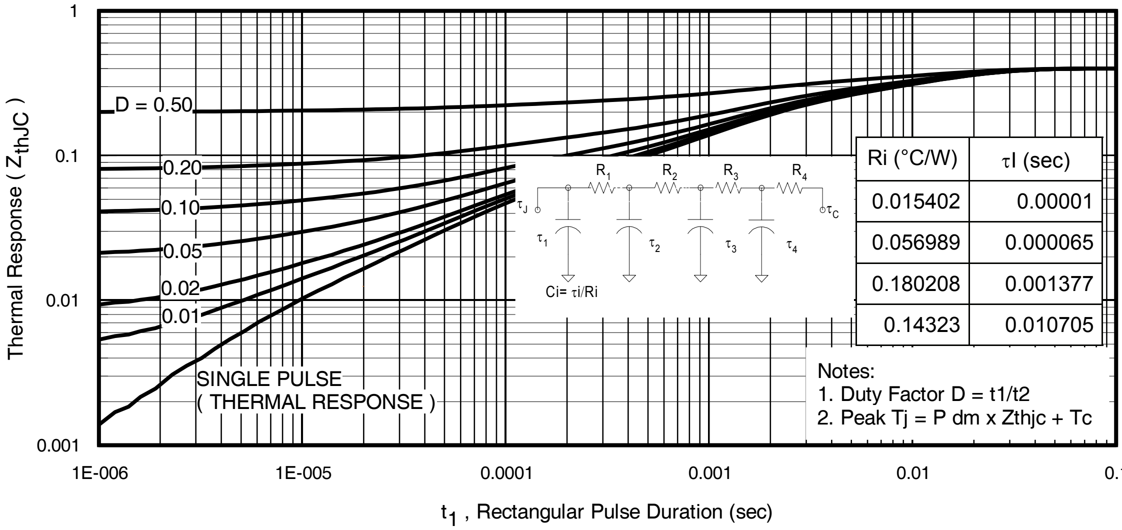


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

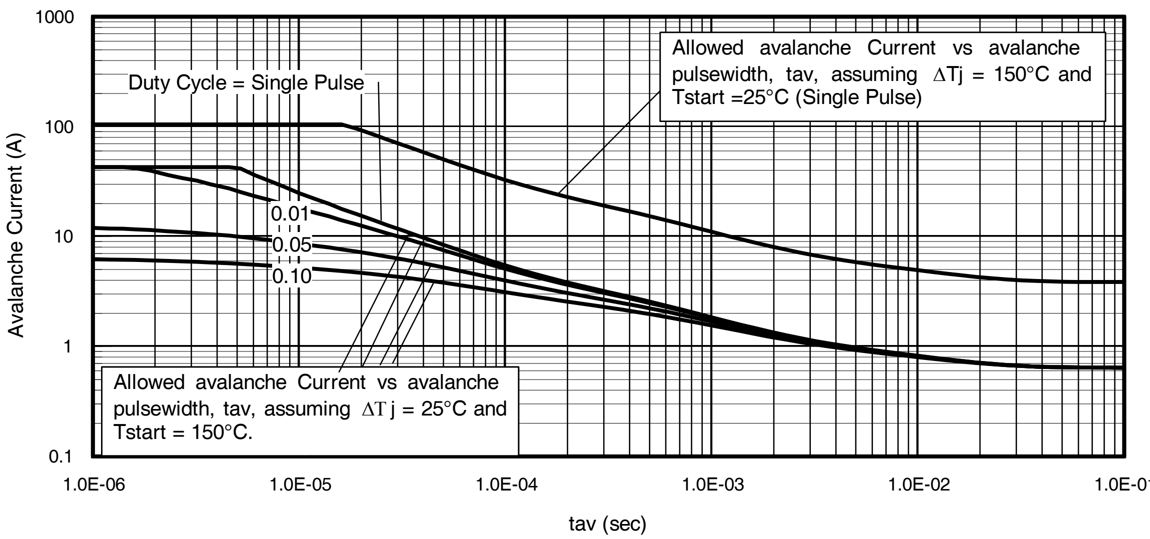


Fig 14. Avalanche Current vs. Pulse width

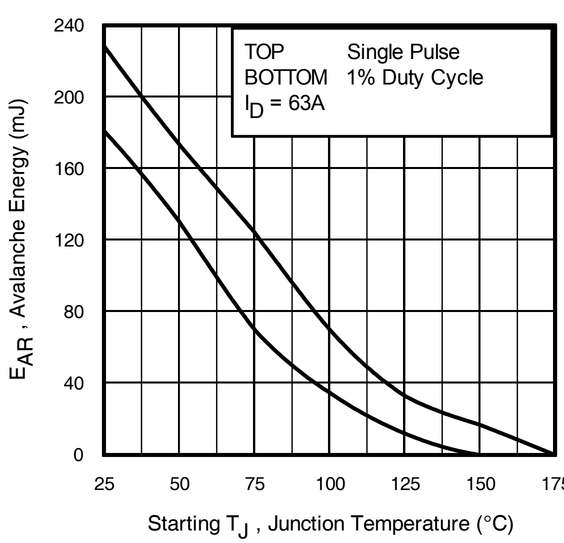


Fig 15. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.infineon.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 18a, 18b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 13, 14).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

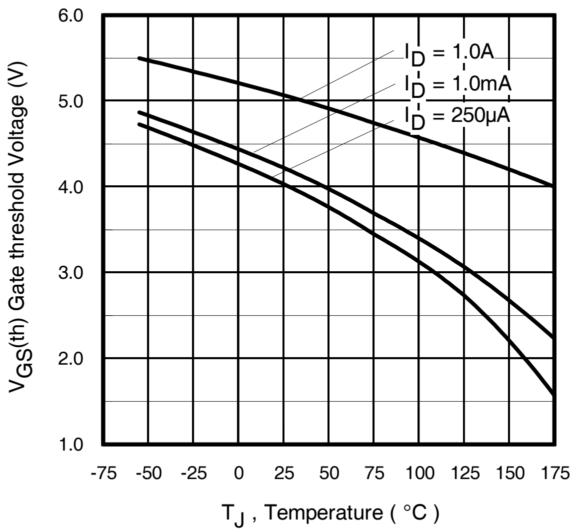


Fig 16. Threshold Voltage vs. Temperature

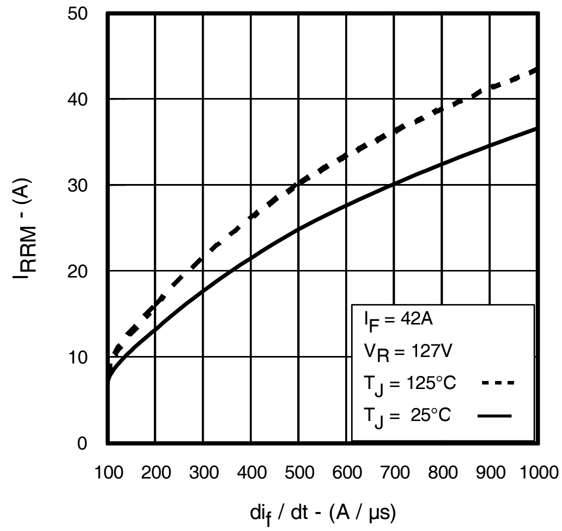


Fig. 17 - Typical Recovery Current vs. dif/dt

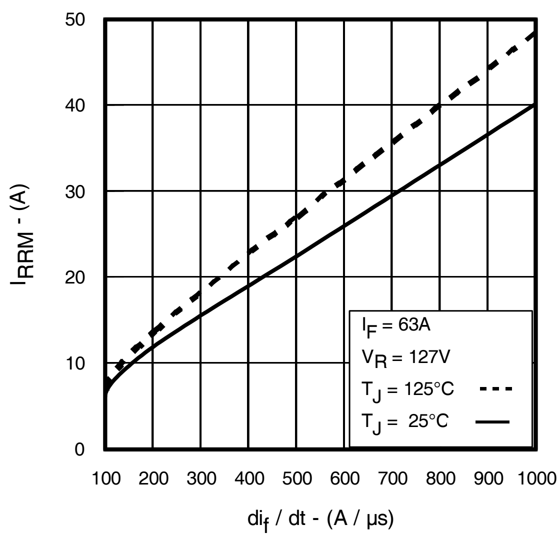


Fig. 18 - Typical Recovery Current vs. dif/dt

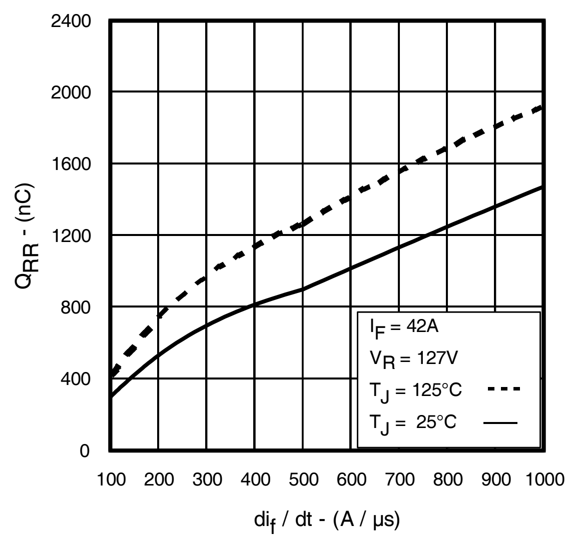


Fig. 19 - Typical Stored Charge vs. dif/dt

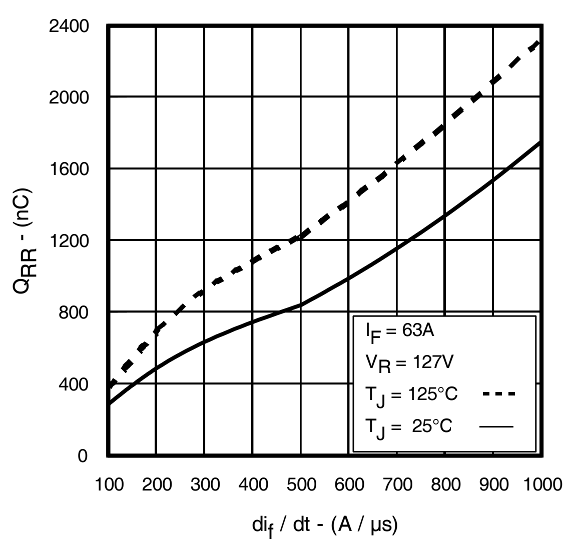


Fig. 20 - Typical Stored Charge vs. dif/dt

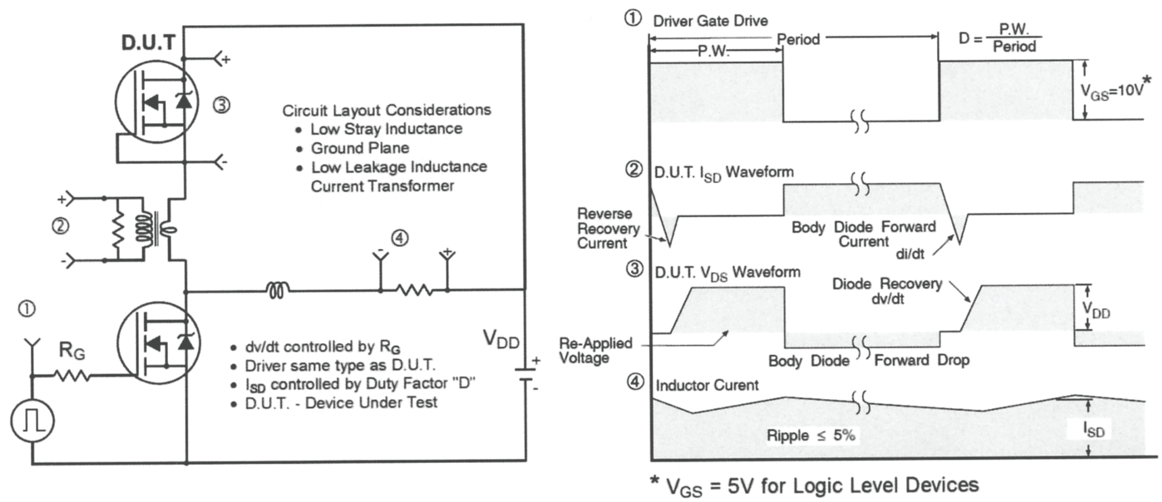


Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

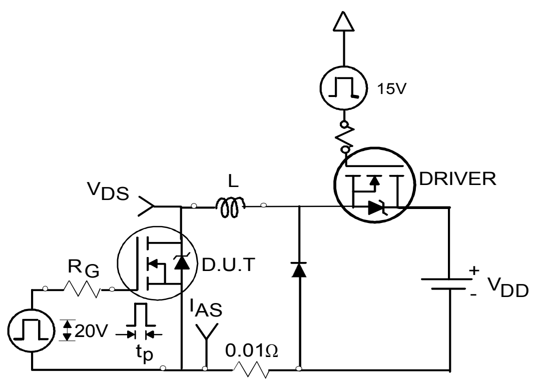


Fig 22a. Unclamped Inductive Test Circuit

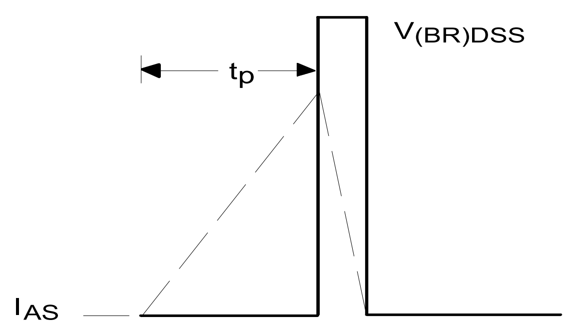


Fig 22b. Unclamped Inductive Waveforms

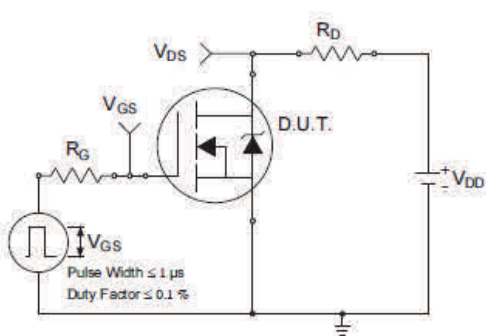


Fig 23a. Switching Time Test Circuit

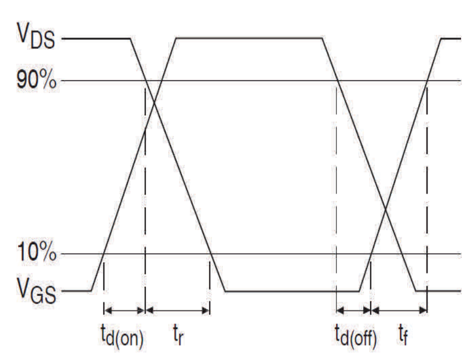


Fig 23b. Switching Time Waveforms

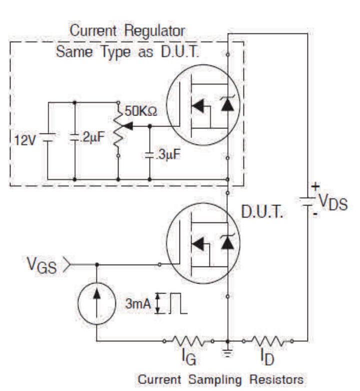


Fig 24a. Gate Charge Test Circuit

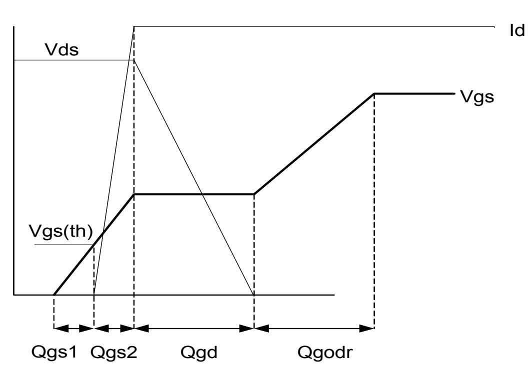
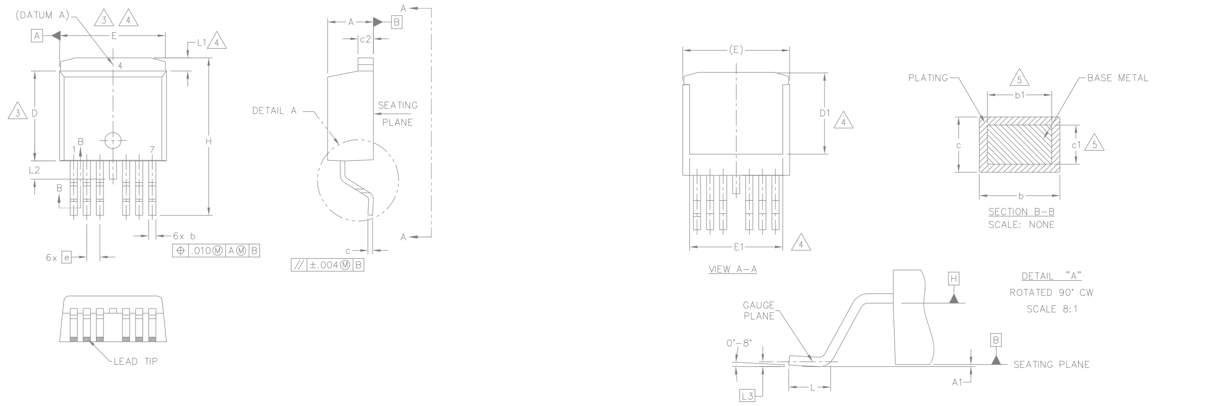


Fig 24b. Gate Charge Waveform

D²Pak - 7 Pin Package Outline (Dimensions are shown in millimeters (inches))

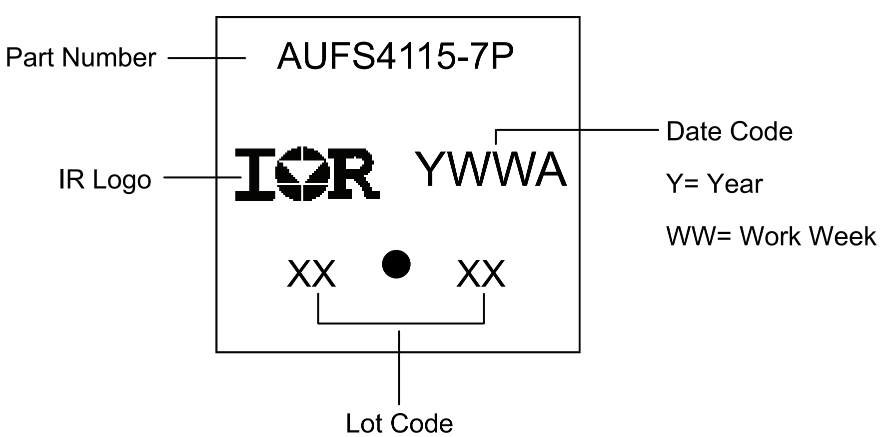


SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	–	0.254	–	.010	
b	0.51	0.99	.020	.036	
b1	0.51	0.89	.020	.032	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	7.42	.270	.292	4
E	9.65	10.54	.380	.415	3,4
E1	6.22	8.48	.245	.334	4
e	1.27 BSC		.050 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	–	1.68	–	.066	4
L2	–	1.78	–	.070	
L3	0.25 BSC		.010 BSC		

NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M–1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO–263CB. EXCEPT FOR DIMS. E, E1 & D1.

D²Pak - 7 Pin Part Marking Information



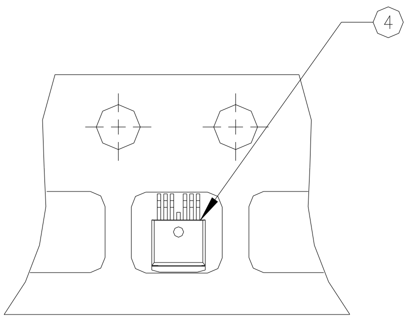
Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

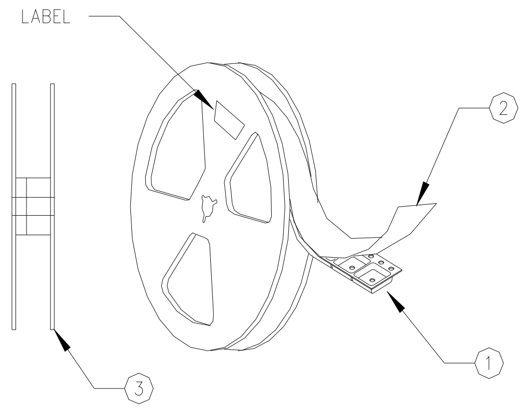
D²Pak - 7 Pin Tape and Reel

NOTES, TAPE & REEL, LABELLING:

1. TAPE AND REEL.
   1.1 REEL SIZE 13 INCH DIAMETER.
   1.2 EACH REEL CONTAINING 800 DEVICES.
   1.3 THERE SHALL BE A MINIMUM OF 42 SEALED POCKETS CONTAINED IN THE LEADER AND A MINIMUM OF 15 SEALED POCKETS IN THE TRAILER.
   1.4 PEEL STRENGTH MUST CONFORM TO THE SPEC. NO. 71-9667.
   1.5 PART ORIENTATION SHALL BE AS SHOWN BELOW.
   1.6 REEL MAY CONTAIN A MAXIMUM OF TWO UNIQUE LOT CODE/DATE CODE COMBINATIONS. REWORKED REELS MAY CONTAIN A MAXIMUM OF THREE UNIQUE LOT CODE/DATE CODE COMBINATIONS. HOWEVER, THE LOT CODES AND DATE CODES WITH THEIR RESPECTIVE QUANTITIES SHALL APPEAR ON THE BAR CODE LABEL FOR THE AFFECTED REEL.

2. LABELLING (REEL AND SHIPPING BAG).
   2.1 CUST. PART NUMBER (BAR CODE): IRFXXXXSTRL-7P
   2.2 CUST. PART NUMBER (TEXT CODE): IRFXXXXSTRL-7P
   2.3 I.R. PART NUMBER: IRFXXXXSTRL-7P
   2.4 QUANTITY:
   2.5 VENDOR CODE: IR
   2.6 LOT CODE:
   2.7 DATE CODE:





Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Qualification Information

Qualification Level		Automotive (per AEC-Q101) Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		D^2-Pak 7 Pin	MSL1
ESD	Machine Model	Class M3 (+/- 400V)† AEC-Q101-002	
	Human Body Model	Class H2 (+/- 4000V)† AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 2000V)† AEC-Q101-005	
RoHS Compliant		Yes	

† Highest passing voltage.

Revision History

Date	Comments
12/4/2015	• Updated datasheet with corporate template • Corrected ordering table on page 1.

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