



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

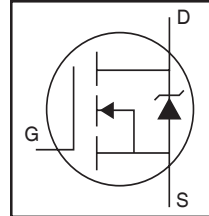


IRLS3036PbF IRLSL3036PbF

HEXFET® Power MOSFET

Applications

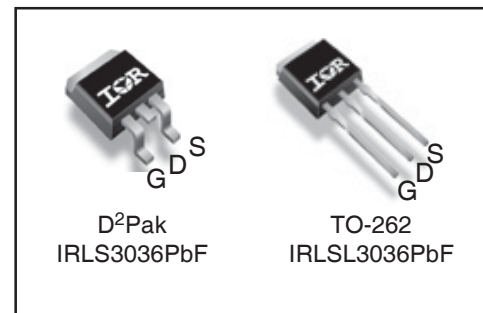
- DC Motor Drive
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits



V_{DSS}		60V
$R_{DS(on)}$	typ.	1.9mΩ
	max.	2.4mΩ
I_D (Silicon Limited)		270A ①
I_D (Package Limited)		195A

Benefits

- Optimized for Logic Level Drive
- Very Low $R_{DS(ON)}$ at 4.5V V_{GS}
- Superior R^*Q at 4.5V V_{GS}
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free



G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	270 ①	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	190 ①	
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Package Limited)	195	
I_{DM}	Pulsed Drain Current ②	1100	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	380	W
	Linear Derating Factor	2.5	W/°C
V_{GS}	Gate-to-Source Voltage	±16	V
dv/dt	Peak Diode Recovery ④	8.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

Avalanche Characteristics

E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ③	290	mJ
I_{AR}	Avalanche Current ②	See Fig. 14, 15, 22a, 22b	A
E_{AR}	Repetitive Avalanche Energy ⑩		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑨ ⑪	—	0.40	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount, steady state) ⑩	—	40	

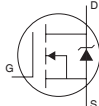
Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.061	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 5\text{mA}$ ②
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	1.9	2.4	m Ω	$V_{GS} = 10V, I_D = 165A$ ③
		—	2.2	2.8		$V_{GS} = 4.5V, I_D = 140A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.5	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 60V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 60V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 16V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -16V$
$R_{G(int)}$	Internal Gate Resistance	—	2.0	—	Ω	

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	340	—	—	S	$V_{DS} = 10V, I_D = 165A$
Q_g	Total Gate Charge	—	91	140	nC	$I_D = 165A$
Q_{gs}	Gate-to-Source Charge	—	31	—		$V_{DS} = 30V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	51	—		$V_{GS} = 4.5V$ ⑤
Q_{sync}	Total Gate Charge Sync. ($Q_g - Q_{gd}$)	—	40	—		$I_D = 165A, V_{DS} = 0V, V_{GS} = 4.5V$
$t_{d(on)}$	Turn-On Delay Time	—	66	—	ns	$V_{DD} = 39V$
t_r	Rise Time	—	220	—		$I_D = 165A$
$t_{d(off)}$	Turn-Off Delay Time	—	110	—		$R_G = 2.1\Omega$
t_f	Fall Time	—	110	—		$V_{GS} = 4.5V$ ⑤
C_{iss}	Input Capacitance	—	11210	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	1020	—		$V_{DS} = 50V$
C_{riss}	Reverse Transfer Capacitance	—	500	—		$f = 1.0\text{MHz}$
$C_{oss \text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related) ⑦	—	1430	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 48V$ ⑦
$C_{oss \text{ eff. (TR)}}$	Effective Output Capacitance (Time Related) ⑥	—	1880	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 48V$ ⑥

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	270	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ③	—	—	1100		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 165A, V_{GS} = 0V$ ⑤
t_{rr}	Reverse Recovery Time	—	62	—	ns	$T_J = 25^\circ\text{C}$ $V_R = 51V,$
		—	66	—		$T_J = 125^\circ\text{C}$ $I_F = 165A$
Q_{rr}	Reverse Recovery Charge	—	310	—	nC	$T_J = 25^\circ\text{C}$ $di/dt = 100A/\mu s$ ⑤
		—	360	—		$T_J = 125^\circ\text{C}$
I_{RRM}	Reverse Recovery Current	—	4.4	—	A	$T_J = 25^\circ\text{C}$
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

- ① Calculated continuous current based on maximum allowable junction temperature Bond wire current limit is 195A. Note that current limitation arising from heating of the device leads may occur with some lead mounting arrangements.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 0.021\text{mH}$
 $R_G = 25\Omega, I_{AS} = 165A, V_{GS} = 10V$. Part not recommended for use above this value.
- ④ $I_{SD} \leq 165A, di/dt \leq 430A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 175^\circ\text{C}$.
- ⑤ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- ⑥ $C_{oss \text{ eff. (TR)}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑦ $C_{oss \text{ eff. (ER)}}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note # AN-994.
- ⑨ $R_{\theta j}$ is measured at T_J approximately 90°C .
- ⑩ Limited by T_{Jmax} , see Fig. 14, 15, 22a, 22b for typical repetitive avalanche performance.
- ⑪ $R_{\theta jC}$ value shown is at time zero.

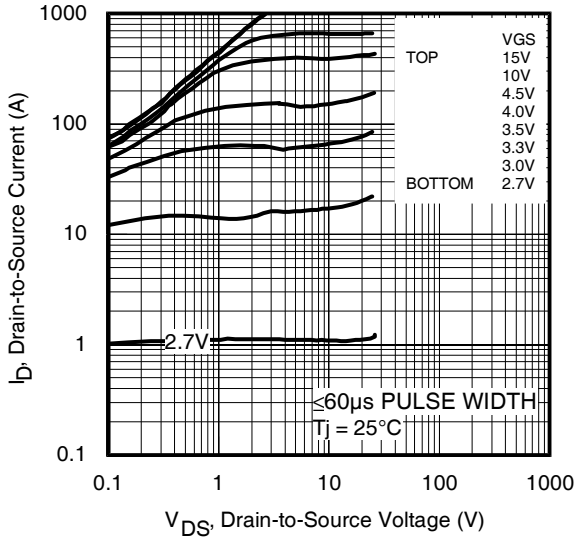


Fig 1. Typical Output Characteristics

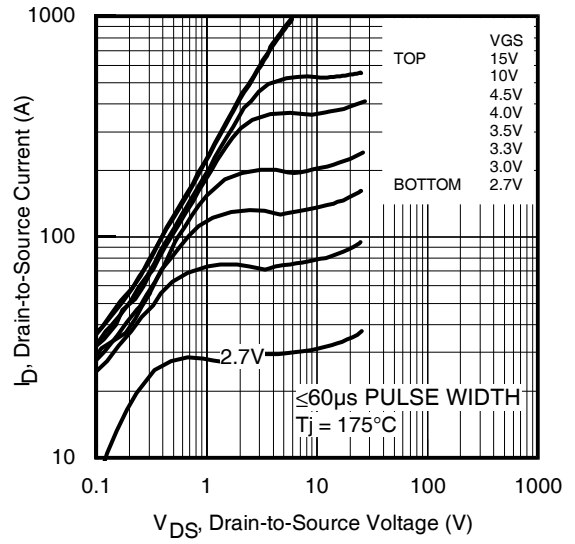


Fig 2. Typical Output Characteristics

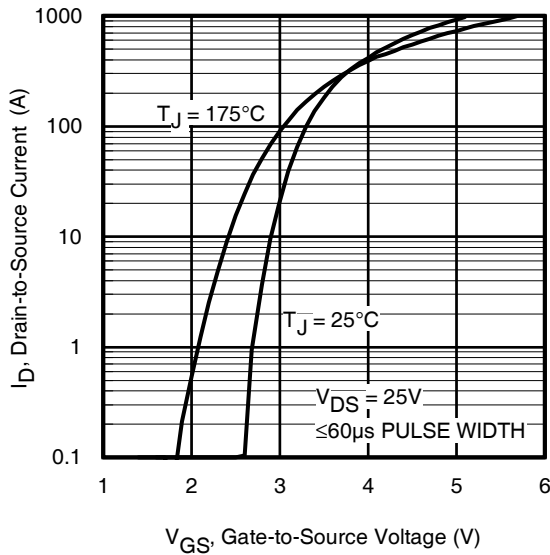


Fig 3. Typical Transfer Characteristics

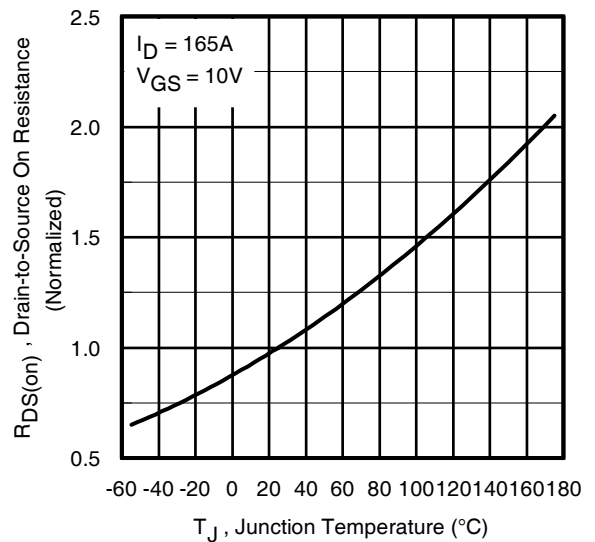


Fig 4. Normalized On-Resistance vs. Temperature

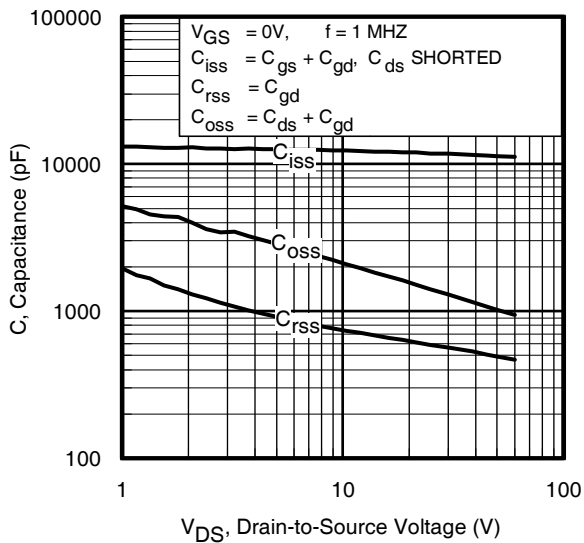


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

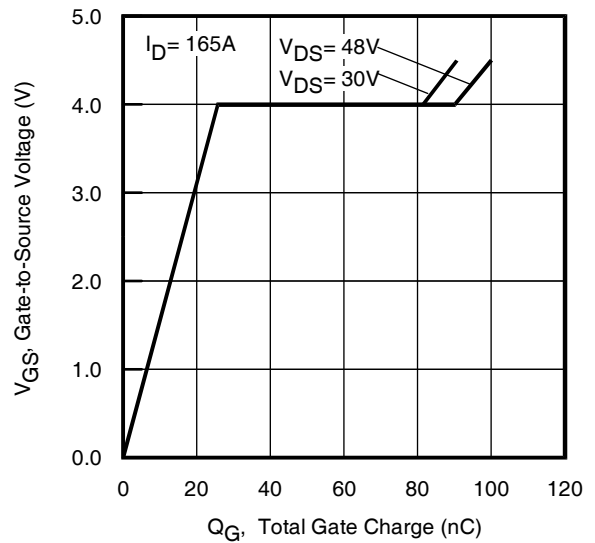


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

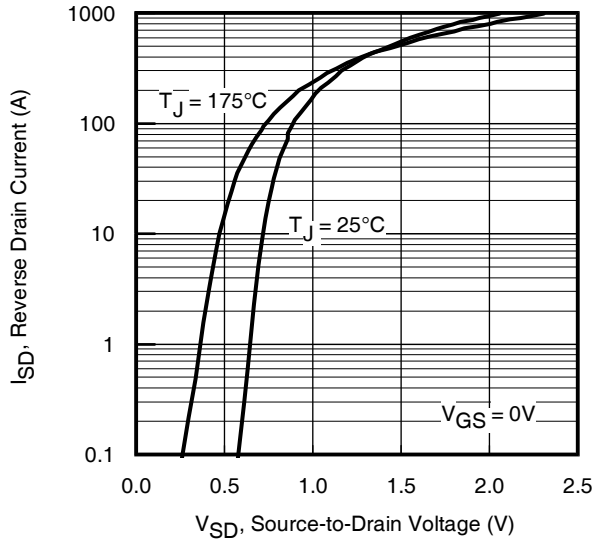


Fig 7. Typical Source-Drain Diode Forward Voltage

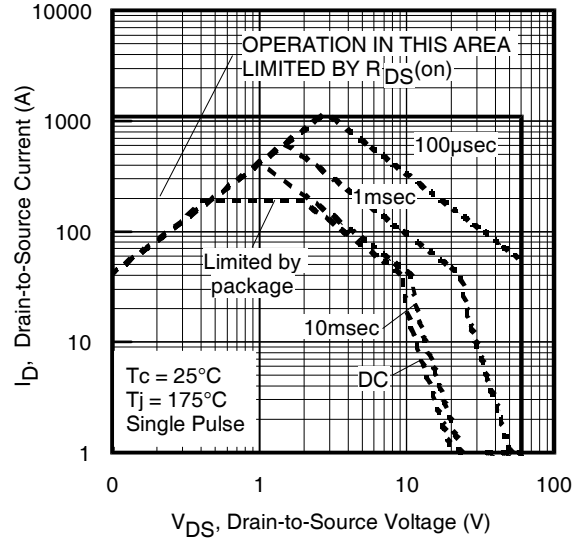


Fig 8. Maximum Safe Operating Area

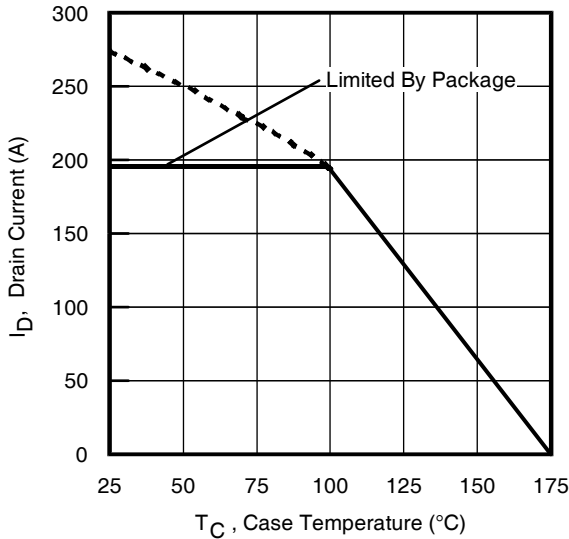


Fig 9. Maximum Drain Current vs. Case Temperature

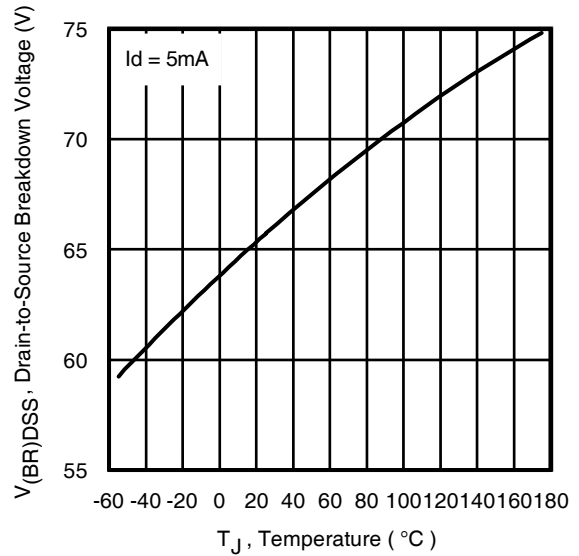


Fig 10. Drain-to-Source Breakdown Voltage

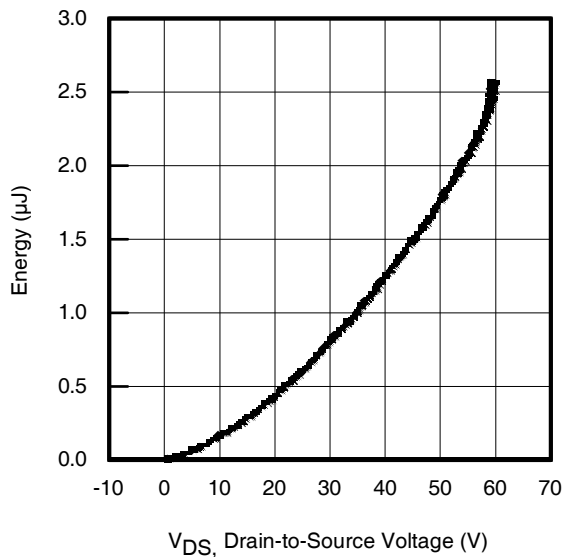


Fig 11. Typical C_{OSS} Stored Energy

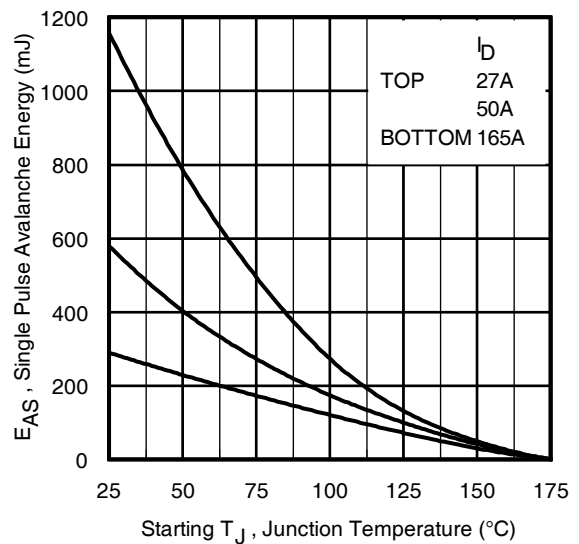


Fig 12. Maximum Avalanche Energy vs. Drain Current

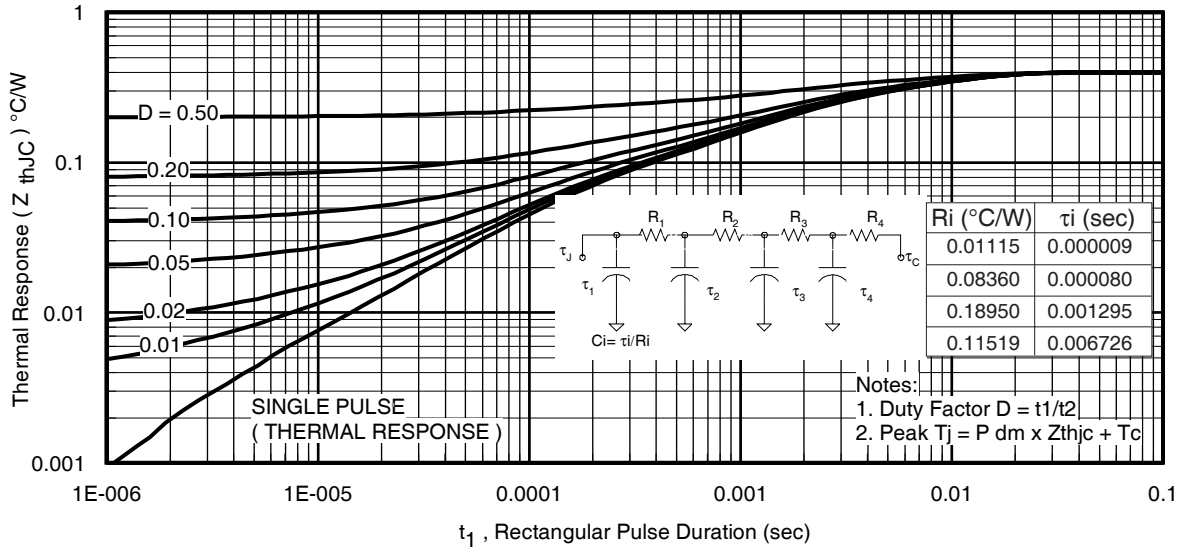


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

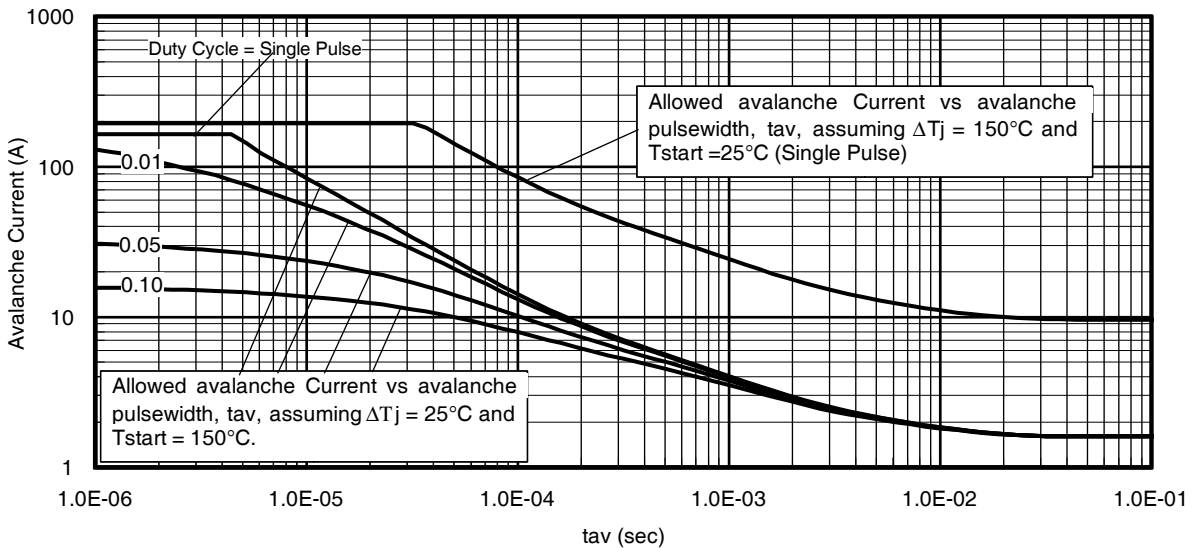


Fig 14. Typical Avalanche Current vs. Pulsewidth

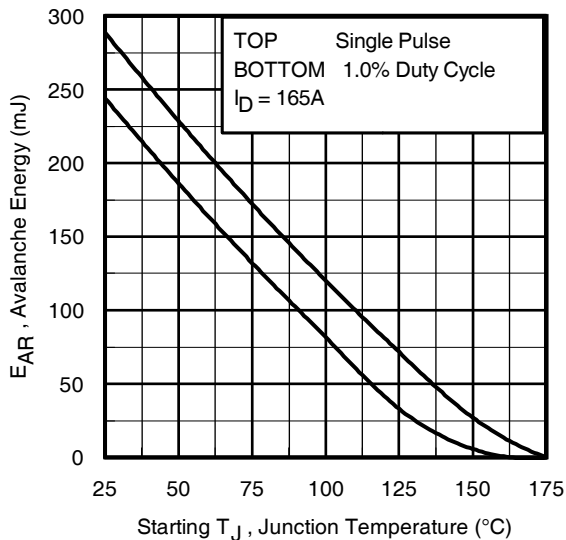


Fig 15. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves, Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

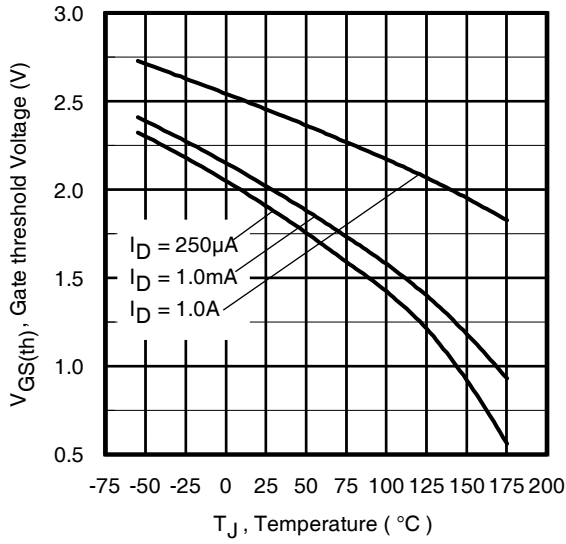


Fig 16. Threshold Voltage vs. Temperature

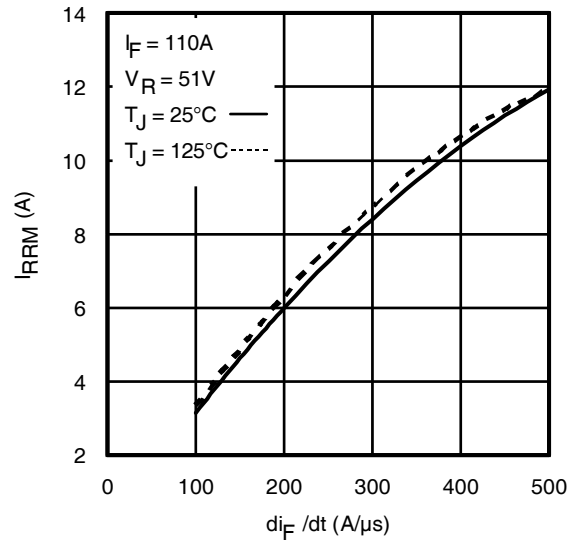


Fig. 17 - Typical Recovery Current vs. di_F/dt

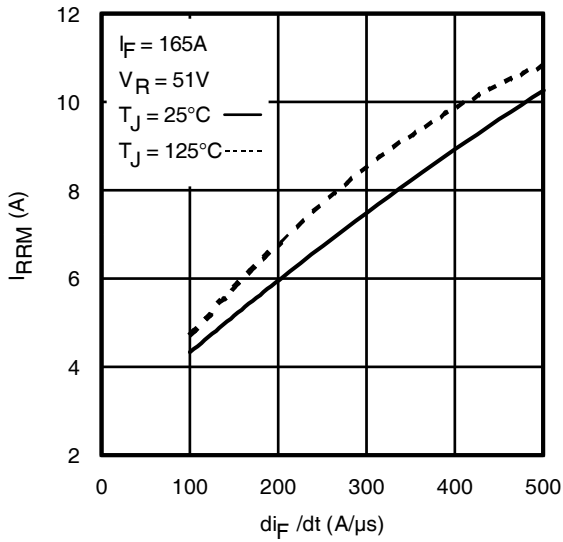


Fig. 18 - Typical Recovery Current vs. di_F/dt

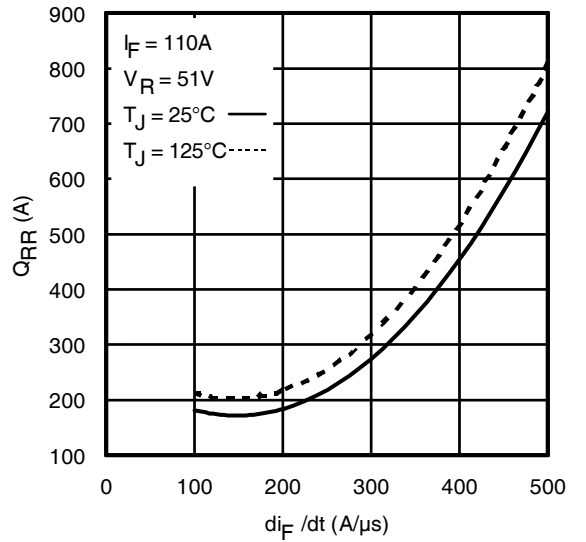


Fig. 19 - Typical Stored Charge vs. di_F/dt

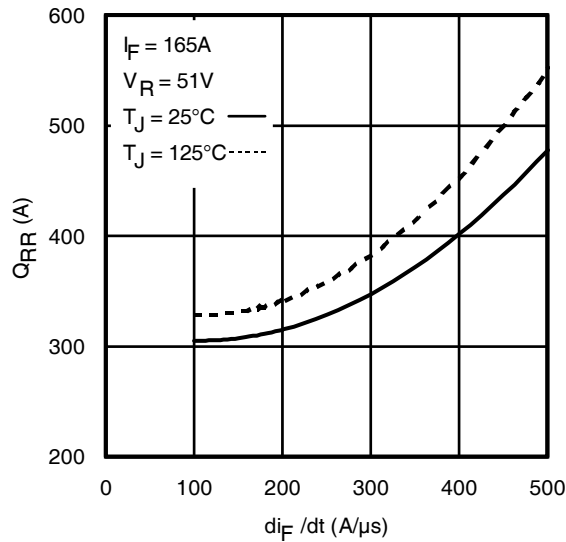


Fig. 20 - Typical Stored Charge vs. di_F/dt

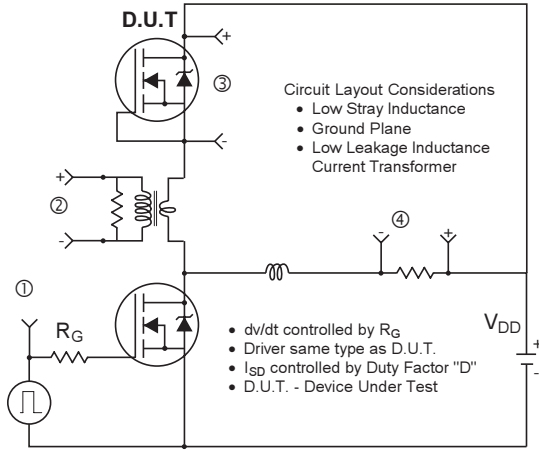
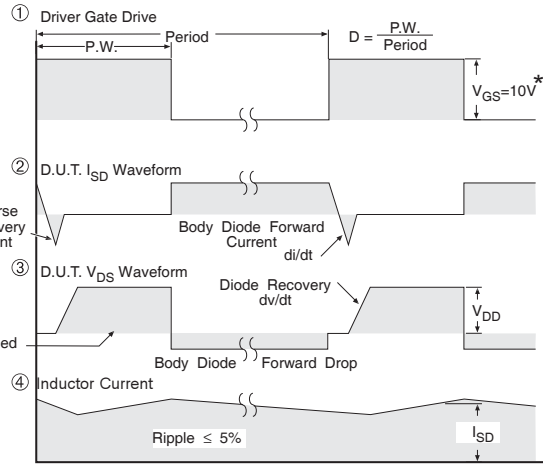


Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs



* $V_{GS} = 5V$ for Logic Level Devices

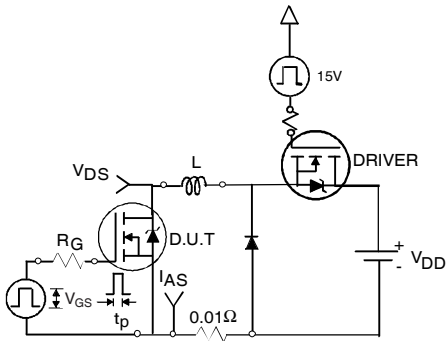


Fig 22a. Unclamped Inductive Test Circuit



Fig 22b. Unclamped Inductive Waveforms

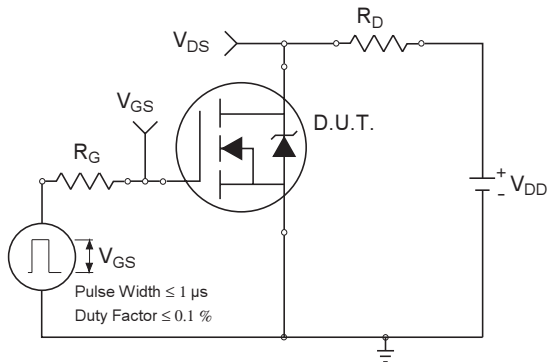


Fig 23a. Switching Time Test Circuit

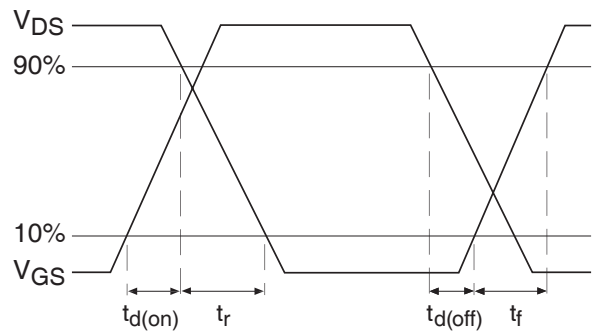


Fig 23b. Switching Time Waveforms

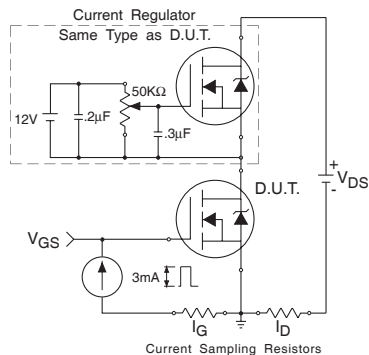


Fig 24a. Gate Charge Test Circuit

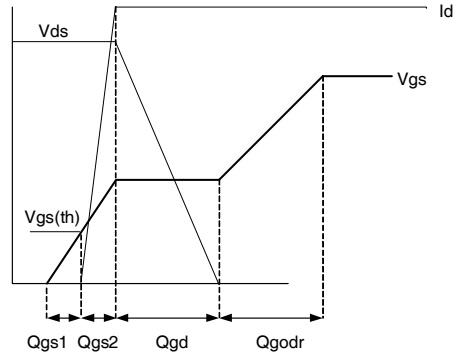
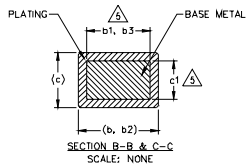
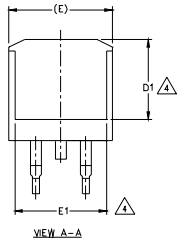
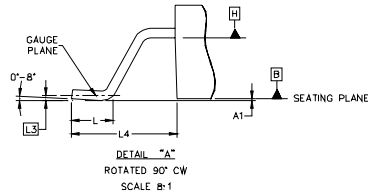
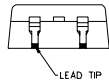
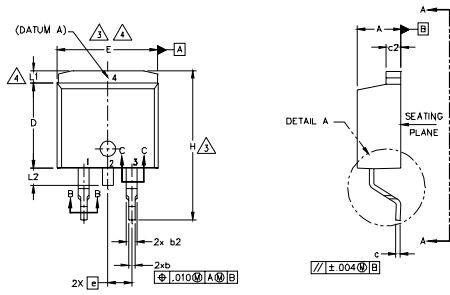


Fig 24b. Gate Charge Waveform

IRLS/SL3036PbF

D²Pak (TO-263AB) Package Outline

Dimensions are shown in millimeters (inches)



LEAD ASSIGNMENTS

DIODES

- 1.- ANODE (TWO DIE) / OPEN (ONE DIE)
2. - CATHODE
- 3.- ANODE

HEXFET

- 1.- GATE
2. - DRAIN
- 3.- SOURCE

IGBTs, CoPACK

- 1.- GATE
2. 4.- COLLECTOR
- 3.- EMITTER

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	
D1	6.86	-	.270	-	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	-	.245	-	4
e	2.54 BSC		.100 BSC		4
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	-	1.65	-	.066	
L2	-	1.78	-	.070	4
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	

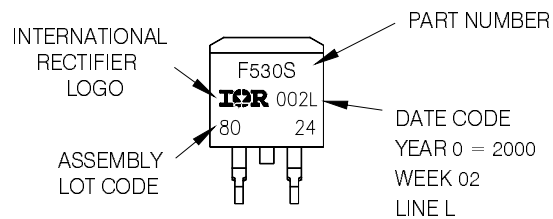
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

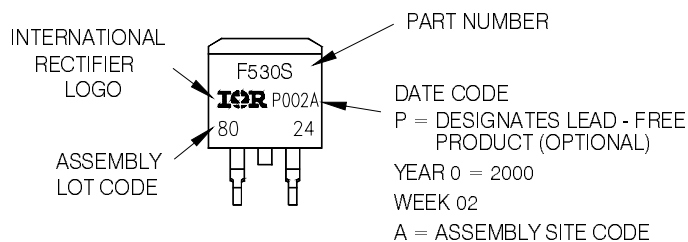
D²Pak (TO-263AB) Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position
indicates "Lead - Free"



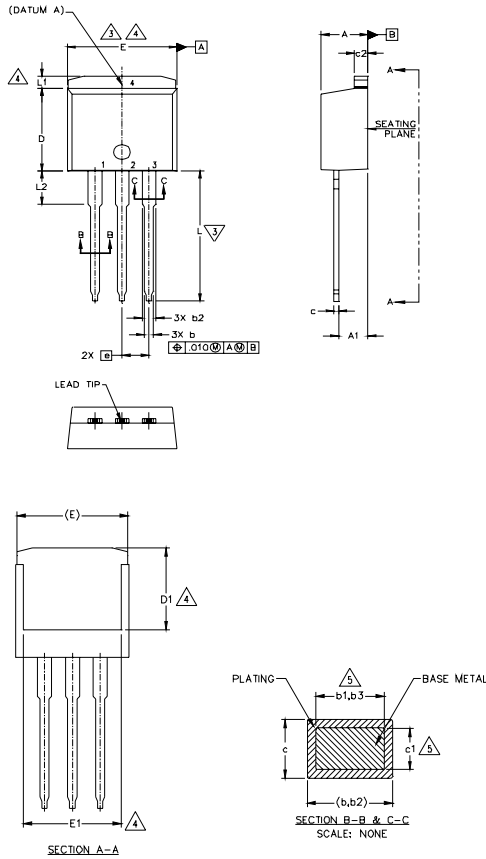
OR



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

TO-262 Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	—	.270	—	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	—	.245	—	4
e	2.54 BSC		.100 BSC		
L	13.46	14.10	.530	.555	
L1	—	1.65	—	.065	4
L2	3.56	3.71	.140	.146	

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 2. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)
 3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
 4. DIERNAL PAD CONTOUR OPTIONAL WITHIN DIMENSION L, L1, D1 & E1.
 5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
 6. CONTROLLING DIMENSION: INCH.
 7. - OUTLINE CONFORMS TO JEDEC TO-262 EXCEPT A1(max.), b1(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

LEAD ASSIGNMENTS

- IGBTs, GpPACs
- 1 - GATE
 - 2 - COLLECTOR
 - 3 - EMITTER
 - 4 - COLLECTOR

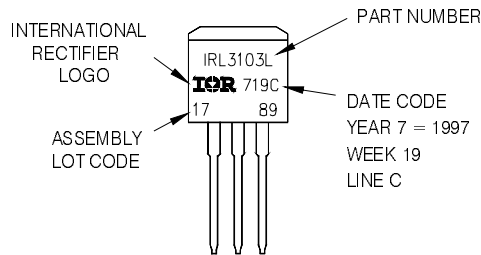
DIODES

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE
- 4 - DRAIN
- 1 - ANODE (NO DI) / OPEN (ONE DI)
- 2 - CATHODE
- 3 - ANODE

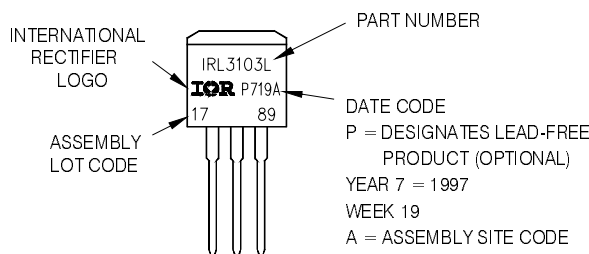
TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "p" in assembly line position indicates "Lead - Free"



OR

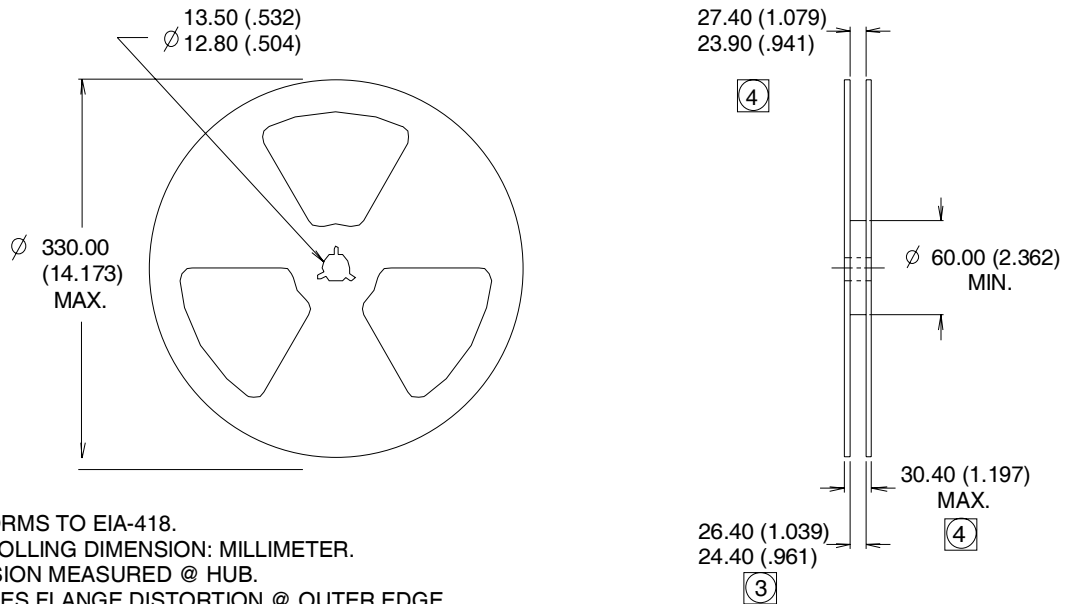
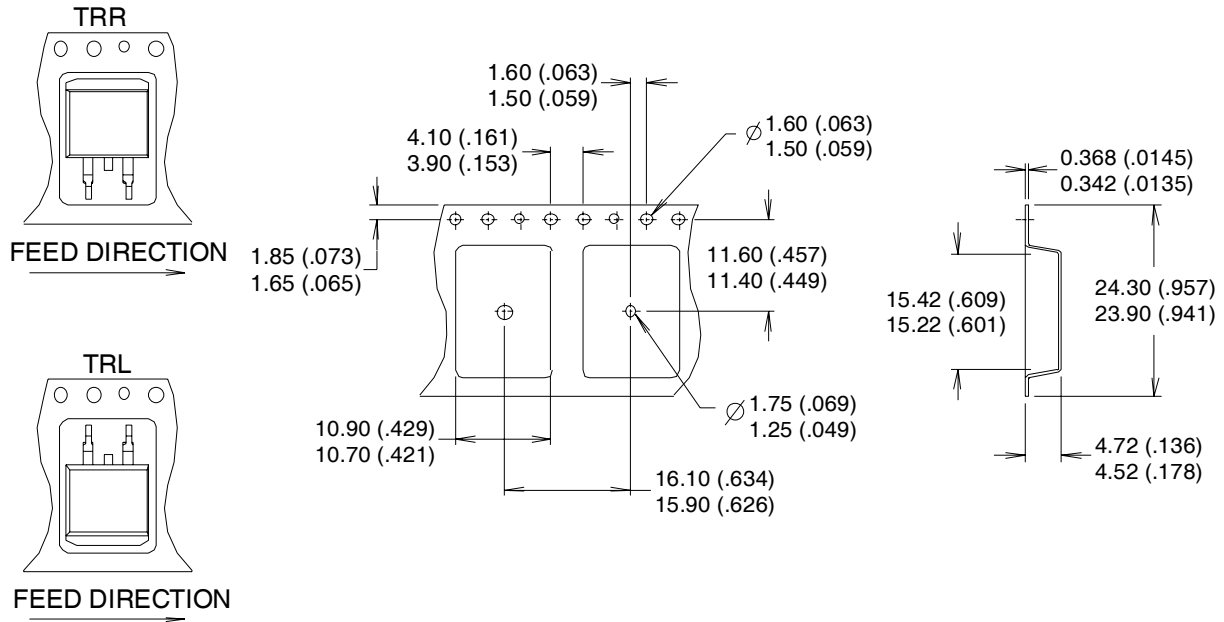


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

IRLS/SL3036PbF

D²Pak (TO-263AB) Tape & Reel Information

Dimensions are shown in millimeters (inches)



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Data and specifications subject to change without notice.
 This product has been designed and qualified for the Industrial market.
 Qualification Standards can be found on IR's Web site.